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CSI COMPUTER SYSTEM/REMOTE INTERFACE UNIT ACCEPTANCE TEST RESULTS

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Acronyms

The following acronyms are used throughout this document.

ACD	-	Analysis and Computation Division
A/D	-	Analog to Digital
AP	-	Array Processor
CAMAC	-	Computer Automated Measurement and Control
CSI	-	Control/Structures Interaction
CCS	-	CSI Computer System
CDPP	-	Console Debugger/Prom Programmer
CEM	-	CSI Evolutionary Model
COFS	-	Control of Flexible Structures
CPU	-	Central Processing Unit
D/A	-	Digital to Analog
DC	-	Direct Current
DSP	-	Digital Signal Processor
EDS	-	Excitation and Damping Subsystem Computer
FIR	-	Finite Impulse Response
FSGB	-	Flight Software and Graphics Branch
GSE	-	Ground Support Equipment
GSET	-	Ground Support Equipment Terminal
HRM	-	High Rate Multiplexer
IIR	-	Inifinte Impulse Response
I/O	-	Input-Output
RIU	-	Remote Interface Unit
SED	-	System Engineering Division
SSRL	-	Space Structures Research Laboratory

Purpose

The purpose of this document is to report on the testing of the Control/Structures Interaction (CSI) Computer System (CCS)/Remote Interface Unit (RIU), which was installed in the Space Structures Research Laboratory (SSRL) for use in conducting real time control experiments on the the CSI Evolutionary Model (CEM). The test work performed on the CCS/RIU in the SSRL is an extension of the earlier test work performed on a duplicate CCS and the RIU in the Flight Software

and Graphics Branch (FSGB) Laboratory at the Analysis and Computation Division (ACD) in March 1991. This document is organized in the following manner. First, a brief description of the overall CCS/RIU system is given. Then, the various tests performed on the CCS/RIU - hardware acceptance, software/control computations, open loop, closed loop, RIU digital filtering and RIU standalone - are discussed. Next, a section outlining the system's development problems, their solutions and recommendations for improvement is presented. Finally, a short summary section closes the document.

System Description

The CCS is intended to allow researchers to conduct real time control tests on a computer system with spaceflight qualified components. The CCS was manufactured by SCI of Huntsville, Alabama, originally for the cancelled Control of Flexible Structures (COFS) flight project, and consists of four major components: the Console Debugger/Prom Programmer (CDPP), the Excitation and Damping System Computer (EDS)[1], the Ground Support Equipment (GSE), and the Ground Support Equipment Terminal (GSET). In addition, two other components, the Remote Interface Unit (RIU)[2] and a dumb graphics terminal, have been interfaced with the CCS. The function(s) of each component is briefly explained below:

Console Debugger/Prom Programmer (CPDD) - The CDPP consists of two parts: a PC XT and a prom burning expansion chassis. The PC XT is primarily used to download software to the EDS via a RS 422 serial interface, while the prom burner is used to re-program the proms on the mass memory and MIL-STD 1750A Central Processing Unit (CPU) boards of the EDS, when necessary. Another function of the CDPP is to provide the user access to the EDS for the purpose of quickly halting the control law computations, and thus the control test, in case of emergencies.

Excitation and Damping System (EDS) - This unit is the 'brain' of the CCS, performing the real time control computations. It houses 1750A CPU, mass memory, MIL-STD 1553B communication, and array processor (AP) boards, all of which are spaceflight qualified. The AP performs the matrix control law computations, and is capable of handling controllers with up to 100 states. Sensor signals and the computed actuator commands are received and transmitted, respectively, on 1553B data bus, which also has been qualified for space operations. The EDS is unique in that it derives its power (112 W) from one of three direct current (DC) power supplies contained in the GSE (the other CCS components draw their power from standard 120 VAC wall socket sources).

Ground Support Equipment (GSE) - The GSE was originally built to simulate a Shuttle input-output (I/O) interface between the CCS and the experimental test article. It contains three DC power supplies, 1750A CPUs and a High Rate Multiplexer (HRM) for I/O processing, 1553B and IEEE 488 communication interfaces, and a 9-track magnetic tape drive system for test data storage. The initial power requirement specifications for the GSE called for 240 VAC and 30 amps, however, subsequent discussions with the manufacturer revealed that a standard 120 VAC wall socket source supply was sufficient. During the CCS development phase, a decision was made to bypass the I/O interfaces provided by the GSE for operations in the SSRL. It was felt, for the purpose of testing in the SSRL, that the I/O functions could be handled more efficiently by the GSET. Thus, in the current configuration, the one power supply which directly powers the EDS is the only part of the GSE which will be used during normal test operations.

Ground Support Equipment Terminal (GSET) - The GSET is a 80286 based PC with a 20 inch color monitor, and serves as the user interface to the CCS. Here, the user enters in the parameters which define the real time control experiment to be conducted, i.e., sensor and actuator selections, sampling rate and length of test, analog and digital filter selections, disturbance excitation types and sources, control law matrices and instrument scale factors. The GSET also communicates hardware and software error and warning messages to the user and computes pre-test sensor biases. Finally, the GSET records the real time test data (sensor signals and actuator commands) off of the 1553B data bus onto its hard disk drive, and converts it into ASCII format. Currently, there is no analysis software on the GSET; an ETHERNET interface has been installed to transfer the data to other systems for post-test analysis. The GSET has enough free hard disk space (25 megabytes at present) to hold data from multiple test runs.

Remote Interface Unit (RIU) - The RIU performs the data acquisition and filtering duties for the CCS. Built in-house, by the System Engineering Division (SED), this unit provides 16 input channels, multiplexed to a single 12-bit A/D converter, as well as 8 output channels, multiplexed into two 12-bit D/A converters (4 channels each). The RIU also provides limited analog low pass filtering, for anti-aliasing, and a Digital Signal Processor (DSP) board for digital filtering. With the DSP, the RIU has the capability to perform real time control tests itself in a so called "standalone" mode, i.e., with the CCS out of the loop. In the normal mode, the RIU communicates with the CCS via the 1553B bus. A 28 VDC, 7 amp power supply, also built by SED, provides the necessary power.

Graphics Terminal - A dumb graphics terminal has been provided, primarily for viewing the test data. Via a standard ROLM phone/data link, the user can log on to other systems, to which

the test data has been previously sent (e.g., a VAX with PRO-MATLAB) for post-test analysis work.

Figure 1 shows the major components and their respective connections.

Figure 2 is a schematic showing the CCS/RIU system within the SSRL. The data flow is as follows. Analog sensor signals come into the SSRL Control Trailer, through the safety PC and signal conditioning amplifiers. The analog sensor signals are then sent from the main patch panel to the RIU, where they are converted to digital signals and filtered as required. These signals are then sent to the CCS back inside the Control Trailer via the 1553B bus for use in control law computations. The resulting digital actuator commands are transmitted to the RIU down the 1553B, where they are converted to analog signals. These analog actuator commands are sent into the Control Trailer and finally out to the CEM.

CCS Hardware Acceptance Test

SCI has provided a detailed procedure for the express purpose of testing the functionality of CCS hardware. The full hardware acceptance test was performed after initial system delivery into the SSRL in August 1990, and a portion of this test was repeated to ensure that the CCS hardware, specifically the EDS, was still functioning properly. Since the current CCS will not use the GSE during actual operations, other than a power supply for the EDS, the GSE I/O tests were not performed. Only those tests involving the EDS were conducted, and they covered the following:

- voltage and power supply
- array processor (AP)
- 1750A CPU
- 1553 bus communication
- shared memory between the AP and 1750A CPU

The hardware acceptance tests indicated that the EDS, as well as the other CCS components in the SSRL, were functioning properly and were ready for further testing with the RIU. Appendices A and B contain the general log and error log file printouts, respectively, for these CCS hardware acceptance tests. The general log file reflects the user inputs and on-screen responses from the tests, while the error log file contains a more detailed listing of test result messages.

Dummy Control Computation Tests

After the completion of the CCS hardware tests, a series of so called "dummy" control experiments were executed on the CCS. These tests, nine in all, are referred to as "dummy" experiments because they were designed to test the CCS software, specifically the EDS computational software, and not as actual laboratory control experiments. All the control law matrices were made up arbitrarily - since the computed actuator commands were never transmitted to the CEM, little thought was given to the performance or stability of these control laws. Instead, emphasis was placed on exercising the features of the CCS software. The sensor signals and CCS computed actuator commands were recorded for each test for post-test analysis. Each set of recorded sensor signals was transferred to a VAX workstation for use in a PRO-MATLAB simulation of the corresponding "dummy" control experiment, with the CCS computed actuator commands being compared to the actuator commands obtained in the simulation for verification purposes.

Table 1 shows the major parameters that describe each of the "dummy" tests. The column entries are as follows: column 1 contains the "dummy" test number; columns 2 and 3, the number of sensors and actuators used in the test, respectively; column 4, the CCS digital sampling rate; column 5, the type of control feedback; column 6, the number of controller states; column 7, the types of disturbance excitations which were used.

Table 1. Dummy computation control tests.

Test No.	No. of Sensors	No. of Actuators	Sampling Rate (Hz)	Control Type	Control States	Excitation Type(s)
1	4	8	150	output	0	p
2	1	1	150	state	2	none
3	1	8	100	output	0	s,p,r
4	8	8	100	state	100	s,p,r
5	8	8	100	state	2	p
6	8	1	150	output	0	s
7	8	1	150	state	50	none
8	8	6	150	state *	100	s,r
9	8	8	150	output **	0	none

p - pulse; s - sine; r - random

* - The controller was not turned on during the test, thus, the actuator commands only involved the defined excitations.

** - The control gain matrix was set equal to the identity matrix, i.e., the actuator commands were equal to the sensor signals.

These "dummy" control experiments were actually executed twice on the CCS/RIU. For the first time, a signal generator was connected directly to the RIU, and sine waves were used to mimic sensor signals. A single constant frequency output from the signal generator was used, this being split into the appropriate number of sensor channels for each test. It should be noted that with this particular configuration, the data flow did not go through the SSRL Control Trailer (see Figure 2), rather, the data flow was exclusively through the 1553B data bus. In all nine tests with the signal generator, the EDS computed actuator commands matched their counterpart PRO-MATLAB simulated actuator commands for the same set of recorded sensor signals. The recorded sensor signals themselves were checked by plotting their time histories on the VAX and visually verifying the signals' frequencies and amplitudes against the known parameters set on the signal generator.

The next round of tests was conducted with the CEM sensors, servo accelerometers #1-8, connected to the RIU. The CEM actuators for the tests, though not yet physically connected to the CCS/RIU, were thrusters #1-8, referring to the eight air thruster pairs on the CEM[3]. Since each pair of thrusters act in unison, they will be referred to as single actuators for the remainder of this document. The CEM was manually excited, and the free response data from the accelerometers were recorded and used in real time in the nine "dummy" control tests. Figures 3a-d show the time histories of the first four accelerometers, respectively, for test #1, while Figures 4a-p show the corresponding thruster command time histories, as computed by the CCS in real time and by the PRO-MATLAB simulation, respectively. Test #1 ran for 40 seconds, with the controller turned on for the last 20 seconds. Note that the 1 lb spike at 20 seconds for thruster #1 (Figure 4a) reflects a commanded 1 lb pulse (duration was 1 time sample, i.e., 0.0067 seconds) at the initiation of the controller. The CCS actuator command and the PRO-MATLAB simulation actuator command matched for each thruster. This result was true for the other eight "dummy" control experiments. This indicated that the CCS software, particularly the EDS computational software, was performing as desired, and that open loop tests with the CEM could commence.

As a further study into the computational capability of the CCS, another set of "dummy" control experiments, each with 8 inputs and 8 outputs, but varying control matrices' sizes, were executed

to determine achievable throughput speeds on the CCS. Appendix C contains the details on these particular tests.

Open Loop Tests with the CEM

Once the CCS control computational software tests were passed, the thrusters were connected to the CCS/RIU for open loop command testing. For these tests, thruster commands were transmitted from the CCS to the CEM, however, no control law computations were performed, only the programmed excitation commands were used to drive the CEM. The current CCS software is capable of commanding three different types of excitations for use as disturbances. They are as follows: constant frequency sine waves, single pulses (of one sample period duration), and uniform random excitation. In the CCS software, any actuator can be commanded to output any of the above three excitations during a test, although each thruster can only be commanded to perform one type of excitation per test.

Along with the digital accelerometer signals and thruster commands, which were recorded on the GSET from each test, strip chart recordings of the corresponding analog accelerometer signals and thruster commands were also available as further checks on the open loop tests. In fact, as a precautionary measure, for the first few open loop tests, the thruster commands from the CCS were not sent out of the Control Trailer to the CEM, but merely recorded on the strip charts to verify the open loop commands. Only after these open loop commands were confirmed on the strip charts, were they sent out to the CEM on subsequent tests.

All three types of excitation were tested on the CEM, and sample results for the 3 types are given in the following paragraphs. The first type tested was sine wave excitations. The test involved disturbing the CEM with four thrusters for the first seven seconds of the experiment, then turning off the excitations and allowing the CEM's motions to freely decay for the remaining 23 seconds of the test. Figures 5a-h show the time histories of accelerometers #1-8, respectively, for this test. Note the open loop responses growing from 0 to 7 seconds, and the spikes in several time histories at 7 seconds, indicating when the thrusters were commanded off. The four thruster command time histories are shown in Figures 6a-d. The thruster sine wave commands were as follows: thruster #3 - amplitude of 2 lbs, frequency of 11.9381 rad/s; thruster #4 - amplitude of 0.9 lbs, frequency of 10.6814 rad/s; thruster #6 - amplitude of 2 lbs, frequency of 0.9111 rad/s; and thruster #7 - amplitude of 0.5 lbs, frequency of 0.9111 rad/s.

The next excitation test used single pulses to disturb the CEM. The same four thrusters used above for the sine wave excitations were used here. The pulse commands, shown in a composite plot in Figure 7, were as follows: thruster #3, 1 lbs at 5 seconds; thruster #4, 2 lbs at 10 seconds; thruster #6, -1 lbs at 15 seconds; and thruster #7, 0.5 lbs at 20 seconds. The total run time for this test was 30 seconds. Figures 8a and 8b show response time histories of accelerometers #7 and #8, respectively. The responses to the pulses can be seen on both accelerometer plots.

The final excitation type to be tested was random excitation. Thrusters #3 and #7 were commanded to produce outputs based on the following equation

$$z_k = a * (b*x_k + c)$$

where z_k was the kth sample thruster command output, in lbs, x_k was the kth sample discrete uniform random variable (between +/- 1.0), and a, b, c were scalar constants. The products of a and b, along with the variance of distribution of the x_k's, dictated the variance of the distribution of the z_k's, while the product of a and c dictated the mean of the distribution of the z_k's. For this test, the variables a and b were both set equal to 0.5, while the variable c was set to zero, for both thrusters, which corresponded to the random z_k's having a near zero mean distribution, since the x_k's also had a distribution with near zero mean. Figures 9a-b show the responses from accelerometers #7 and #8, respectively, to these inputs, while Figures 10a-b show the command time histories for thrusters #3 and #7, respectively; thruster #3 was on from 10 to 13 seconds, and thruster #7 was on from 5 to 7 seconds, both outputing +/- 0.25 lbs force in amplitude. The total run time of the test was 15 seconds.

Table 2 contains the mean and variance values for both the CCS computed and computer simulated random commands. Column 1 identifies the thruster pair which received the random commands, and columns 2 and 3 contain the mean and variance values, respectively.

Table 2. Mean and Variance of the open loop random thruster commands.

Thruster pair	Mean (lbs)	Variance (lbs^2)
#3 (CCS computed)	-0.001538	0.0062514
#7 (CCS computed)	0.001102	0.0069927
#3 (simulation)	0.000998	0.0066179
#7 (simulation)	0.005969	0.0076238

Although the statistical values between test and simulation were close, they did not match exactly. This may be attributed to the differences in the random variables, per time sample, between the EDS and the simulation.

During the open loop command testing phase, both the manual shutdown command and the automatic safety shutdown features of the CCS software were tested. Manual shutdown commands, issued by typing in "halt" on the CDPP, were successful in zeroing all the thruster commands and stopping the control experiment, in all instances. The automatic safety shutdown software keyed on the magnitude levels of the accelerometer signals. Each accelerometer was assigned a maximum allowable signal level, called the critical value; if any accelerometer signal magnitude exceeded its respective critical value during the test, all the thruster commands were automatically zeroed and the experiment was terminated. In order to test this automatic shutdown feature without exciting the CEM to a high (and potentially damaging) degree, artificially small critical values were assigned to the accelerometers. These levels were easily reached using the sine wave excitation commands mentioned above. Figure 11a shows the response time history of accelerometer #1, which was assigned a critical value of 0.1g. The plot shows that the 0.1g level was exceeded at 4.5 seconds, at which time the experiment automatically stopped and the thrusters were issued a zero command. Figure 11b shows the results of a similar test, where accelerometer #2's critical value was set to 0.1g; this experiment was stopped once this level was surpassed at 6.7 seconds. In both tests, messages indicating that a sensor limit was exceeded and the experiment terminated were correctly displayed on the GSET.

Once the open loop testing was satisfactorily completed, the CCS/RIU system was deemed ready for closed loop testing to begin.

Closed Loop Tests with the CEM

Confident that the sensor signals and actuator commands were being properly processed and transmitted between the CCS/RIU and the CEM, closed looped tests were started. Three different closed loop controllers, each a state feedback type involving accelerometers #1-8 and thrusters #1-8, but varying in the number of states, were executed on the CCS/RIU. The performance goal, of damping the vibrational motions of the CEM, was the same for all three controllers. Each test was 30 seconds long, and the same sine wave excitations which were described in the Open Loop Tests section were used to disturb the CEM for the first 7 seconds of each run. After a period of 3

seconds of free decay, the controller was then turned on and left on for the remainder of each test run. The results for each of the three tests are presented in the following paragraphs.

The first closed loop controller was a 16 state decoupled controller, digitally simulating second-order mass-spring-damper systems at sensor/actuator pair locations which actively absorb virbrational energy from the CEM[4]. This controller was executed at 150 Hz and at 200 Hz, the results of the latter test are presented here. For verification purposes, the same controller was executed on the existing SSRL VAX 3200 workstation at 200 Hz; this VAX is used as the primary real time control computer in the SSRL, and is tied into a Computer Automated Measurement and Control (CAMAC) rack which performs the data acquisition and conversion duties. Figures 12a-p show comparisons of the accelerometer response time histories from both the SSRL VAX and CCS/RIU tests. Each accelerometer's time histories, from both tests matched, although the accelerometer data from the CCS/RIU was noticeably more noisy. This was attributed to the fact that the CAMAC A/D converters had 16-bit precision, as opposed to 12-bit for the A/D converter in the RIU; the CAMAC A/D's have 16 times the resolution of the RIU A/D, the CAMAC having 3276 counts per volt representation versus the RIU's 204 counts per volt. This in turn led to the slight differences in thruster command time histories, as seen in Figures 13a-p, for the two tests. Another factor to be considered, when comparing the CCS/RIU to the SSRL VAX, is computational precision. The control law on the SSRL VAX was executed in double precision (i.e., 64 bits), while the CCS was limited to 32-bit precision in its computations in the AP. As a final check, the accelerometer time histories, from both tests, were fed through a PRO-MATLAB simulation of the 16 state decoupled controller. The resulting simulated thruster command time histories for the two tests matched their respective CCS/RIU and SSRL VAX computed thruster command time histories.

During the tests with the 16 state decoupled controller, the manual shutdown command from the CDPP was tested again, to ensure that it can function during an actual closed loop control test. The manual shutdown command was tried on several closed loop tests, always being issued after the controller was working. In each case, the halt command successfully zeroed out all of the thruster commands and terminated the control execution.

The second controller to be tested on the CCS/RIU was a 42 state H∞ controller. The controller was executed at 200 Hz, and the resulting accelerometer response and thruster command time histories can be seen in Figures 14a-h and in Figures 15a-h, respectively. The performance of this controller was considerably better than the 16 state decoupled controller above.

The final closed loop controller which tested was another H∞ controller, this time with 60 states. This controller was executed at 150 Hz and 200 Hz. The accelerometer response and thruster command time history plots can be seen in Figures 16a-h and in Figures 17a-h, respectively, for the 200 Hz test. It is obvious, from these plots, that the controller performance is poor, and a 7 Hz mode has been excited. This 7 Hz mode has also been encountered previously in control tests with the SSRL VAX. To circumvent this problem on the SSRL VAX, the controllers were executed at higher sampling rates, rates at which the present CCS/RIU is incapable of operating at. The sampling rate effect could be noticed when comparing the 150 Hz test results with the 200 Hz test results for this controller. Although the performance was poor in both tests, the 7 Hz instability was more pronounced in the 150 Hz test.

RIU Digital Filtering Tests

This section discusses the results of the RIU digital filtering tests which were performed. Analog low pass filters are also available in the RIU to provide signal anti-aliasing prior to digital filtering. The cutoff frequencies are automatically set by the selected RIU sampling rate, as shown in Table 3.

Table 3. RIU sampling rate and corresponding analog filter cutoff frequencies.

Sampling rate (Hz)	Cutoff frequency (Hz)
60	16.7
600	166.7
6000	1666.7

Although the analog filters were activated for the digital filtering tests, they were not tested by themselves .

As mentioned in the System Description section above, the RIU contains a DSP board for digitally filtering selected sensor signals prior to transmission to the CCS. Currently, the RIU has two pre-defined Finite Impulse Response (FIR) low pass filters which can be called by the user. The first is the so called "structures filter", which has a filter length of 110 (i.e., 109 states), was designed with a sharp roll off with little consideration given to phase shift. This filter will be referred as "filter #2", in this document. A "filter #1" does exist and is termed the "null filter", which simply means no digital filtering; this "null filter" must be defined since all sensor signals,

whether they are to be filtered or not, are sent to the DSP prior to transmission down the 1553B to the CCS. Figures 18a-c show the frequency response plots of filter #2, for the three selectable RIU sampling rates of 60, 600 and 6000 Hz, respectively. The second pre-defined filter has a filter length of 54 (53 states) and was designed to introduce smaller phase shift, for use with control law computations; hence, the name "control filter". For this document, this filter will be called "filter #3". Figures 19a-c show the frequency response plots of filter #3 for the RIU sampling rates of 60, 600 and 6000 Hz, respectively.

To test the RIU digital filters, the RIU input channels were disconnected from the CEM sensors and connected to a signal generator. Fixed-frequency sine waves were then sent to the RIU to mimic the sensor signals, as was done in the first part of the Dummy Control Computations tests. The same sine wave was sent to all eight RIU sensor channels, however, different RIU digital filters (using filters 1-3 described above) were selected for various channels. All the sensor channels were recorded on the CCS's GSET for later analysis. This post test analysis involved the comparison of the RIU digital filter outputs with PRO-MATLAB simulated filter outputs of the known input sine wave. Several tests were made, involving different frequency sine wave inputs; the results of three of these tests are presented here. In these cases, the RIU was set to sample at 600 Hz.

Figures 20a, 21a and 22a show time history plots of 0.1 Hz, 1.0 Hz and 8.0 Hz raw signal generator sine waves, respectively, compared to RIU filter #2's outputs. Note that the RIU outputs have been scaled by the dc filter gain of 0.749, to account for the magnitude of the digital filter. The phase shift became more pronounced at the higher signal frequencies. The group delay effects of the initialization of the digital filter was not recorded because the RIU begins to process the sensor signals in its DSP as soon as the RIU is fully configured, not when the CCS begins to record the data (time = 0 in the plots). There is a built-in five second delay between RIU software configuration and the start of data recording on the GSET.

Figures 20b, 21b and 22b show comparisons between the time history plots of RIU filter #2 outputs, and filter #2 PRO-MATLAB simulated outputs of 0.1 Hz, 1.0 Hz and 8.0 Hz sine wave inputs, respectively. The 0.1 Hz and 1.0 Hz tests show excellent agreement, however, there are larger differences between the filtered test data and simulated data for the 8.0 Hz case. This may be attributed to the differences between the actual raw 8.0 Hz signal, used in the actual test, and the "created" 8.0 Hz signal used in the corresponding PRO-MATLAB simulation. For all of these filter tests, the GSET-recorded raw test sine waves could not be used directly in the PRO-MATLAB simulations because of the slower sampling rates of the CCS. The RIU was sampling

the test sine waves at a rate of 600 Hz since the digital filters were designed for that rate. However, the CCS cannot operate at 600 Hz (see Appendix C) and was sampling and recording the test data at 150 Hz. Thus, in order to properly simulate the RIU digital filter outputs at 600 Hz, test sine wave signals, sampled at 600 Hz, had to be created in PRO-MATLAB. These created sine waves were based upon the measured raw test sine waves; the created sine waves were made to match the actual test sine waves in terms of frequency, amplitude and phase, but contained 4 times the number of sample points over a given period of time. In the 8.0 Hz case, the created 600 Hz sampled signal did not match the measured signal as well as in the 0.1 Hz and 1.0 Hz cases, which led to the slight differences in the filter test data and the PRO-MATLAB filtered data.

Figures 23a, 24a and 25a show time history plots of 0.1 Hz, 1.0 Hz and 8.0 Hz raw signal generator sine waves, respectively, compared to RIU filter #3's outputs. Note, again, that the RIU outputs have been scaled by the dc filter gain of 0.913, to account for the magnitude of digital filter #3. Also, it can be seen that the phase shift is much less for this filter. Figures 23b, 24b and 25b show comparisons between the time history plots of RIU filter #3 outputs, and filter #3 PRO-MATLAB simulated outputs of 0.1 Hz, 1.0 Hz and 8.0 Hz sine wave inputs, respectively.

One interesting point discovered during the digital filtering tests was that the output of RIU channel #1 was a factor of 1.023 higher than other RIU channels with the same outputs. This held true for all three frequency test cases, presented above. At present, there is no explanation of this.

RIU Standalone Tests

As previously mentioned, the RIU has the capability to execute control laws on its DSP with the CCS out of the loop, although it is possible for the EDS to initially excit the CEM with open loop commands. This is the so called "standalone" mode of the RIU. The RIU control laws take the form of transfer functions, i.e., in the form of digital Infinite Impulse Response (IIR) filters, for programming in the DSP; the coefficients are entered in on the GSET and transmitted to the RIU via a standard PC serial interface. These control law transfer functions must be designed for one of the three available RIU digital sampling rates - 60, 600 or 6000 Hz. Currently, the RIU control laws are limited both in order, and in the number of sensor inputs and actuator outputs which can be processed. Only three different control transfer functions, i.e., three different actuator/sensor pairs, can be specified with the present RIU.

With the above limitations in mind, an appropriate control law was choosen to test the RIU standalone mode. A six state decoupled controller, with three sensor inputs (accelerometers # 1, 3 and 8) and three thruster commands (thrusters # 1, 3 and 8) was selected. The orginal six state matrices were transformed into 3 separate second order, single input, single out transfer functions, using available routines in PRO-MATLAB; they were discretized at 600 Hz and are shown below:

$$\frac{thruster\#1}{accel.\#1} = \frac{2.4257*10^{-4}z^{-1} + 2.3344*10^{-4}z^{-2}}{1.0000 - 1.9940z^{-1} + 0.9943z^{-2}}$$

$$\frac{thruster\#3}{accel.\#3} = \frac{-3.0964*10^{-4}z^{-1} + 2.9472*10^{-4}z^{-2}}{1.0000 - 1.9924z^{-1} + 0.9927z^{-2}}$$

$$\frac{thruster\#8}{accel.\#8} = \frac{-2.3730*10^{-3}z^{-1} + 2.3623*10^{-3}z^{-2}}{1.0000 - 1.9930z^{-1} + 0.9930z^{-2}}$$

Transfer functions of this control law, digitized for execution at 200 Hz, were previously verified in successful closed loop tests on the SSRL VAX 3200.

The above transfer functions were programmed into the DSP onboard the RIU with the GSET via a RS 232 interface; for the RIU standalone tests, the only component of the CCS used was the GSET, all the rest were turned off. Once the RIU was executing in standalone mode, the CEM was manually excited to see if the control law could control the CEM. A problem with this particular control law was encountered in the RIU, in repeated testing, the thrusters never fired. Subsequent tests, with the RIU actuator command signals being monitored on an oscilloscope, revealed that the RIU computed actuator values were always zero. Although no direct cause of the problem has been discovered, the problem has been attributed to the small magnitudes of the numerator coefficients, which presented numerical difficulties for the RIU.

Other RIU standalone tests, involving other transfer functions programmed in the DSP, have been successfully tested. These tests used the pre-defined digital FIR filters available in the RIU, programmed as transfer functions for 3 sensor/actuator pairs.

Development problems and recommendations

This section outlines the problems encountered during the development of the CCS/RIU system, and some of the solutions which had to be implemented to make the CCS/RIU function as effectively as possible. Both software and hardware problems reported here are categorized as either being in the CCS (i.e, in one of its components), or in the RIU; they were as follows:

CCS Problems:

PROBLEM #1 - How and where to store the real time experimental data.

SOLUTION - The initial plan called for using the existing HRM I/O interface of the GSE and storing the data on the 9 track magnetic tape. The IEEE 488 interface would then be used to transfer the test data to a PC for post test analysis. However, this would have entailed writing additional complicated software which, in turn, would have delayed the delivery time of the CCS. This plan was dropped in favor of simply using the GSET to capture the test data directly off of the 1553B bus and storing the data onto its hard disk. The hard disk had over 25 megabytes of unused disk space which was ample to hold data sets from multiple test runs. This efficient method was further enhanced by switching the GSET from Remote Terminal mode, in which it would "talk" to the 1553B bus to Bus Monitor mode, where the GSET would just "listen" and record all data transmissions off the 1553B bus. This doubled the speed of real time data recording.

PROBLEM #2 - The 1553B interface card in the GSET PC had a tendency of misreading the data transmissions off of the 1553 bus, which resulted in either single data words (single actuator or single sensor values), or entire data transactions (all actuator or sensor values) associated with a time sync not being recorded properly. Fortunately, these data drop outs were rare; on average, only 1-3 data recording errors occurred over a test run containing recorded data for some 5000 time syncs. However, the number of data recording errors which occurred in a test run tended to increase at the higher sampling rates, i.e., above 200 Hz.

SOLUTION - The problem's cause was attributed to the fact that the 1553B interface card in the GSET was of an old design from SCI, and its speed performance limitations were known. Neither extra funds nor time were available to procure a better 1553B card (SCI planned to market an improved 1553B interface card with better speed performance later in 1991). A post processing

software fix was introduced to help alleviate this problem, and worked as follows. After a test run was completed, the file containing the recorded data transactions was checked for data errors. Each data set associated with a time sync was compared with data sets of previous time syncs, and any large deviations in data indicated missing words or whole transactions. If any error was detected among the data of a given time sync, the software simply copied the appropriate transaction (be it sensor or actuator) from the previous time sync. At the end of this post processing, a file was made available to the user which listed the errors, their corresponding time tags and what data was corrected.

PROBLEM #3 - The 1553B interface card in the GSET PC also caused errors in the recorded time tags. This problem involved sudden jumps in the recorded time to some random value (sometimes forward in time, sometimes backwards), which then incremented normally for several seconds, then jumping back to the correct time.

SOLUTION - No satisfactorily solution was found for this problem. Fortunately, this problem occurred very rarely.

PROBLEM #4 - Testing in the FSGB Laboratory revealed a third problem involving data recording errors related to the 1553B interface in the GSET PC: Unlike the first two 1553B interface problems, whose existences did not come as a surprise because of the known limitations of the 1553B card design, this problem cropped up suddenly. The recorded test data (either sensors or actuators, and sometimes both) were corrupted by equally spaced spikes, the magnitude of these spikes were often much greater than the actual signals. Figure 26 shows a sample data history plot which illustrates these data spikes; this problem was given the name "fencing", because of the resemblance of the data spikes to boards in a fence. It should be noted that these spikes only existed in the data files stored in the GSET. Whenever these spikes manifested themselves in the GSET data, no spikes could be found in the corresponding sensor data coming from or actuator commands going to the RIU. This was confirmed with the PC monitoring the sensor data in the RIU and by observing the computed actuator commands on an oscilloscope. Thus, these spikes affected neither the control law computations in the EDS, nor the data transmissions to and from the RIU.

SOLUTION - The problem was traced to the 1553B card in the GSET PC. Personnel more familiar with the 1553B were consulted about this problem, and they suggested that the data spikes

may have come from the GSET, perhaps from a neighboring board or a bad PC power supply, or from an external source in the lab. The exact source of the spikes was never discovered, and thus no solution was ever found. After a week and a half from their first appearance, the spikes suddenly disappeared and have not been seen since. It should be noted that these spikes may return.

PROBLEM #5 - How to speed up the EDS in performing control law computations at speeds up to least 200 Hz. The main difficulty was in trying to speed up the data transfer in and out of the 1750A and the AP.

SOLUTION - A number of solutions were implemented, and the combination of these made it possible to not only meet the 200 Hz closed loop sampling rate goal, but to exceed it. They were as follows:

* Block data transfer commands for the 1750A CPU, written in assembly language, replaced the single transfer commands which were in place.

* Minimized the number of clock interfaces of the 1750A.

* Added software code which allowed the boards in the EDS to run concurrently.

* Improved the interrupts on the EDS internal bus and sped up the executive I/O processing for the 1750A.

* For state feedback control computations, a copy of the state vector was stored directly in the AP's memory. This eliminated the need to transfer the state vector in and out of the AP for every state vector update computation, and greatly sped up the total control law computations. In general, data transfers within the EDS were minimized as much as possible.

* All disturbance excitations were pre-calculated and stored in the EDS memory board for use at the appropriate times during the real time experiment.

* Several changes to the software requirements were made: the elimination of the requirement to display data graphically in real time, and the elimination of the requirement to digitally filter the sensor data in the EDS prior to its use the control computations. The digital filters could be incorporated with the actual control law computations, which would increase the order of the state vector and thus make more efficient use of the AP.

RIU Problems:

PROBLEM #6 - Spikes in the sensor data were introduced by the RIU; the separate PC which monitored the sensor data sampled by the RIU prior to its transmission down the 1553B bus confirmed the RIU as the source. The spikes were few in number (typically no more than 3-5 spikes per sensor channel for a 20-30 second test run), but unlike the data spikes of the 1553B GSET "fencing" problem, these particular spikes were real and affected the control law computations of the actuator commands.

SOLUTION - It was discovered that certain terminal resistors on the RIU's backplane were loading down other chips on the same backplane. This caused the spikes. Once these resistors were removed, the RIU data spike problem was eliminated.

PROBLEM #7 - The RIU, when initially powered up, did not zero the outputs of its D/A converters, thus, some unknown non-zero signals would exist until the converters were reset to zero by the start of an experiment.

SOLUTION - Until the RIU was re-programmed to zero the D/A converters after power up, the actuator signals to the CEM were disabled from inside the Control Trailer in the SSRL until the first experiment was ready to be executed.

Recommendations:

The following general recommendations are suggested to improve the CCS/RIU system:

- Replace the 1553B bus with the 1773 fiber optic bus. The 1773 bus offers two major advantages over the current 1553B: greater effective bus length would be allowed, and faster data transmission rates (10 megabits per seconds versus the 1553B's 1 megabits per second). Minimal modifications would be required to make the current software compatible with the 1773 bus.

- Upgrade the existing GSET 286 PC to a 386, or higher, with more memory and hard disk space. This would allow post test data analysis to be performed on the GSET, and not have to ship the data to other computers.

- Add more AP boards into the EDS to allow for parallel computations in real time. More mass memory boards in the EDS would also be useful.

- Replace the current 1553B interface card in the GSET with the improved 1553B card from SCI. This should alleviate some of the data recording errors which occur with the present system.

- Expand current software to allow for more flexible programming. Currently, the only available control computations are state and output feedback with time invariant matrices. Also, more kinds of disturbance excitations, such as swept sine or user defined, should be added.

- Expand the RIU standalone capability. Currently, only 3 sensors and 3 actuators can be used in control laws executed in the RIU.

Summary

The CCS/RIU, a real time computer system based upon spaceflight qualified components, has been installed in the SSRL. Initial acceptance tests, which have included system hardware, computational software, open and closed loop tests with the CEM, RIU digital filtering and RIU standalone, have been passed satisfactorily. The open and closed loop tests, in particular, have demonstrated that the CCS/RIU system is capable of performing useful real time control experiments on actual laboratory test articles. Further improvements to the system, for laboratory use, in terms of faster computational speeds, an increase in the number of input channels, and

better support equipment in general are all possible. Also, these initial tests results have indicated that the EDS shows promise as a viable spaceflight computer, and further study in this direction is warranted.

References

1. SCI Systems, Inc., *MAST Final Report*, SCI Report No. P007-001A, Jun. 1990.

2. Borchardt, Jr., R. P., "Control Structures Interaction (CSI) Project Remote Interface Unit (RIU) MIL-STD-1553B Interface Description", Version C, Sept. 1990.

3. Belvin, W. K., Elliott, K. E., Bruner, A. M., Sulla, J. L., Bailey, J., "The LaRC Phase-0 Evolutionary Model Testbed: Design and Experimental Results", *Proceedings of the Fourth NASA/DoD Control/Structures Interaction Technology Conference*, WL-TR-91-3031, Jan. 1991, pp. 594-613.

4. Bruner, A. M., Belvin, W. K., Horta, L. G., Juang, J. N., "Active Vibration Absorber for the CSI Evolutionary Model: Design and Experimental Results", Presented at the AIAA 32nd Structures, Structural Dynamics & Materials Conference, Apr. 1991, Paper No. 91-1123.

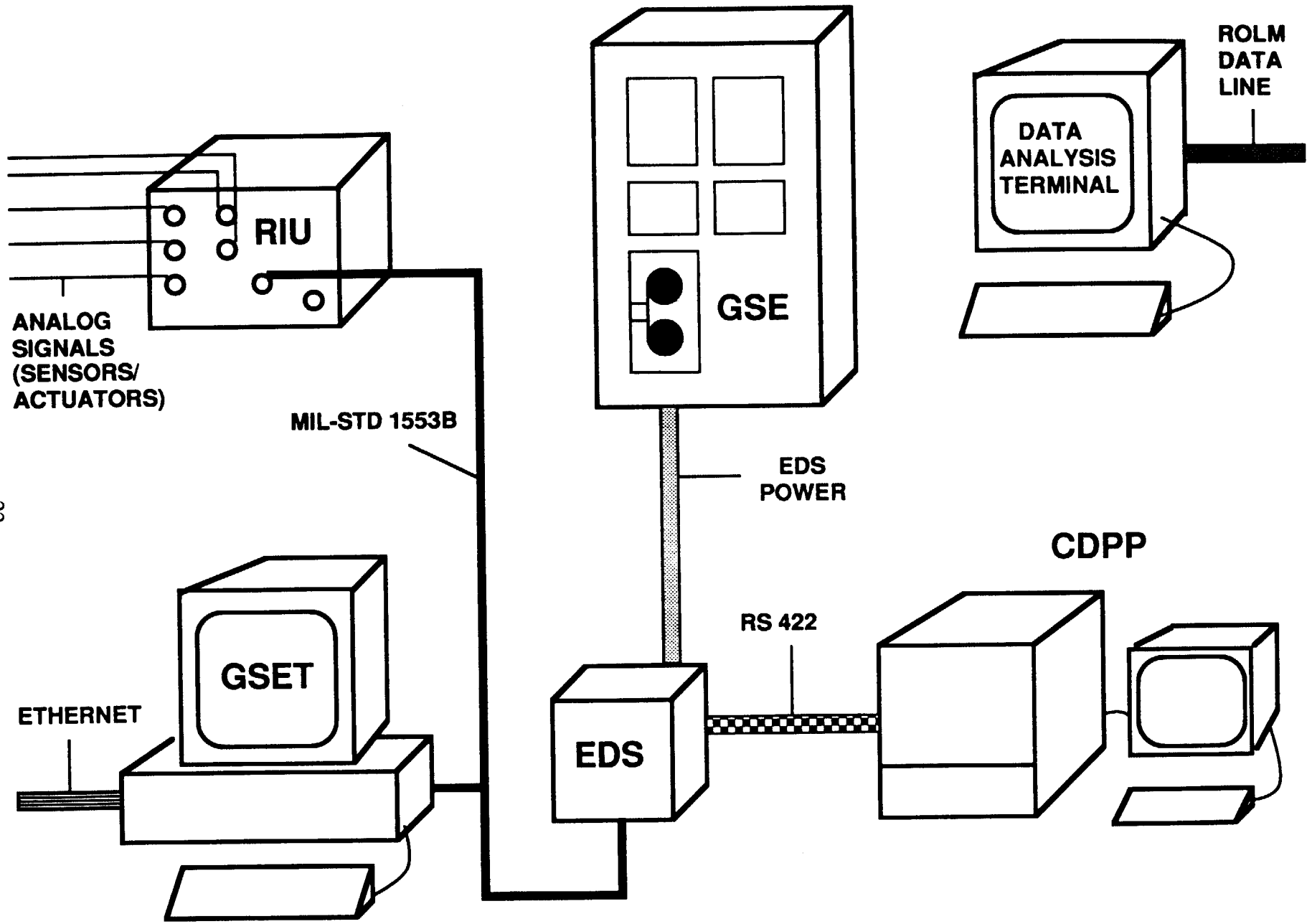


Figure 1. Schematic of CCS/RIU, showing the major components and connections.

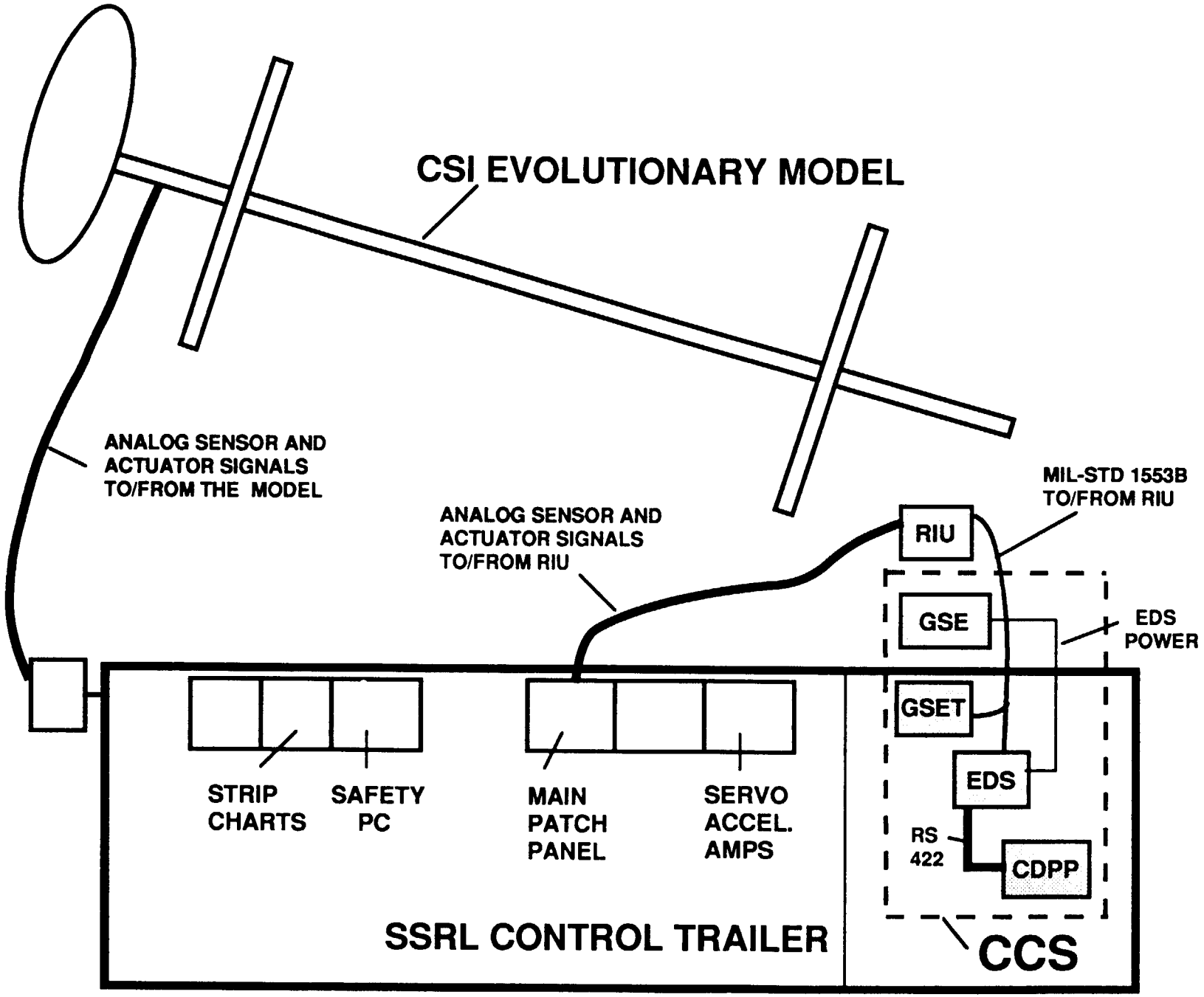


Figure 2. Schematic showing the CCS/RIU in the SSRL.

Figure 3a. Accelerometer #1 time history for "dummy" control computations test #1.

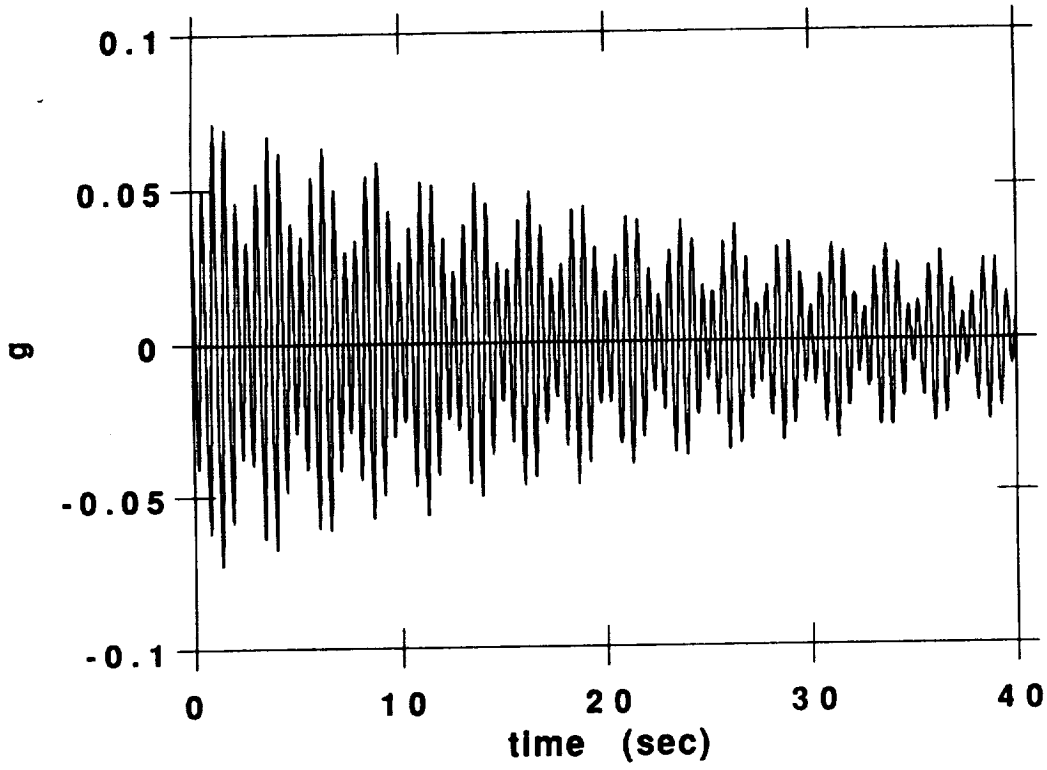


Figure 3b. Accelerometer #2 time history for "dummy" control computations test #1.

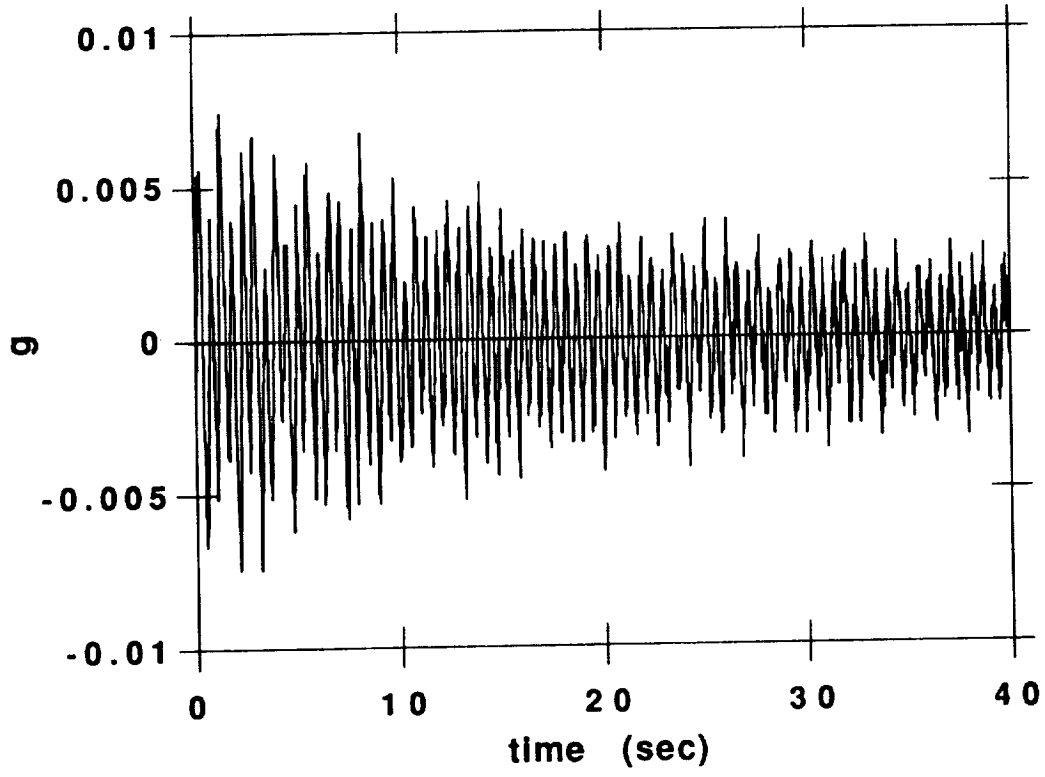


Figure 3c. Accelerometer #3 time history of "dummy" control computations test #1.

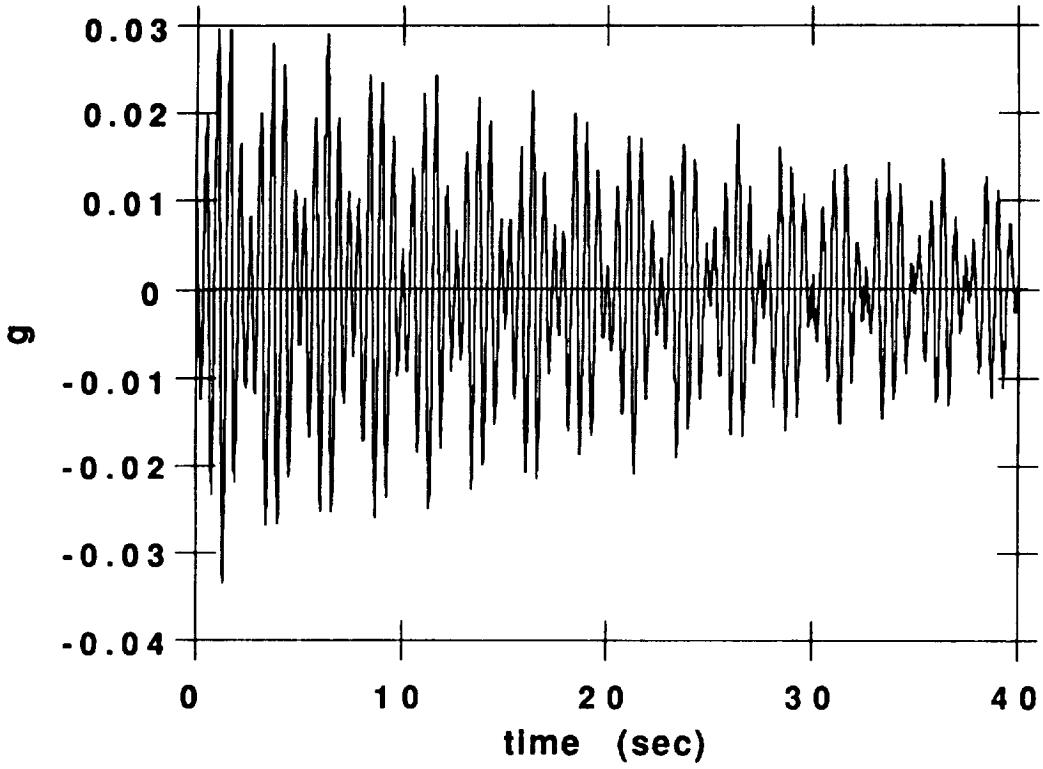


Figure 3d. Accelerometer #4 time history for "dummy" control computations test #1.

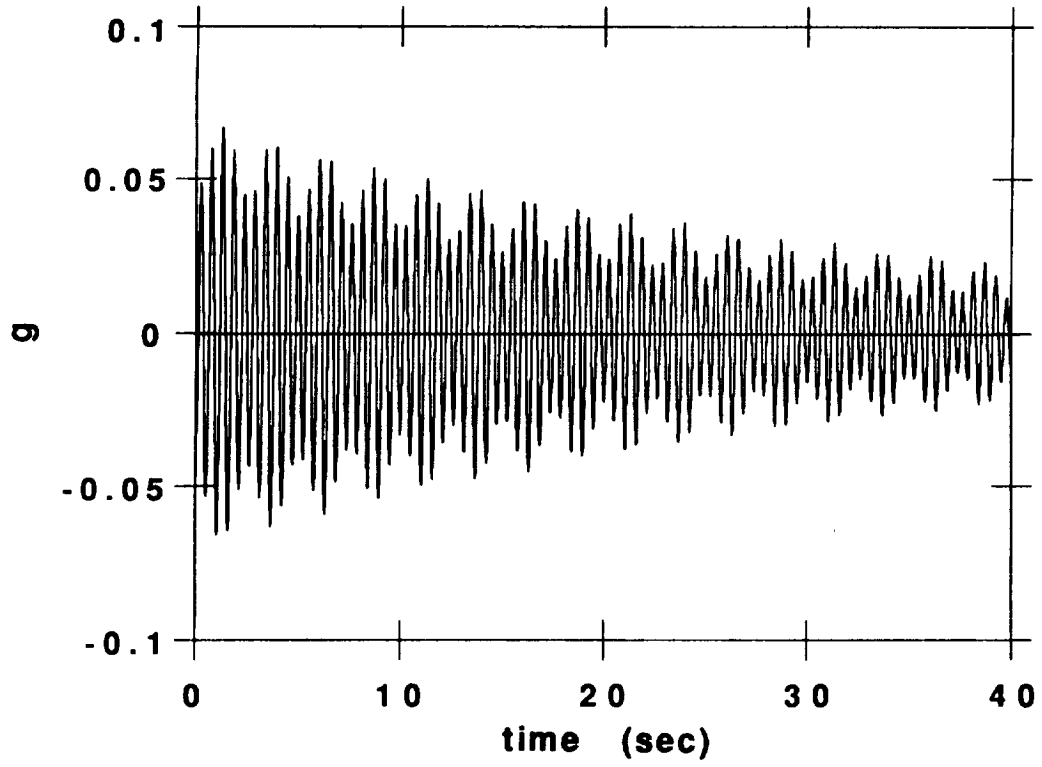


Figure 4a. Thruster #1 command time history for "dummy" control computations test #1, from CCS.

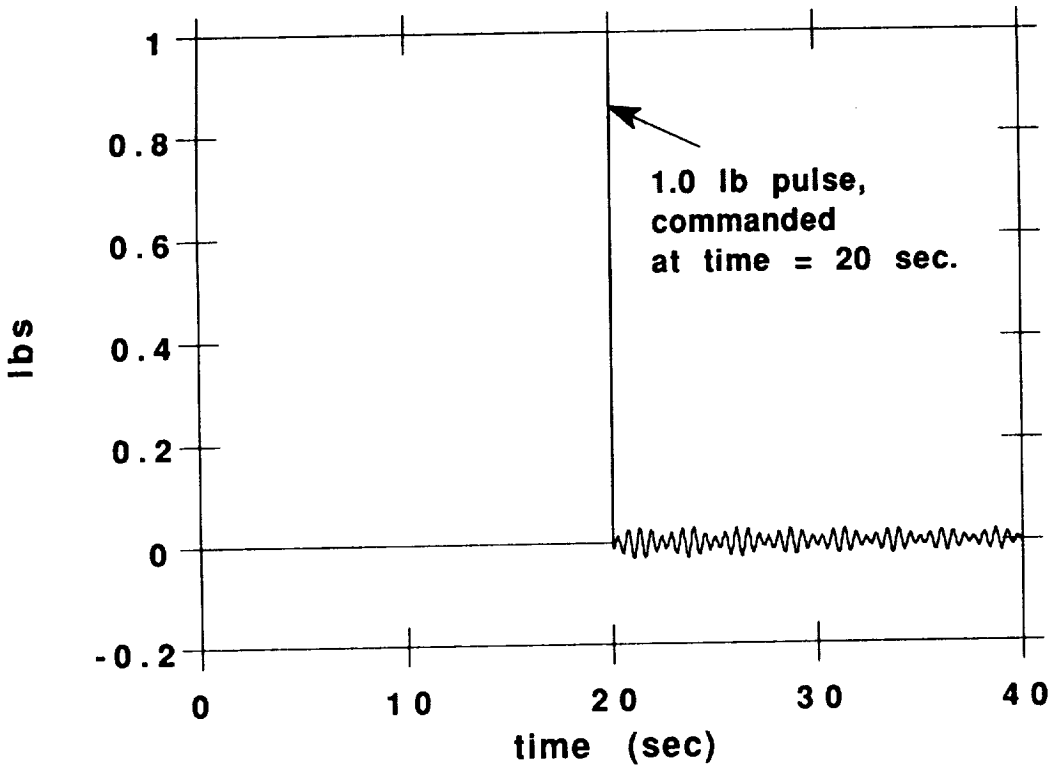


Figure 4b. Thruster #1 command time history for "dummy" control computations test #1, from simulation.

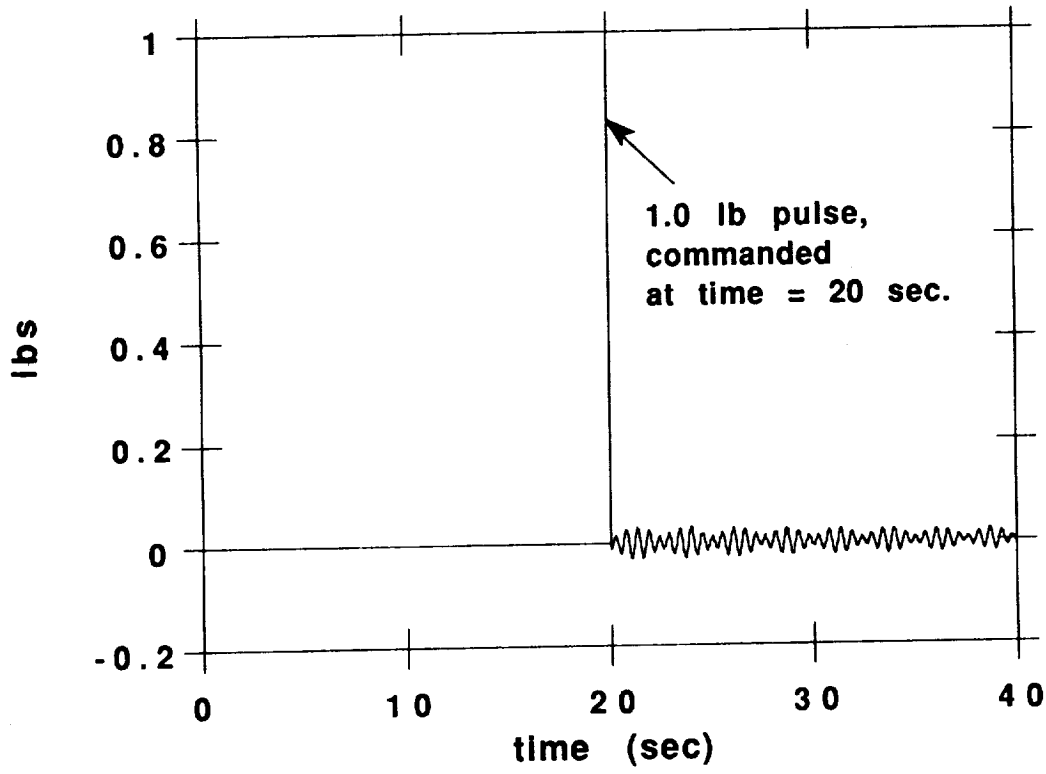


Figure 4c. Thruster #2 command time history for "dummy" control computations test #1, from CCS.

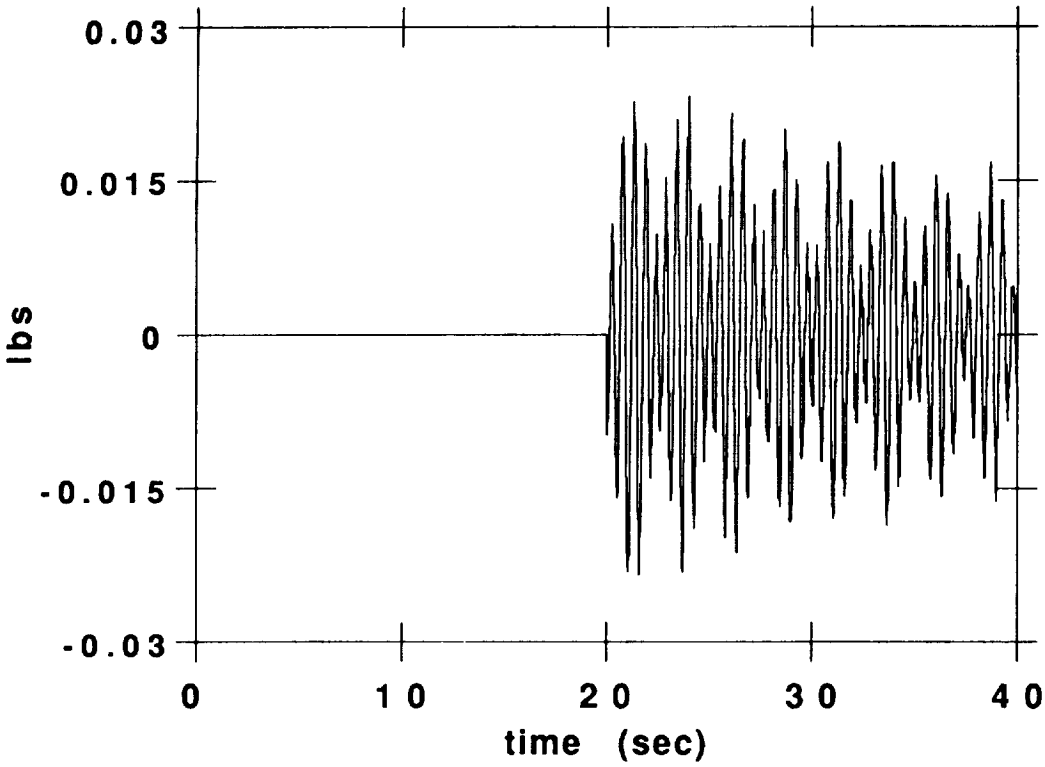


Figure 4d. Thruster #2 command time history for "dummy" control computations test #1, from simulation.

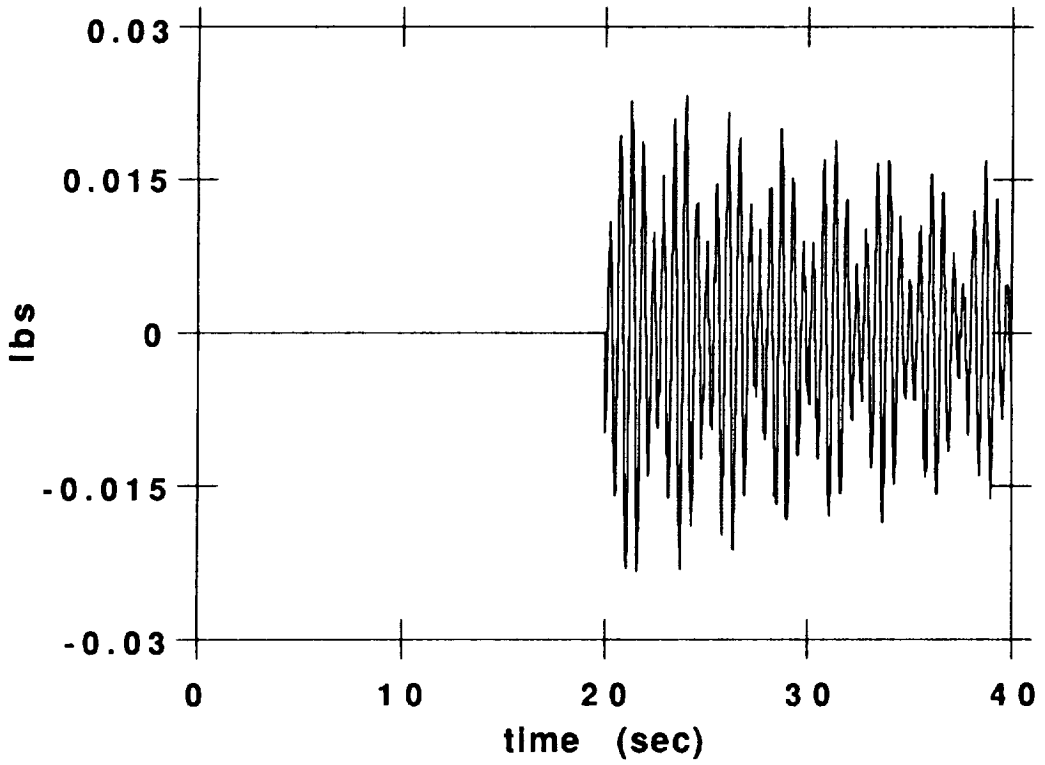


Figure 4e. Thruster #3 command time history for "dummy" control computations test #1, from CCS.

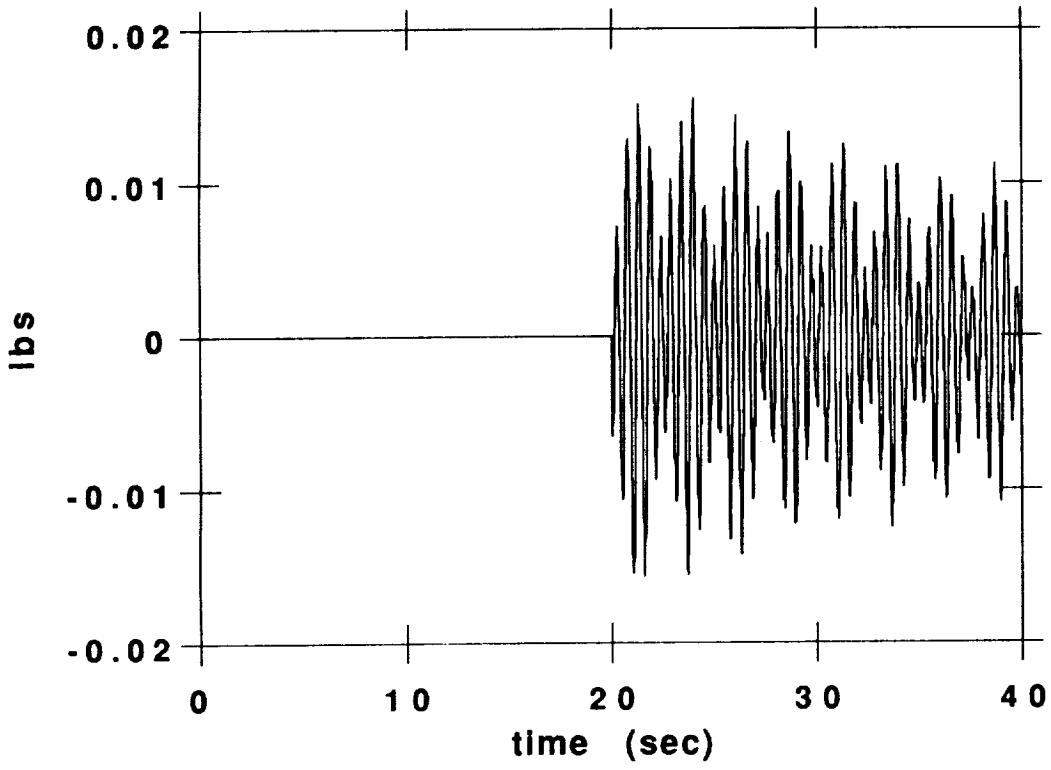


Figure 4f. Thruster #3 command time history for "dummy" control computations test #1, from simulation.

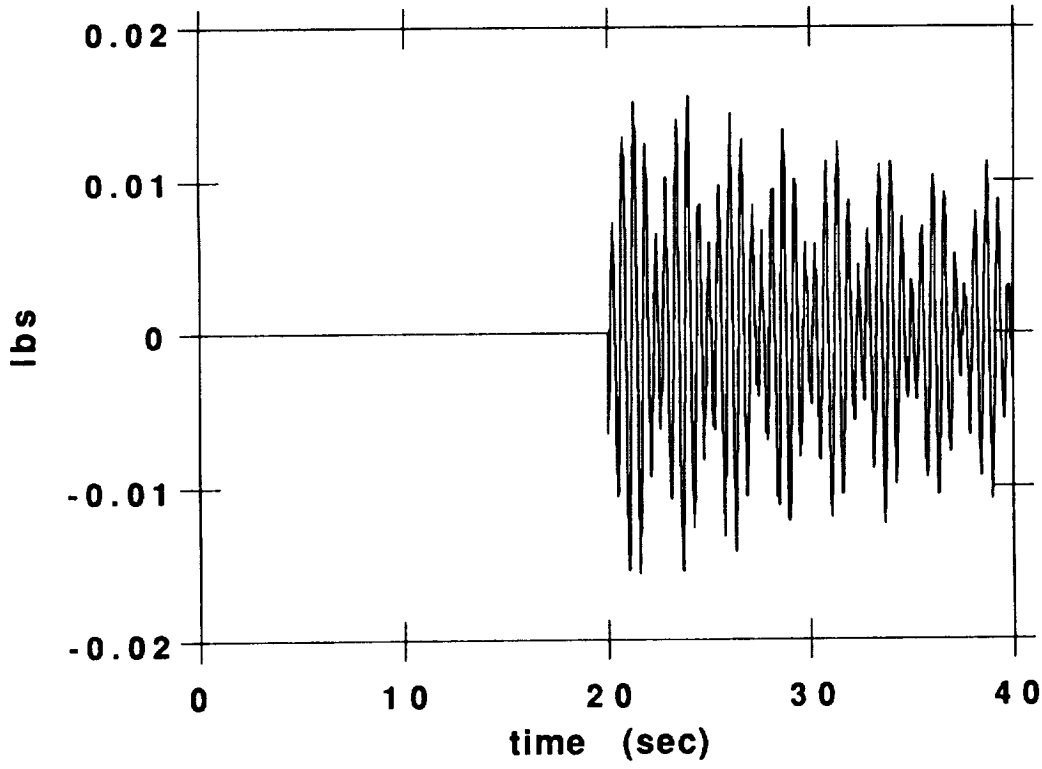


Figure 4g. Thruster #4 command time history for "dummy" control computations test #1, from CCS.

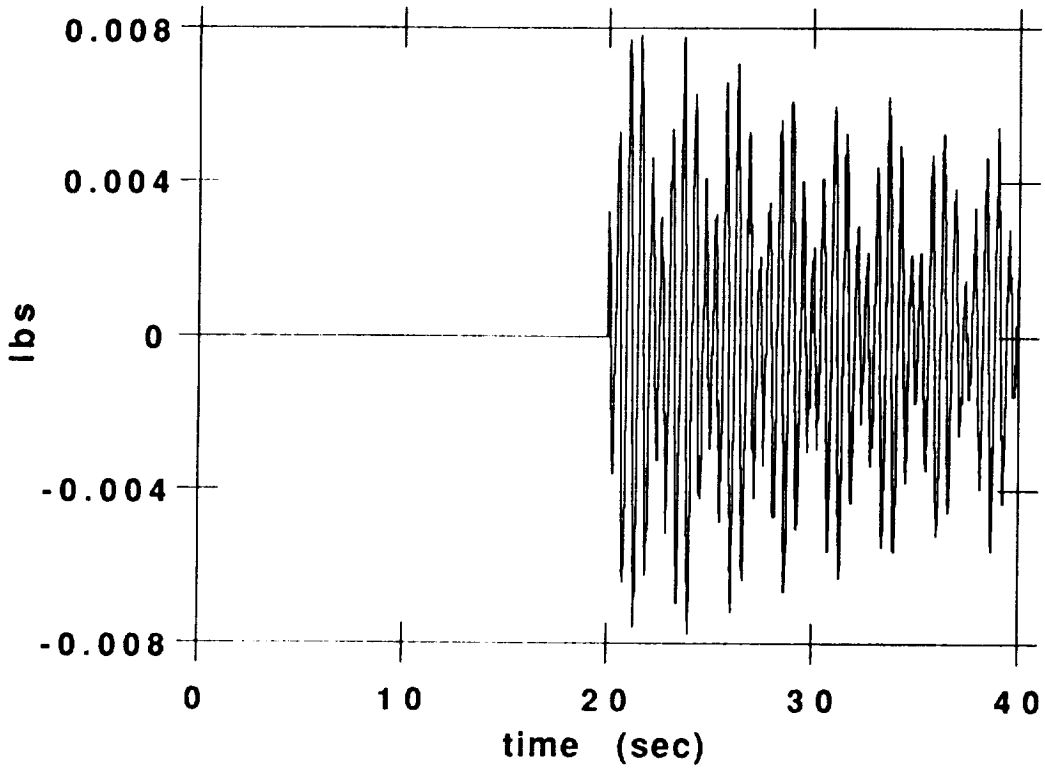


Figure 4h. Thruster #4 command time history for "dummy" control computations test #1, from simulation.

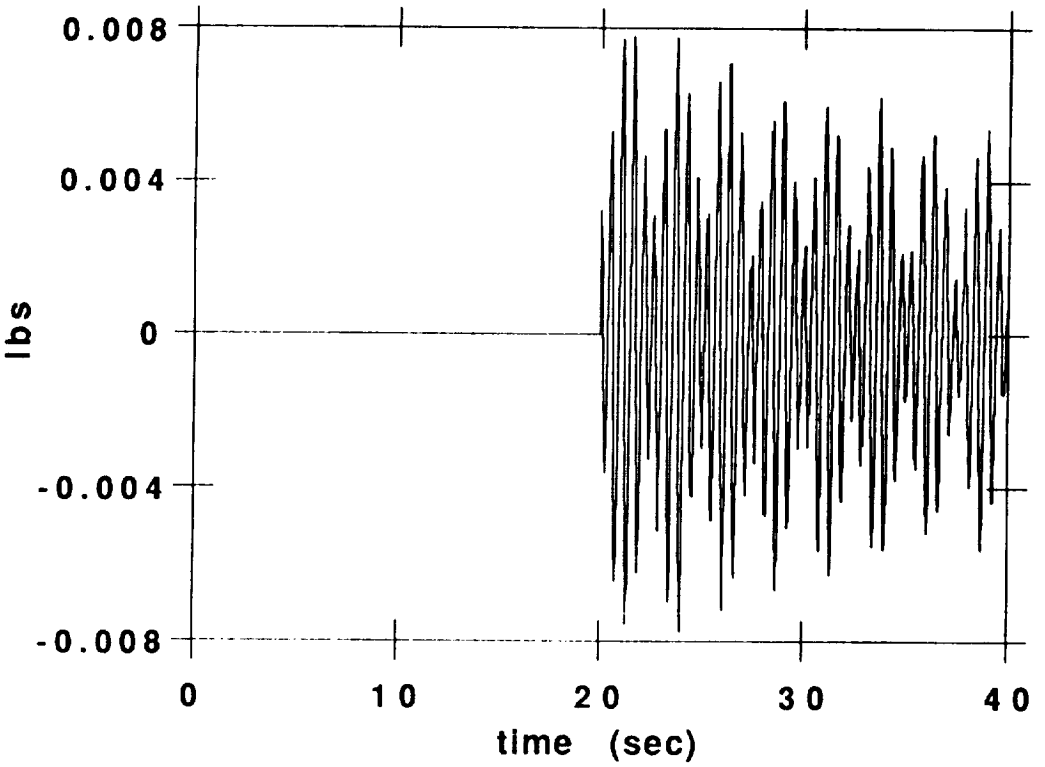


Figure 4i. Thruster #5 command time history for "dummy" control computations test #1, from CCS.

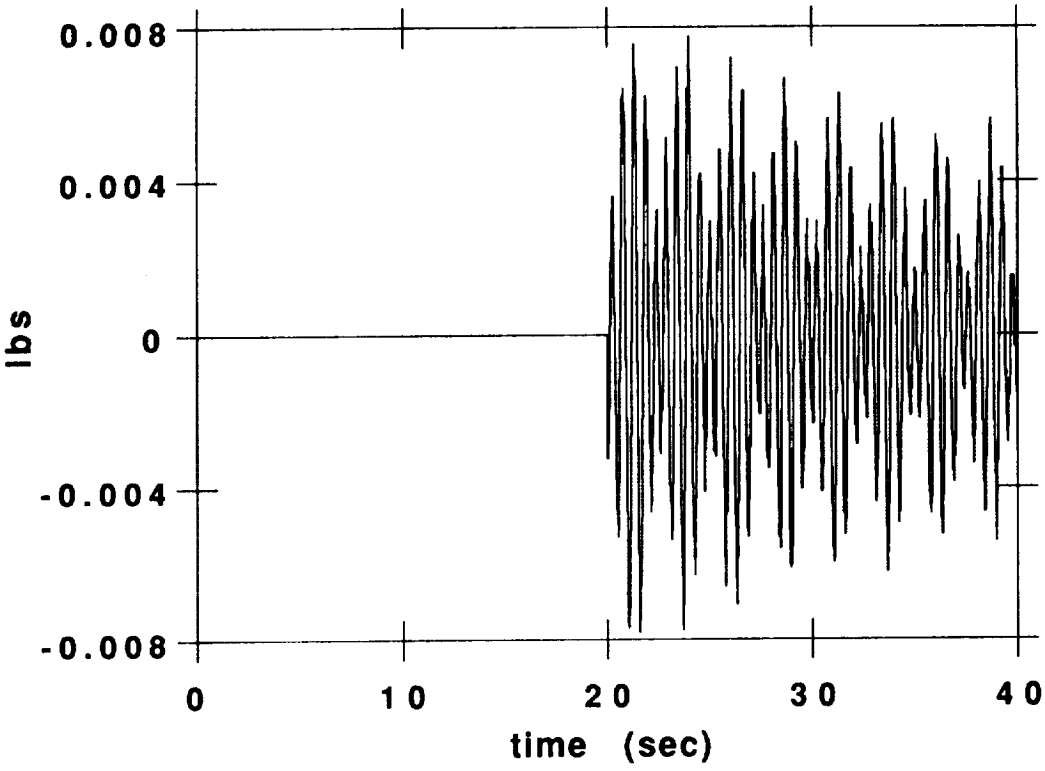


Figure 4j. Thruster #5 command time history for "dummy" control computations test #1, from simulation.

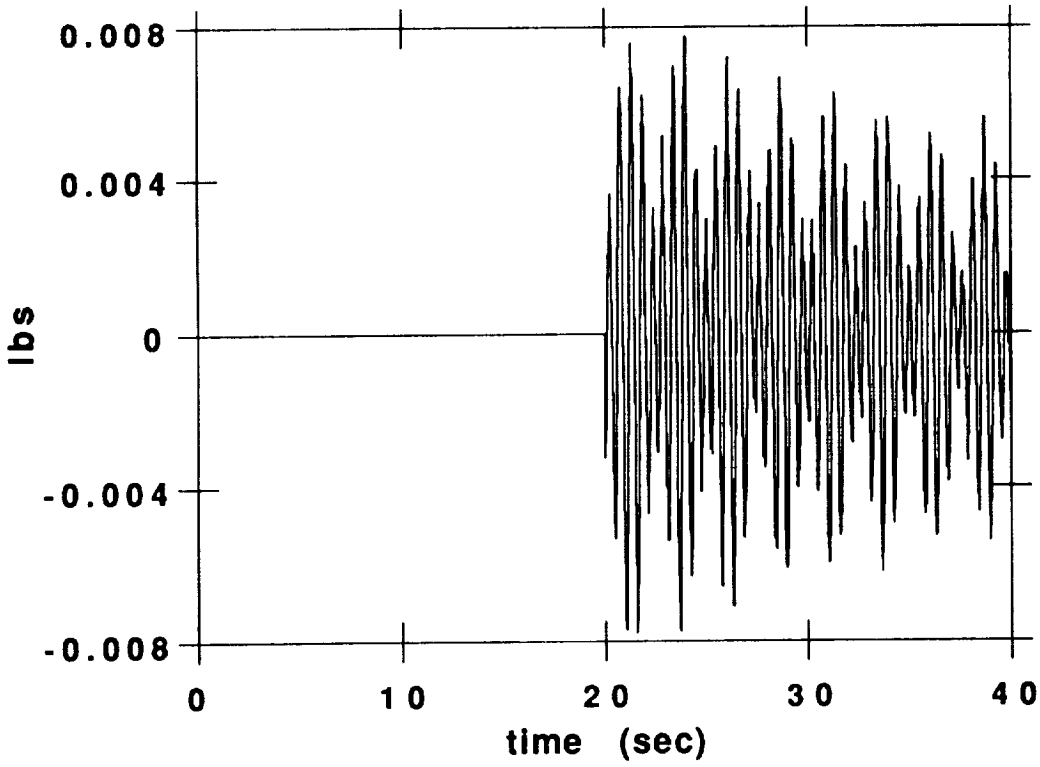


Figure 4k. Thruster #6 command time history for "dummy" control computations test #1, from CCS.

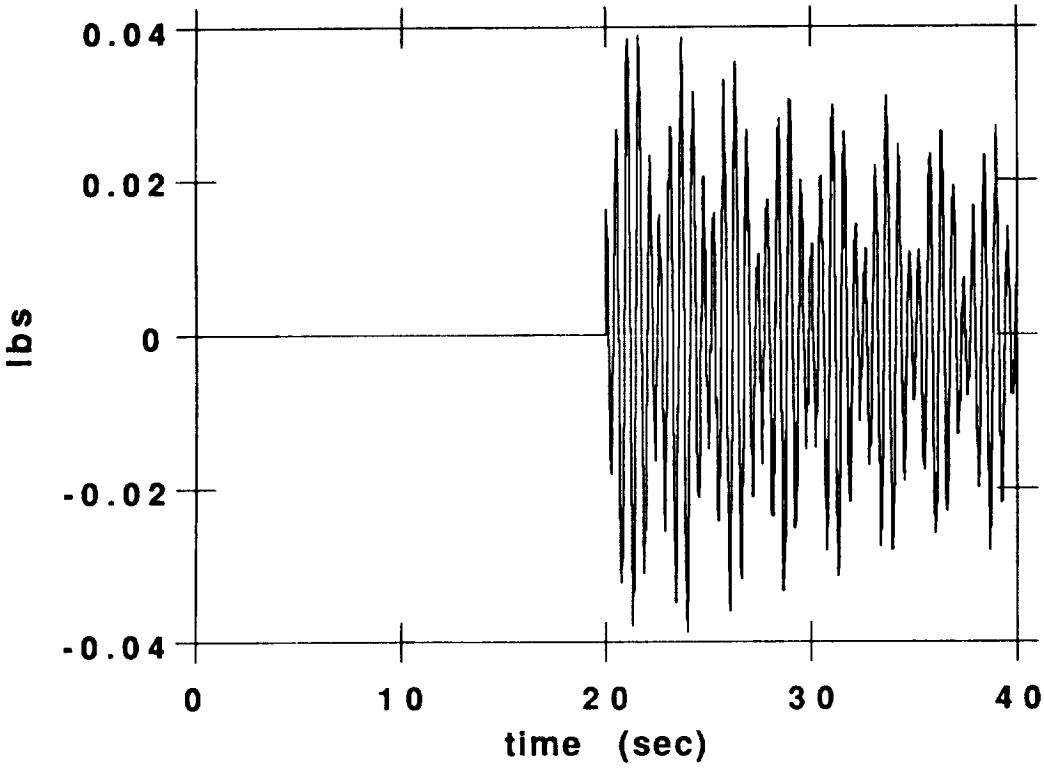


Figure 4l. Thruster #6 command time history for "dummy" control computations test #1, from simulation.

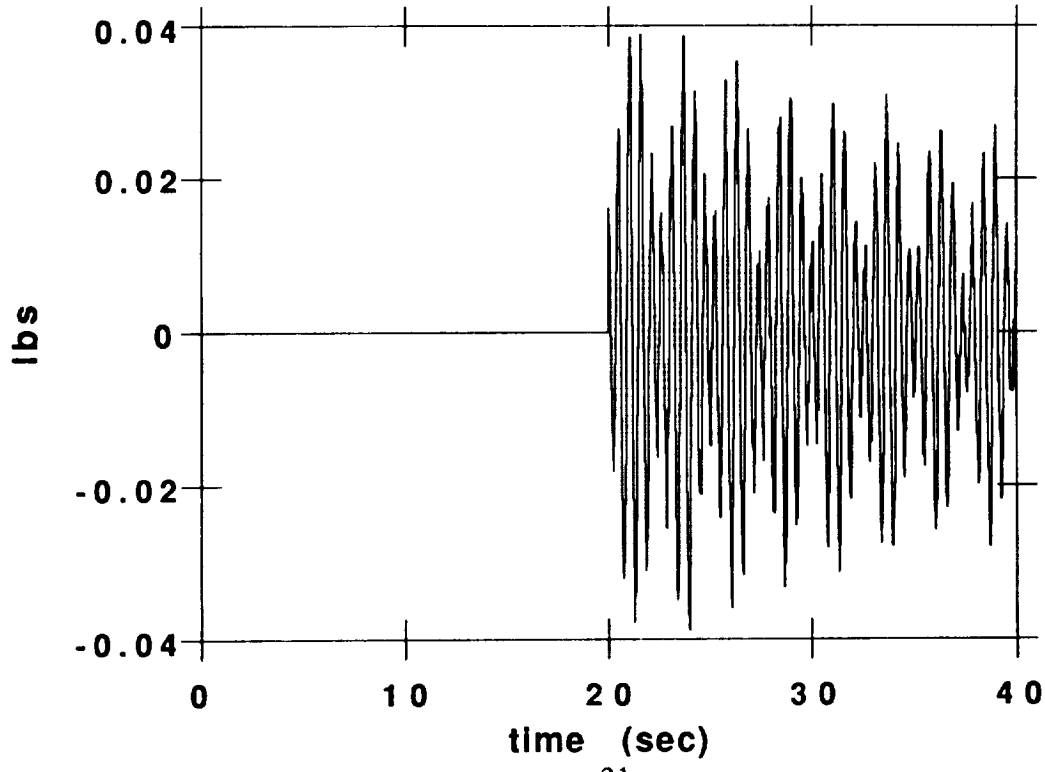


Figure 4m. Thruster #7 command time history for "dummy" control computations test #1, from CCS.

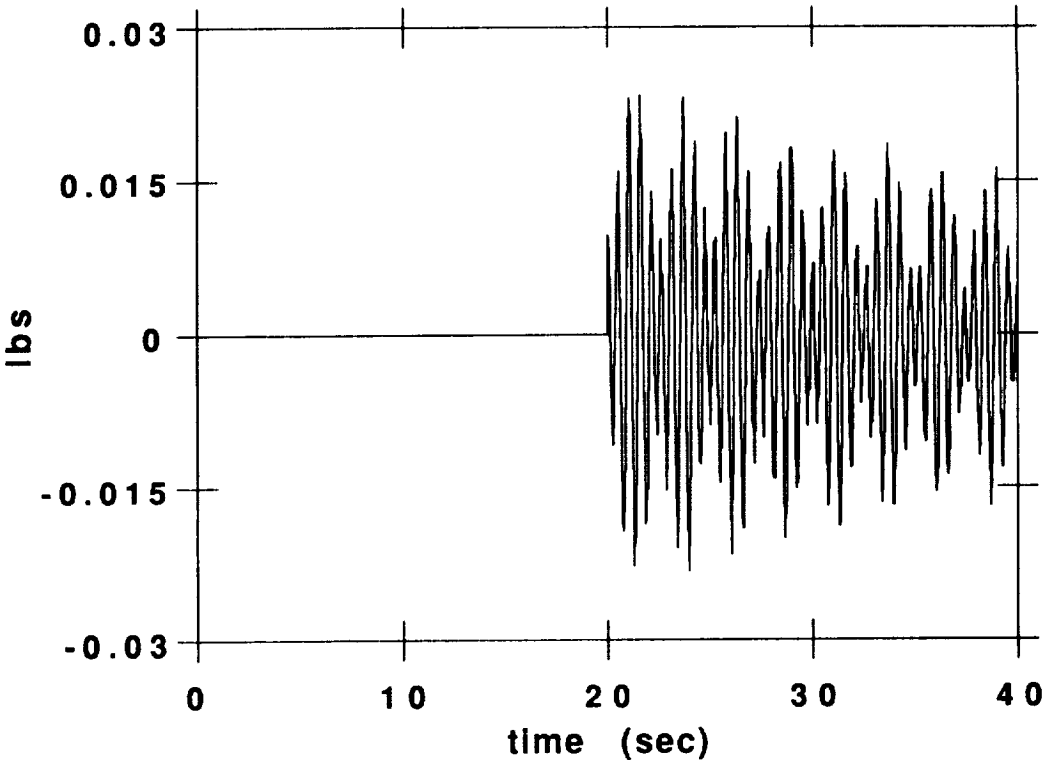


Figure 4n. Thruster #7 command time history for "dummy" control computations test #1, from simulation.

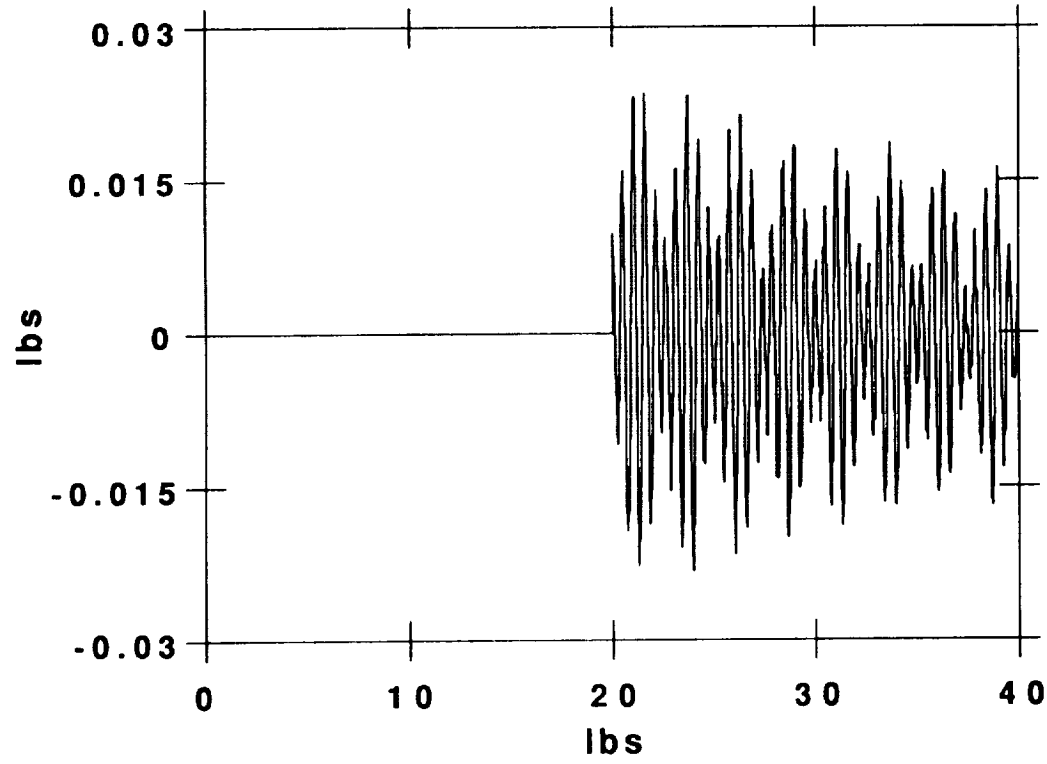


Figure 4o. Thruster #8 command time history for "dummy" control computations test #1, from CCS.

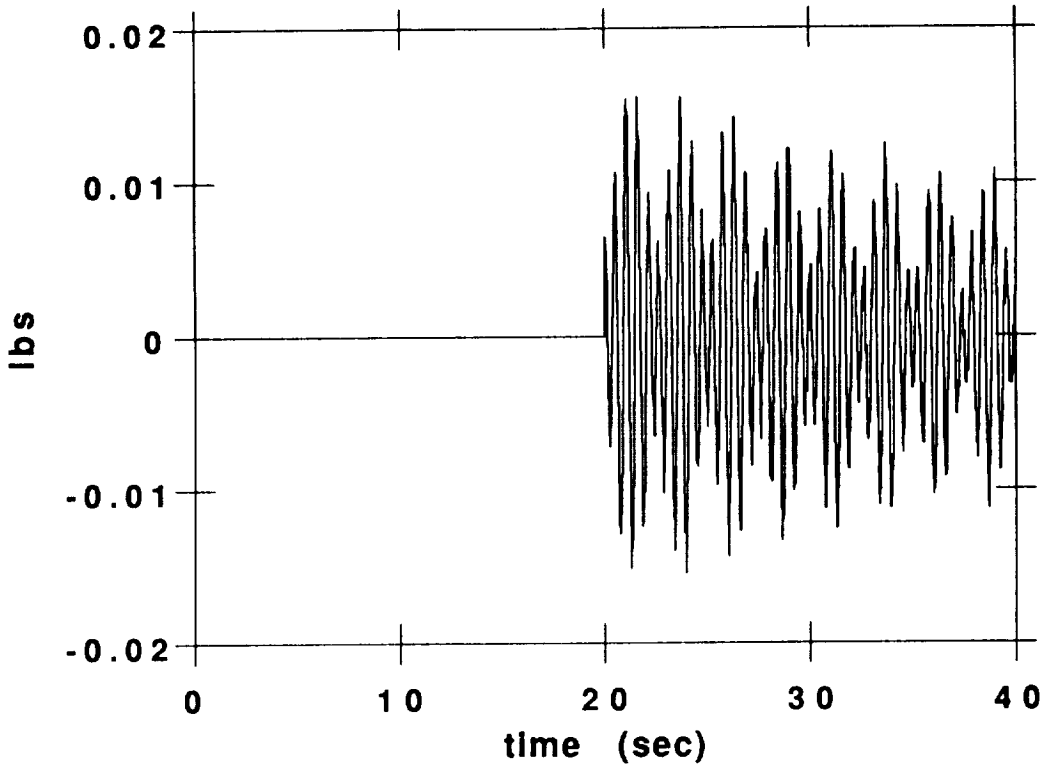


Figure 4p. Thruster #8 command time history for "dummy" control computations test #1, from simulation.

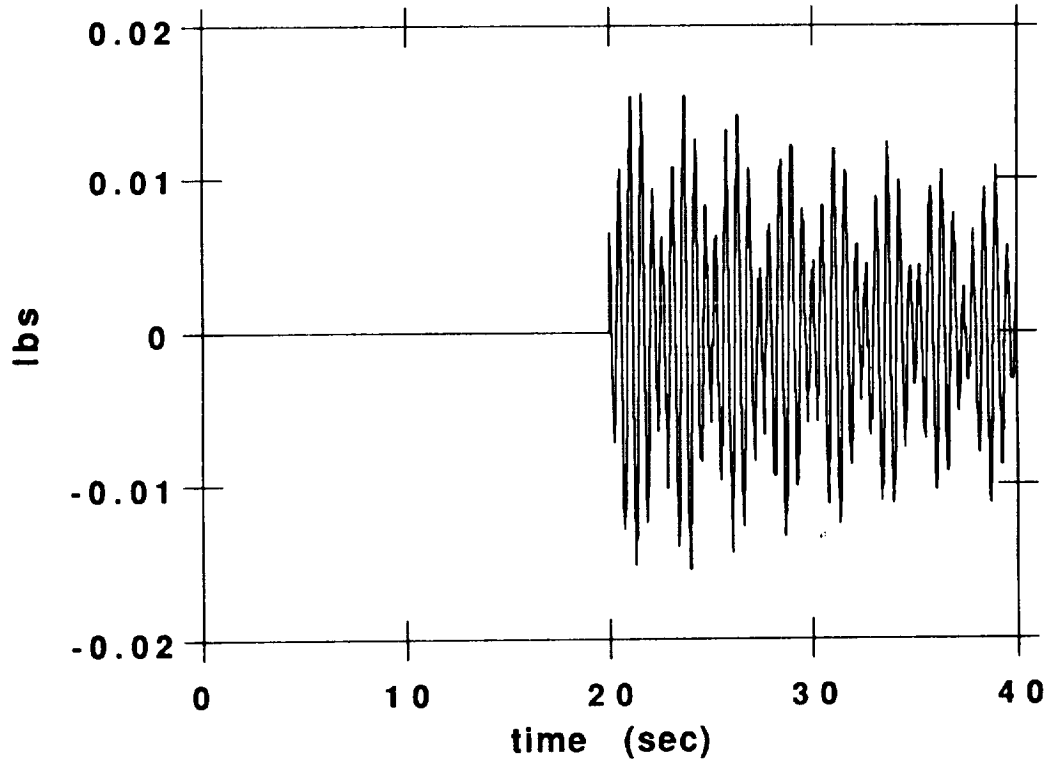


Figure 5a. Accelerometer #1 time history for open loop sine wave excitation test.

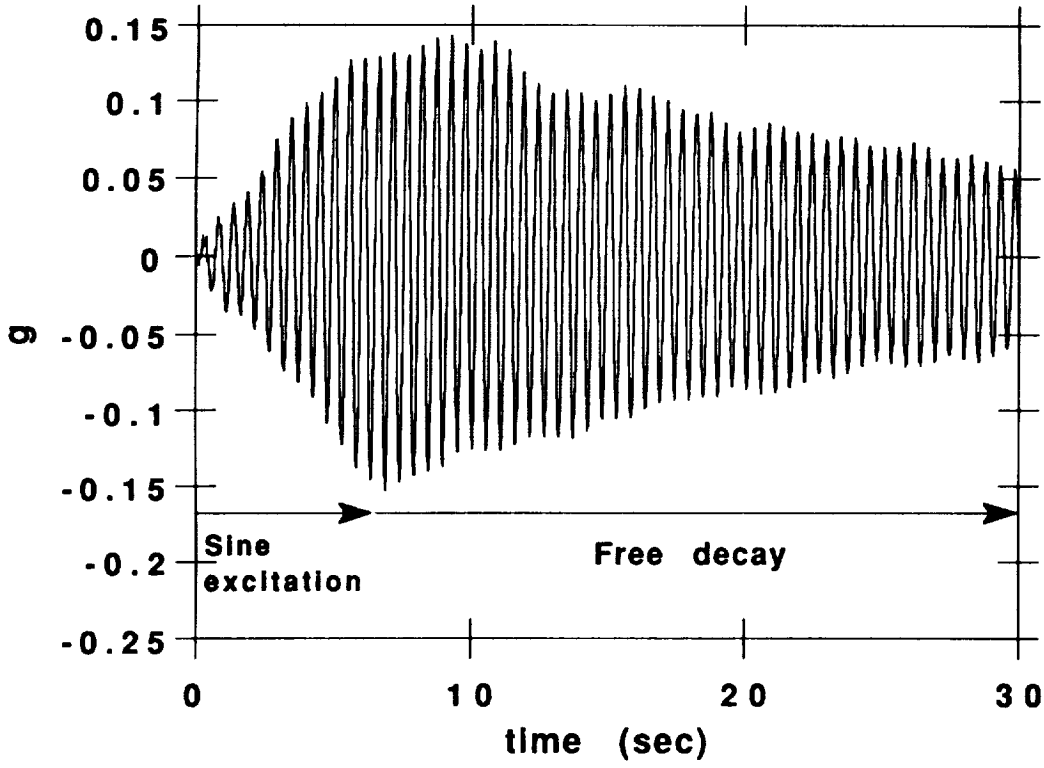


Figure 5b. Accelerometer #2 time history for open loop sine wave excitation test.

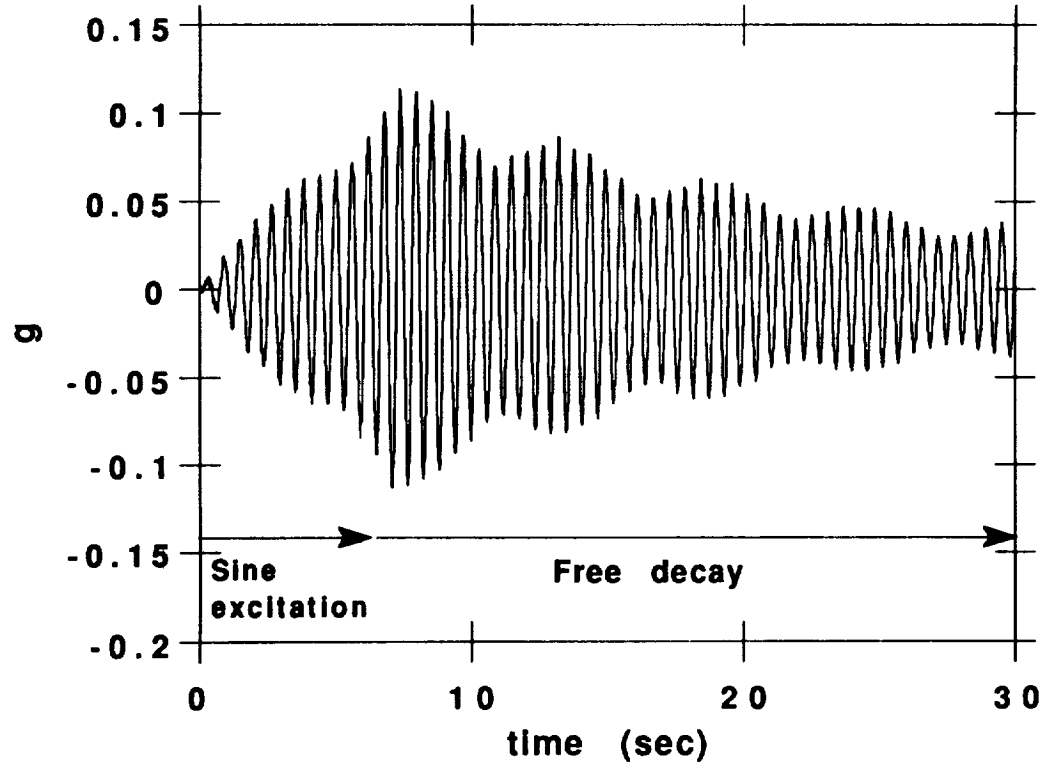


Figure 5c. Accelerometer #3 time history for open loop sine wave excitation test.

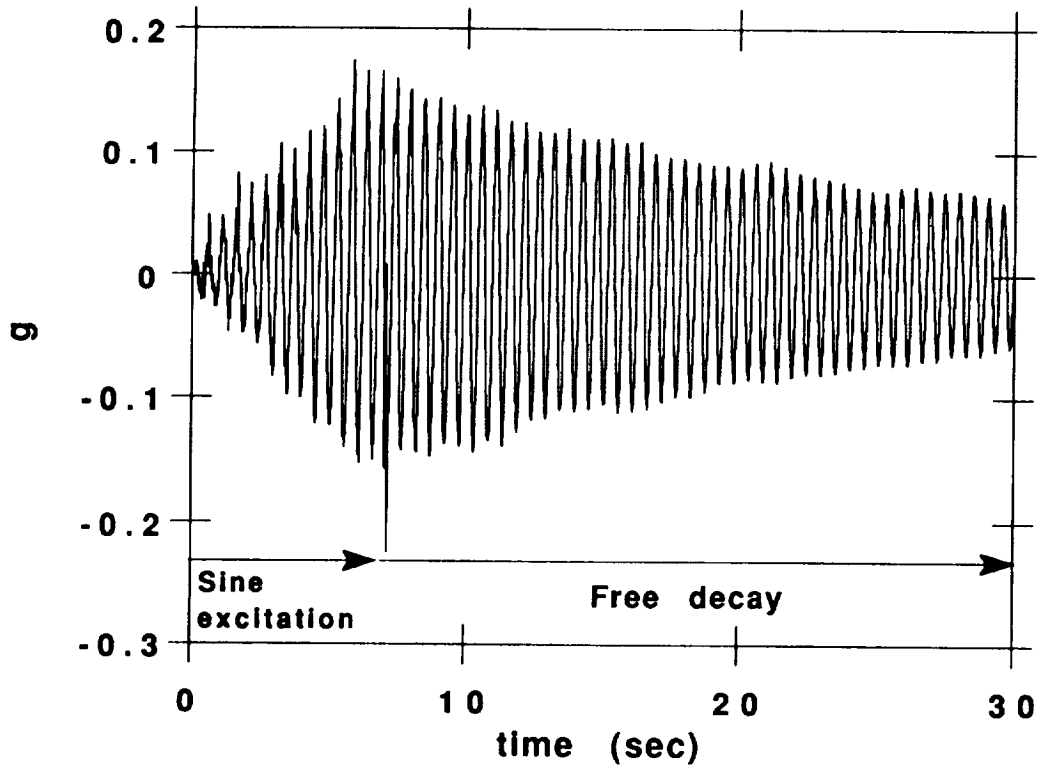


Figure 5d. Accelerometer #4 time history for open loop sine excitation test.

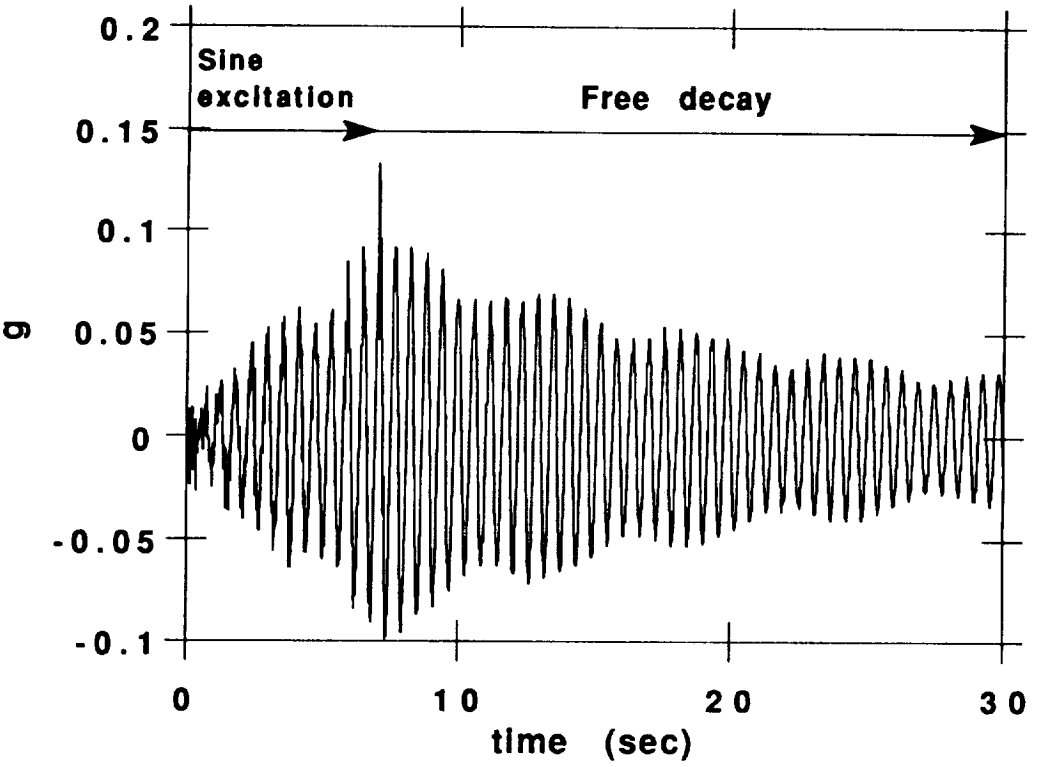


Figure 5e. Accelerometer #5 time history for open loop sine wave excitation test.

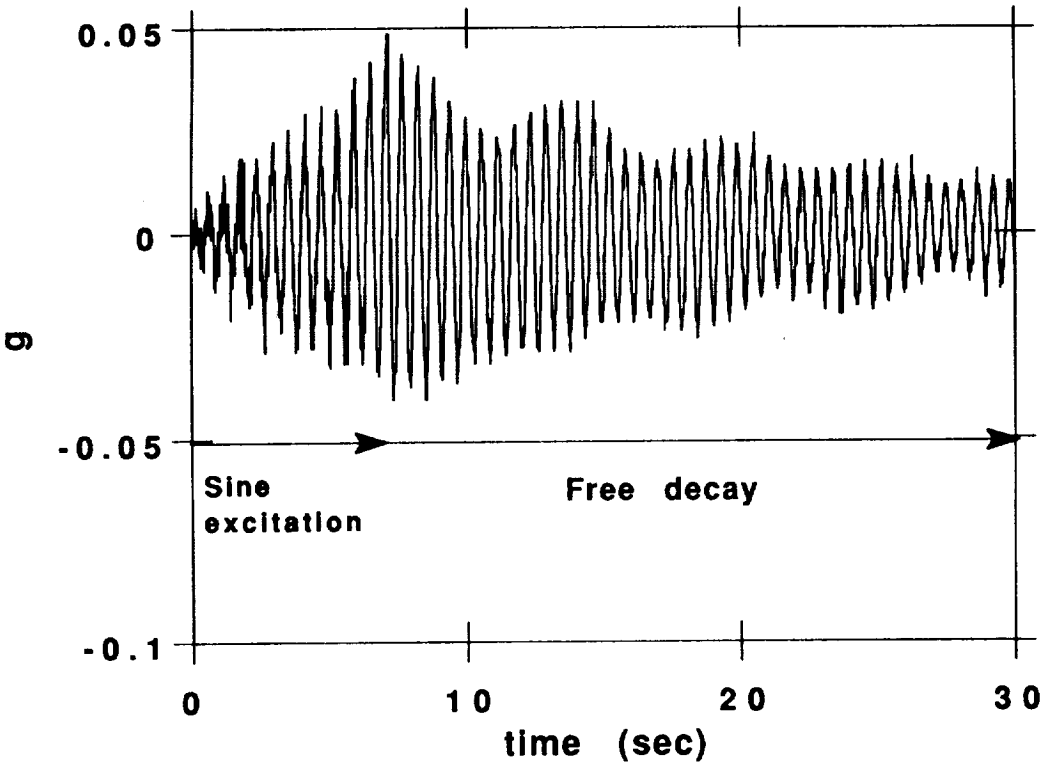


Figure 5f. Accelerometer #6 time history for open loop sine wave excitation test.

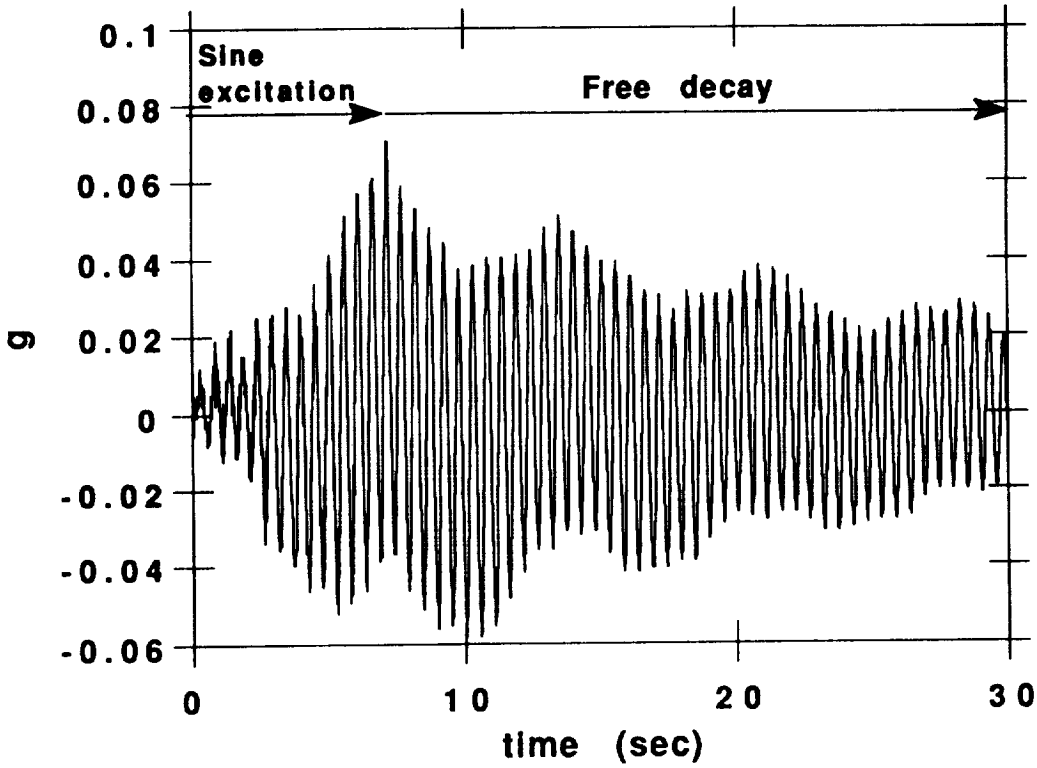


Figure 5g. Accelerometer #7 time history for open loop sine wave excitation test.

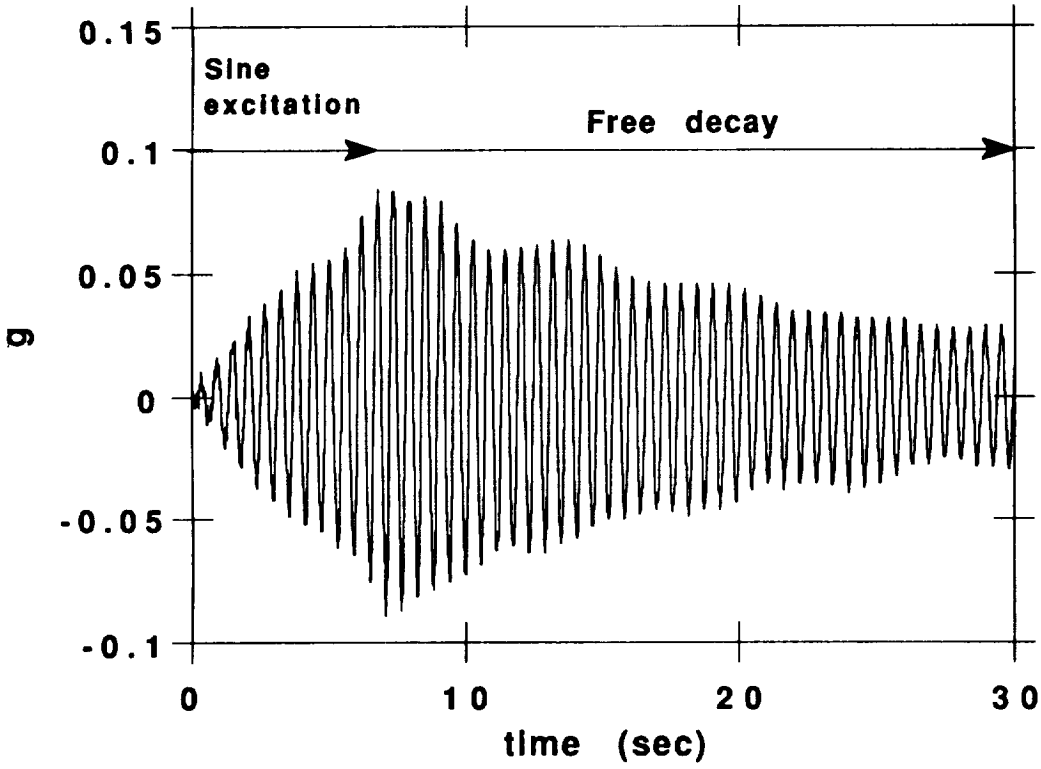


Figure 5h. Accelerometer #8 time history for open loop sine wave excitation test.

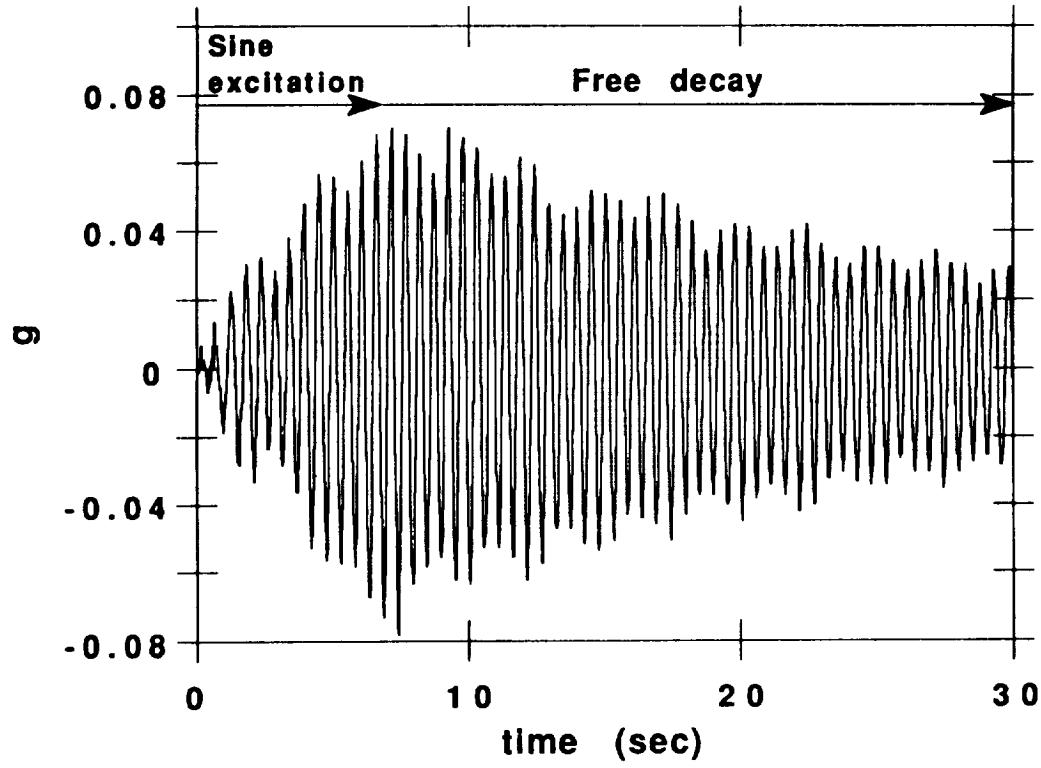


Figure 6a. Thruster #3 command time history for open loop sine wave excitation test.

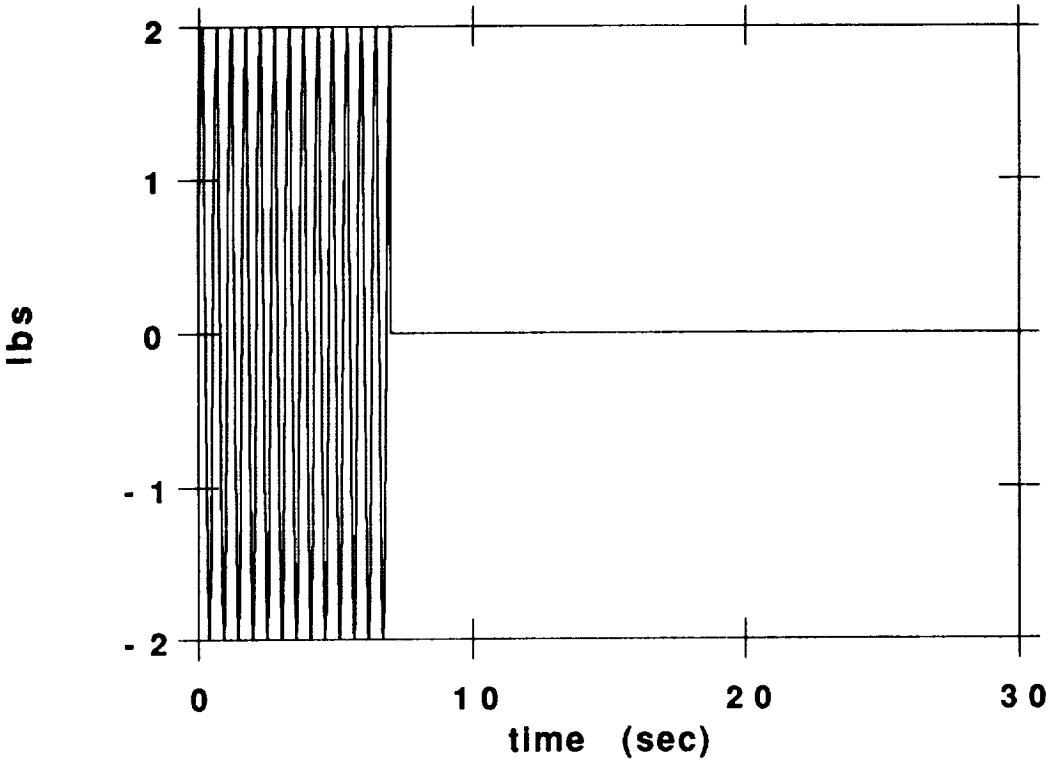


Figure 6b. Thruster #4 command time history for open loop sine excitation test.

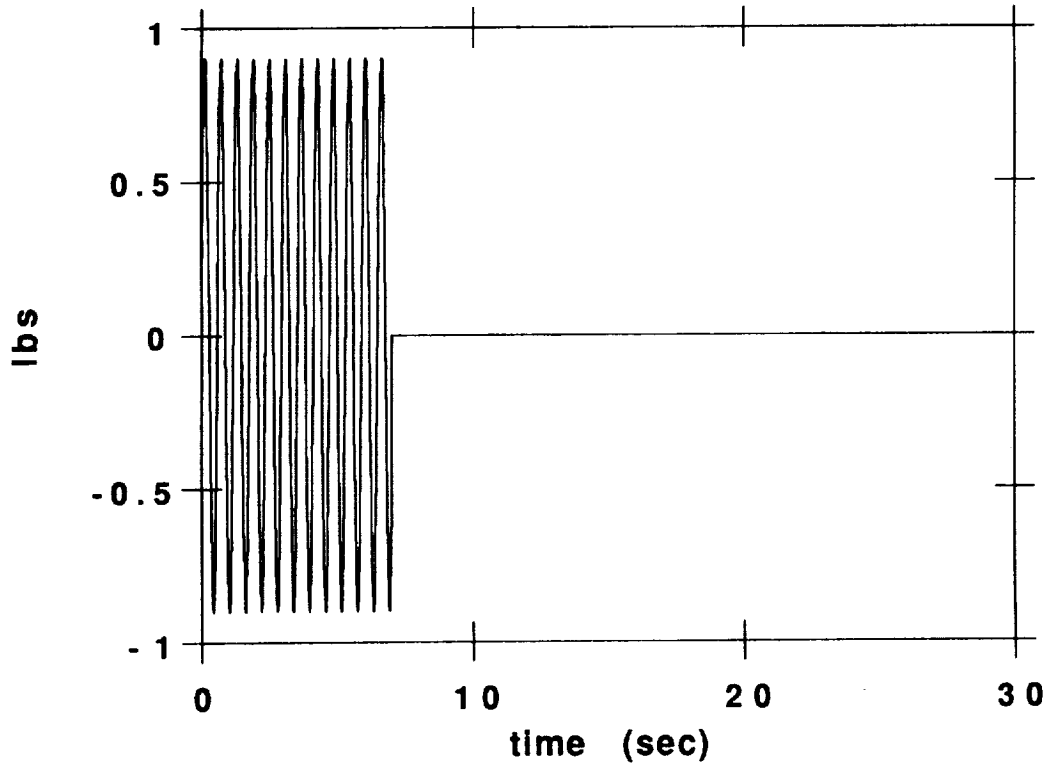


Figure 6c. Thruster #6 command time history for open loop sine wave excitation test.

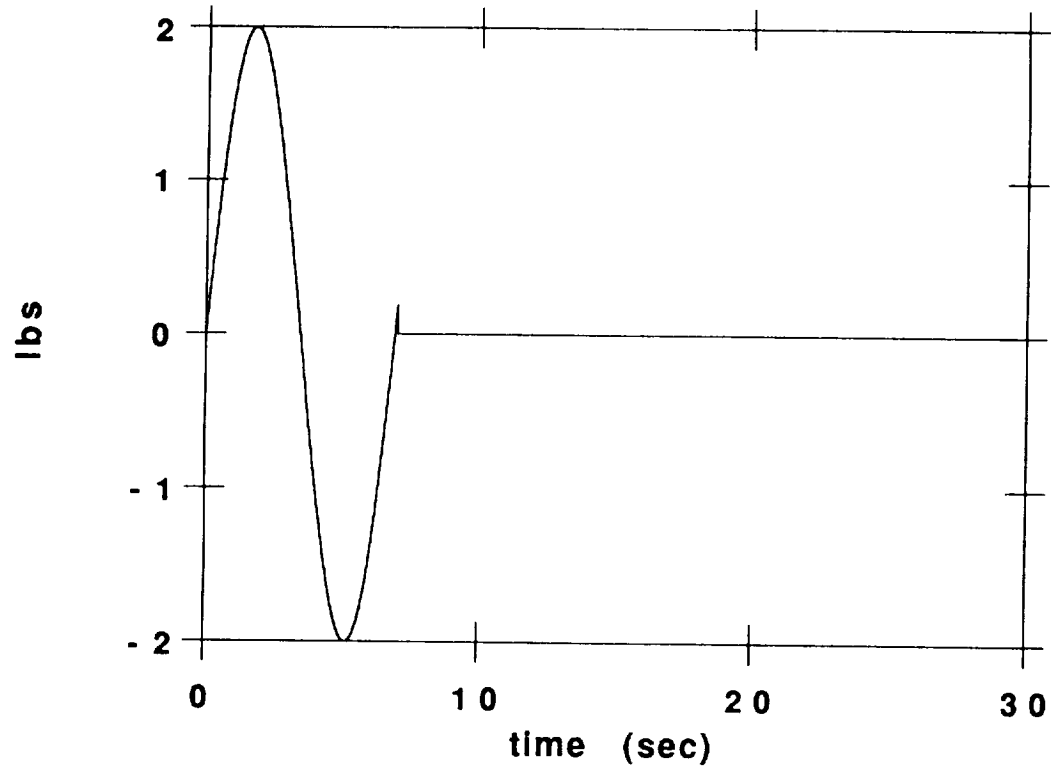


Figure 6d. Thruster #7 command time history for open loop sine wave excitation test.

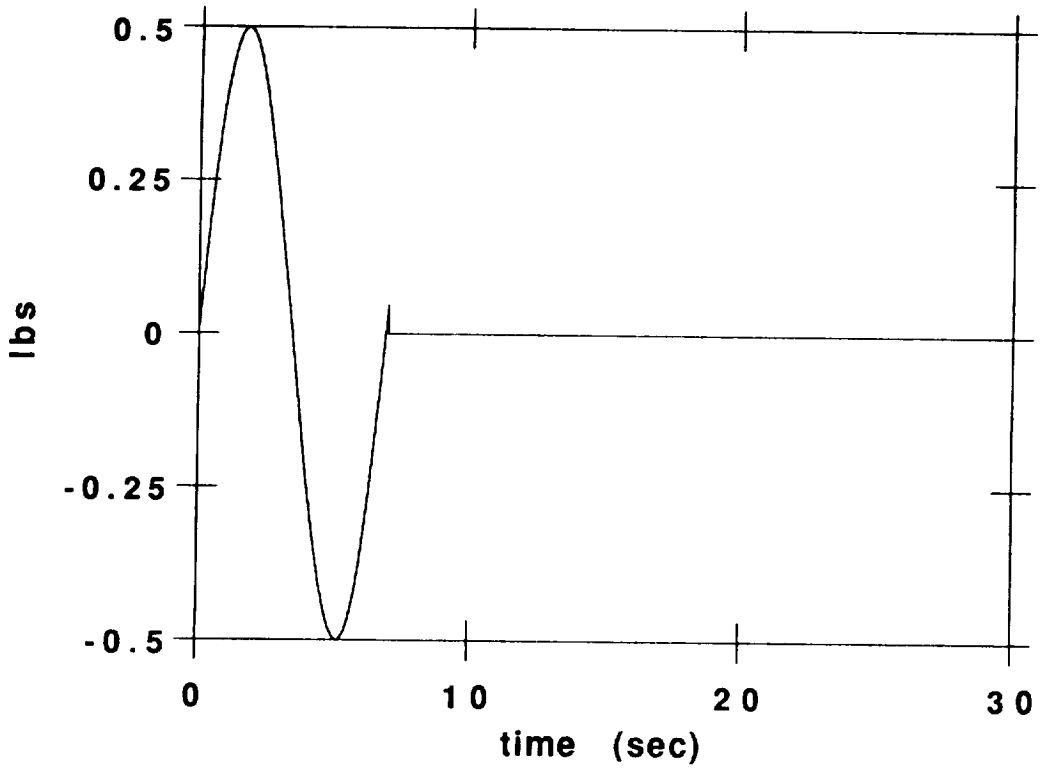


Figure 7. Composite plot of thrusters #3, #4, #6 and #7 command time histories for pulses excitation test.

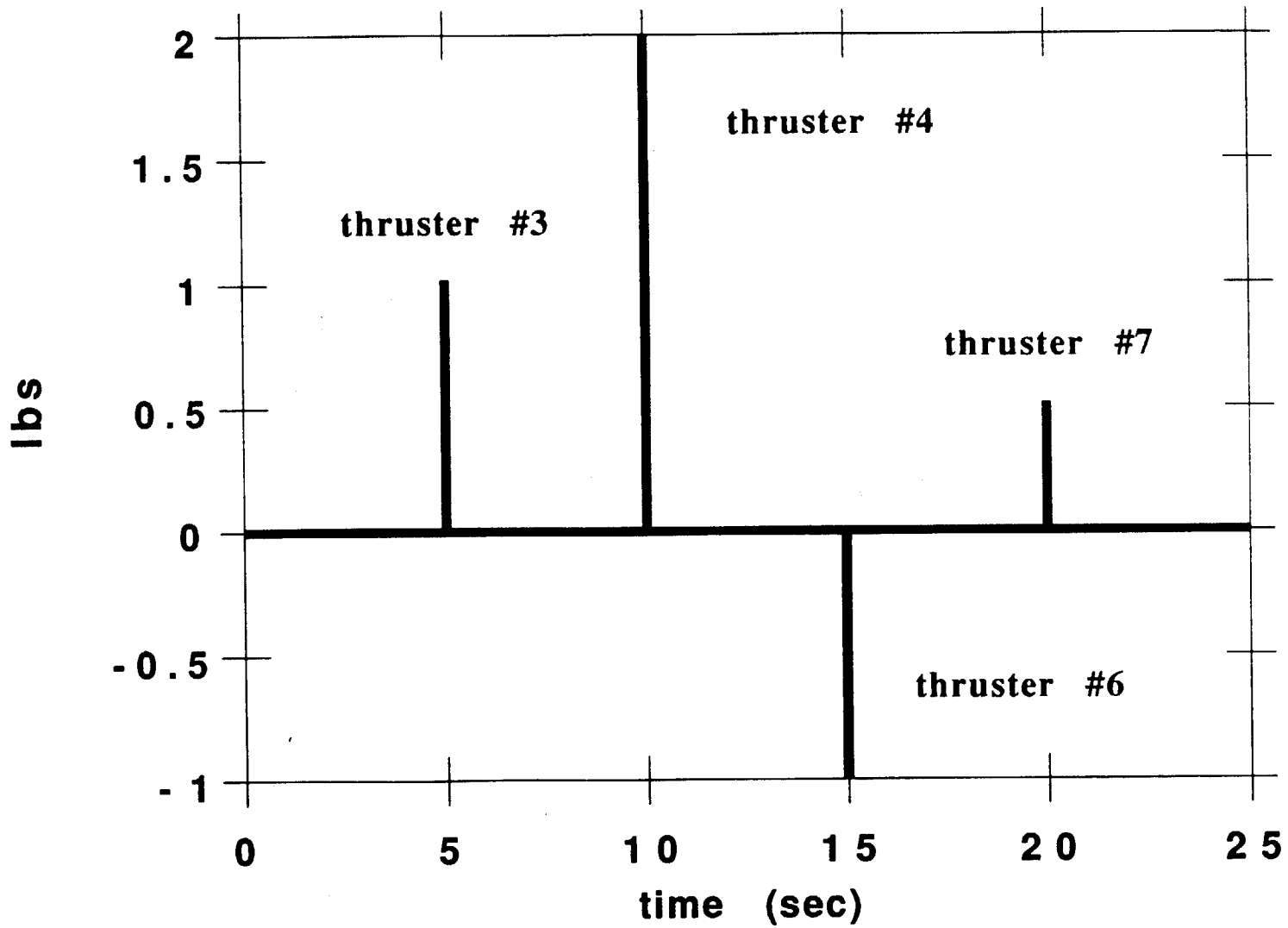


Figure 8a. Accelerometer #7 time history for open loop pulses excitation test.

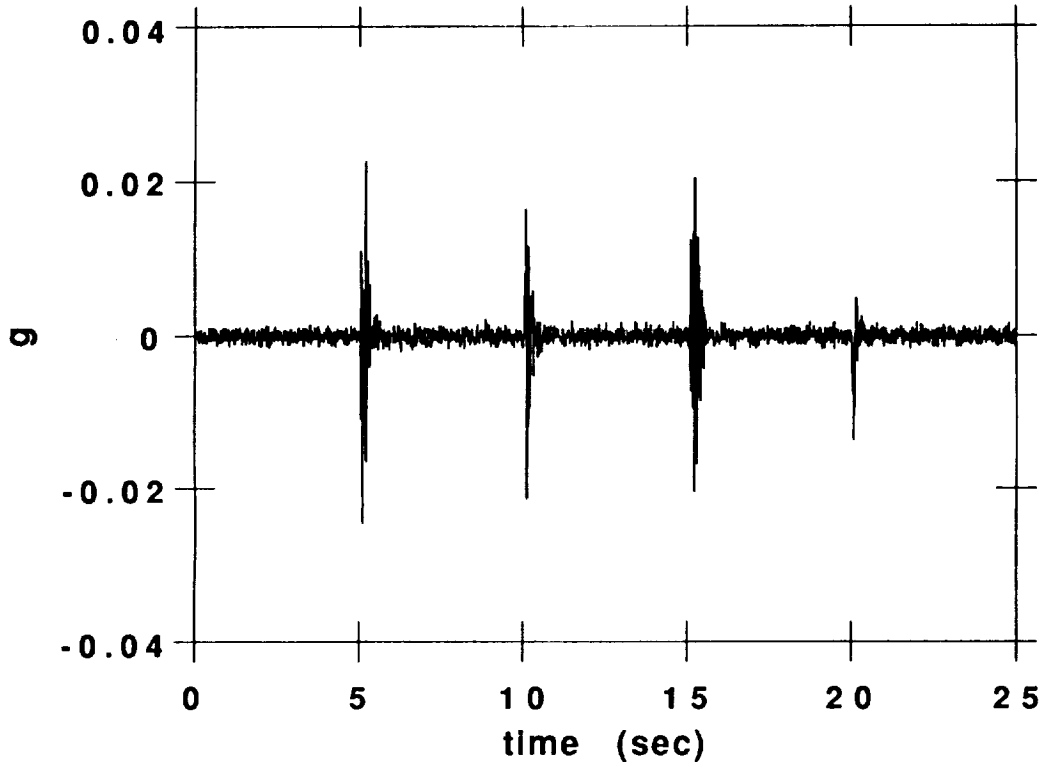


Figure 8b. Accelerometer #8 time history for open loop pulses excitation test.

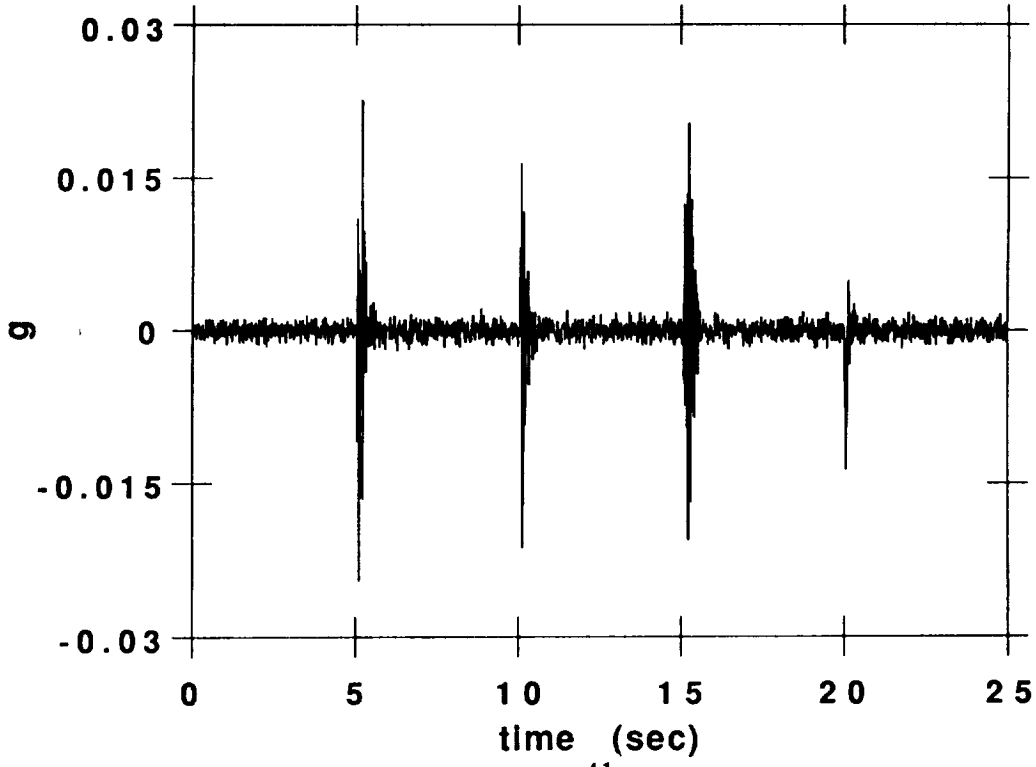


Figure 9a. Accelerometer #7 time history for open loop random excitation test.

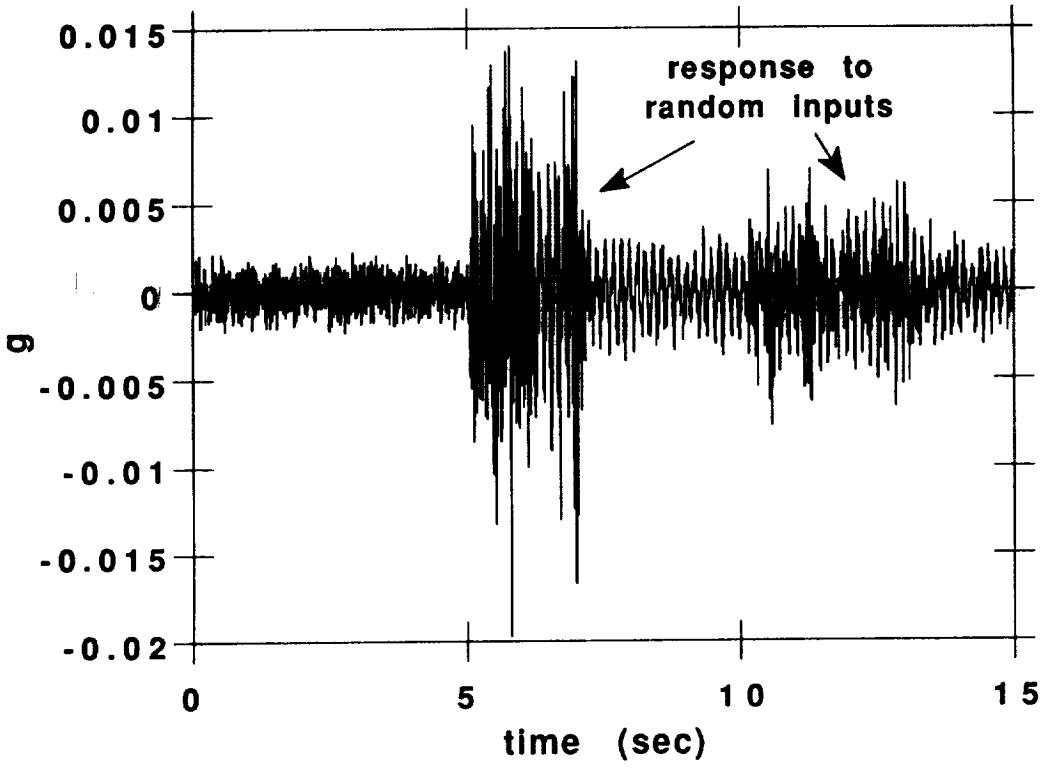


Figure 9b. Accelerometer #8 time history for open loop random excitation test.

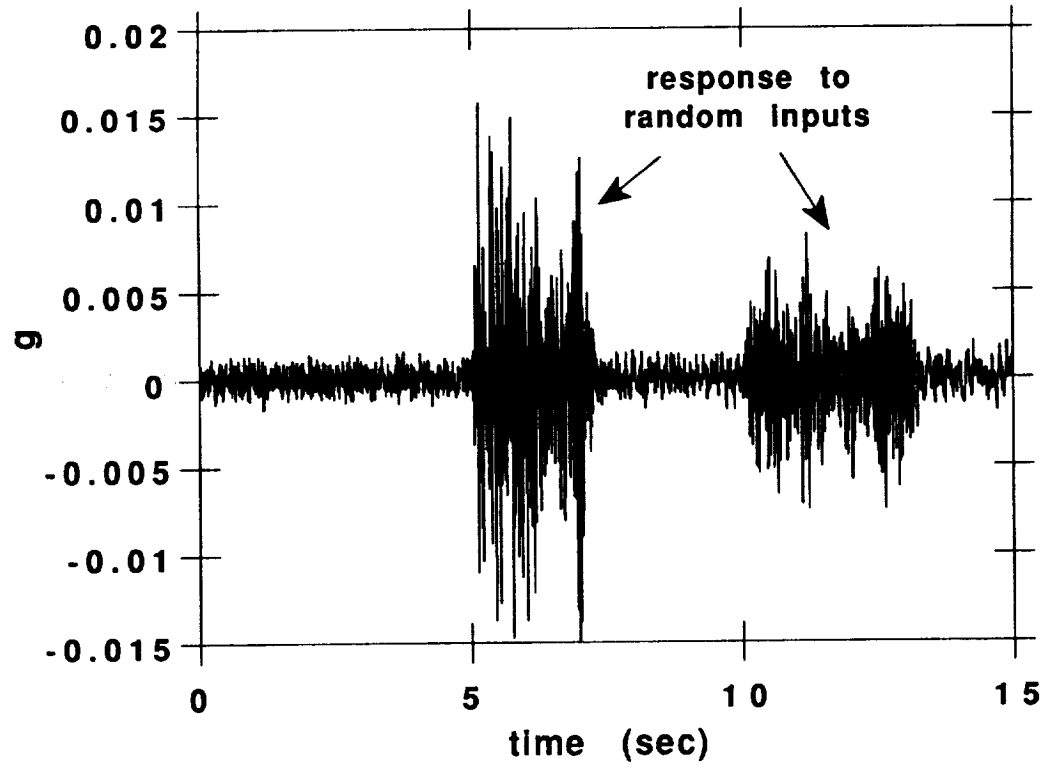


Figure 10a. Thruster #3 command time history for open loop random excitation test.

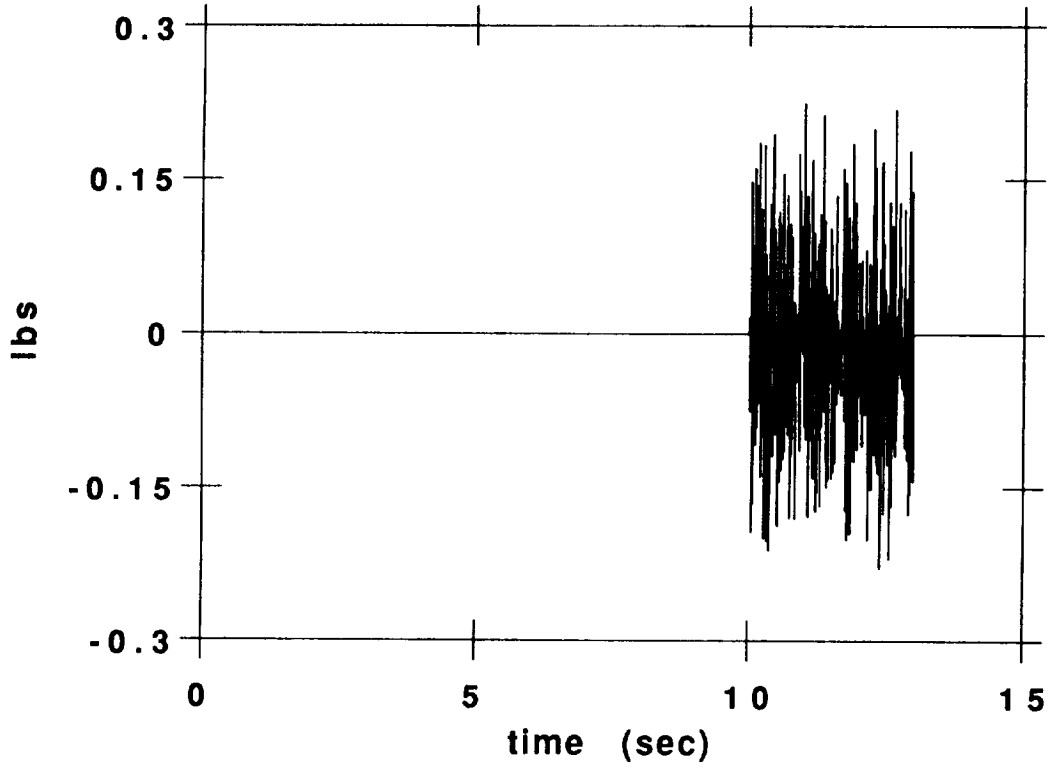


Figure 10b. Thruster #7 command time history for open loop random excitation test.

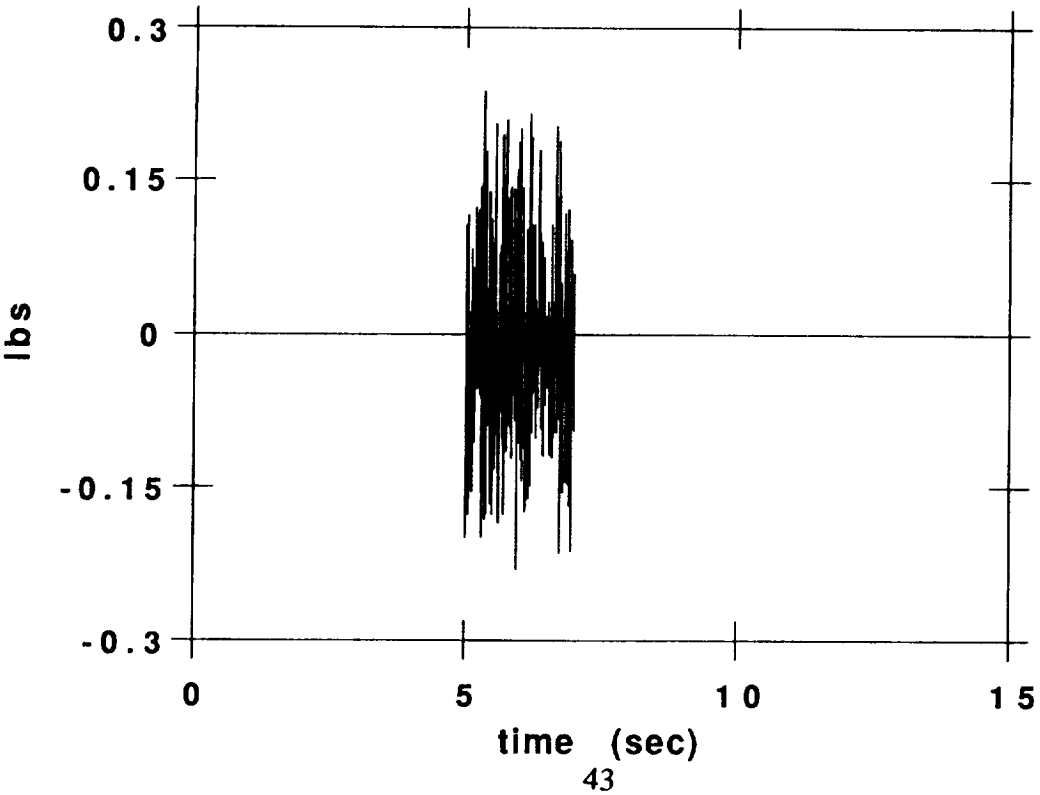


Figure 11a. Accelerometer #1 time history for open loop automatic software shutdown test - critical value 0.1 g.

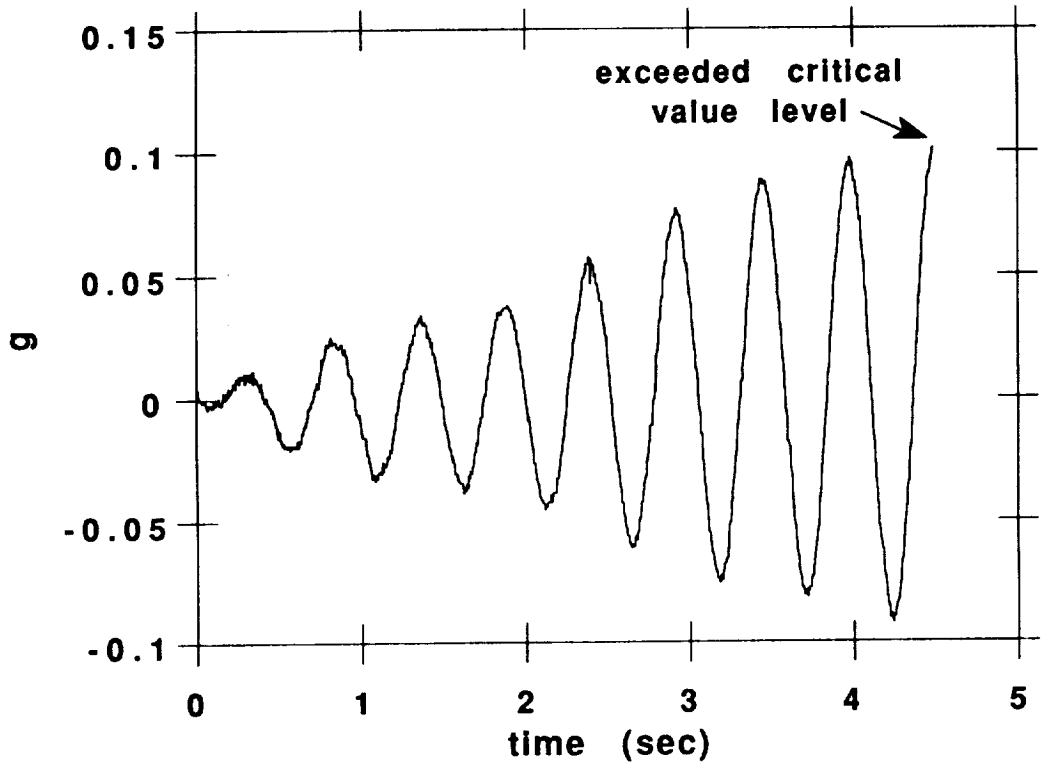


Figure 11b. Accelerometer #2 time history for open loop automatic software shutdown test - critical value 0.1g.

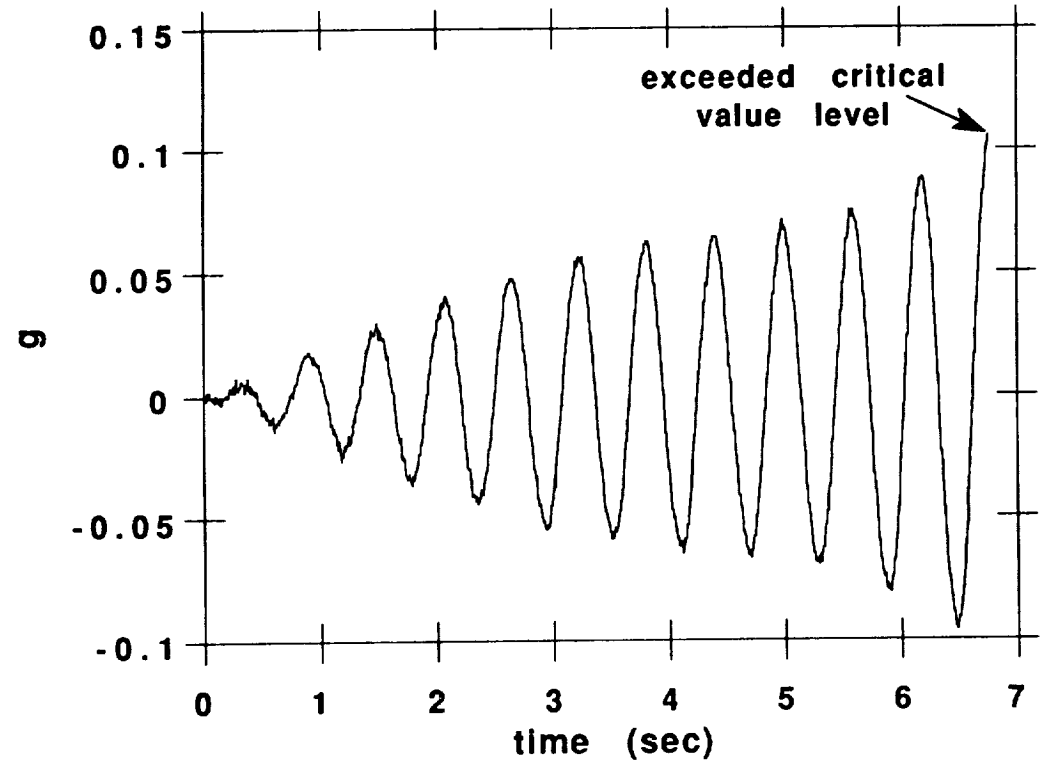


Figure 12a. Accelerometer #1 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

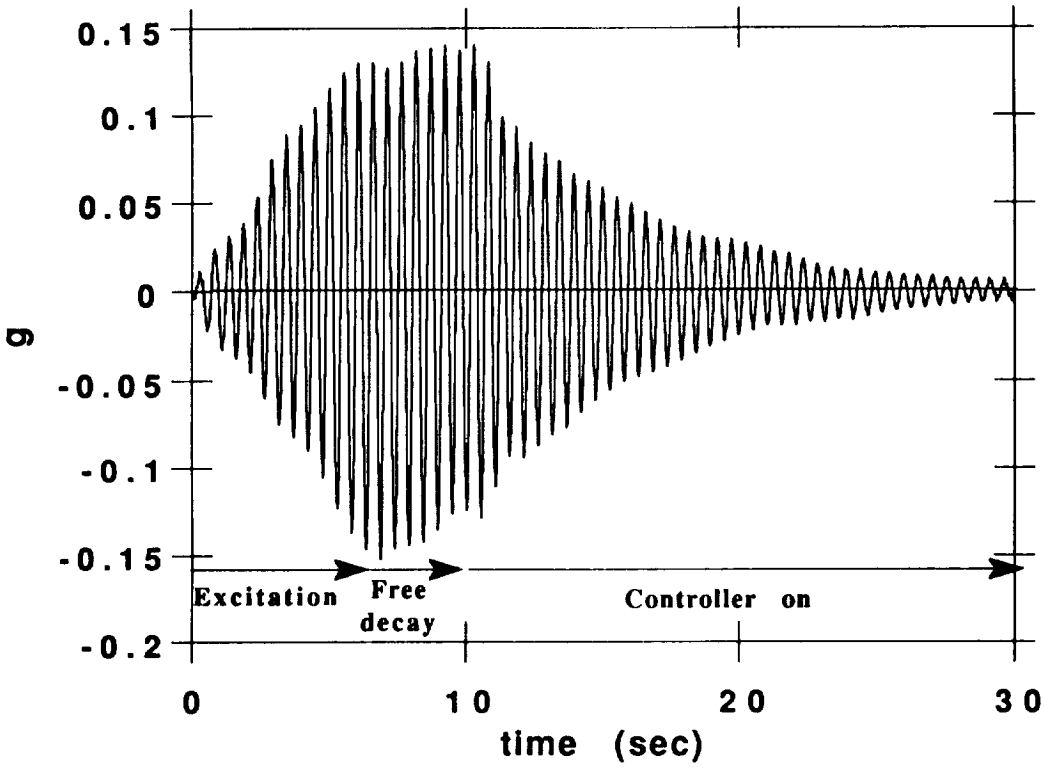


Figure 12b. Accelerometer #1 time history for closed loop test with 16 state decoupled controller - CCS.

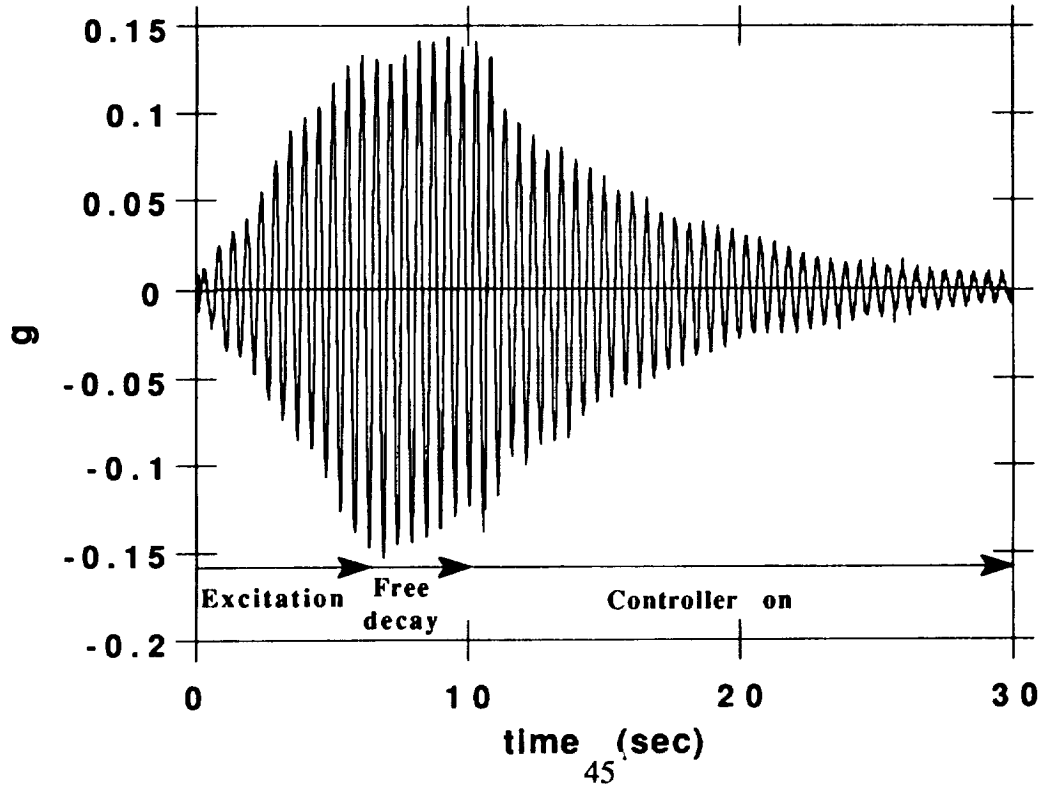


Figure 12g. Accelerometer #4 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

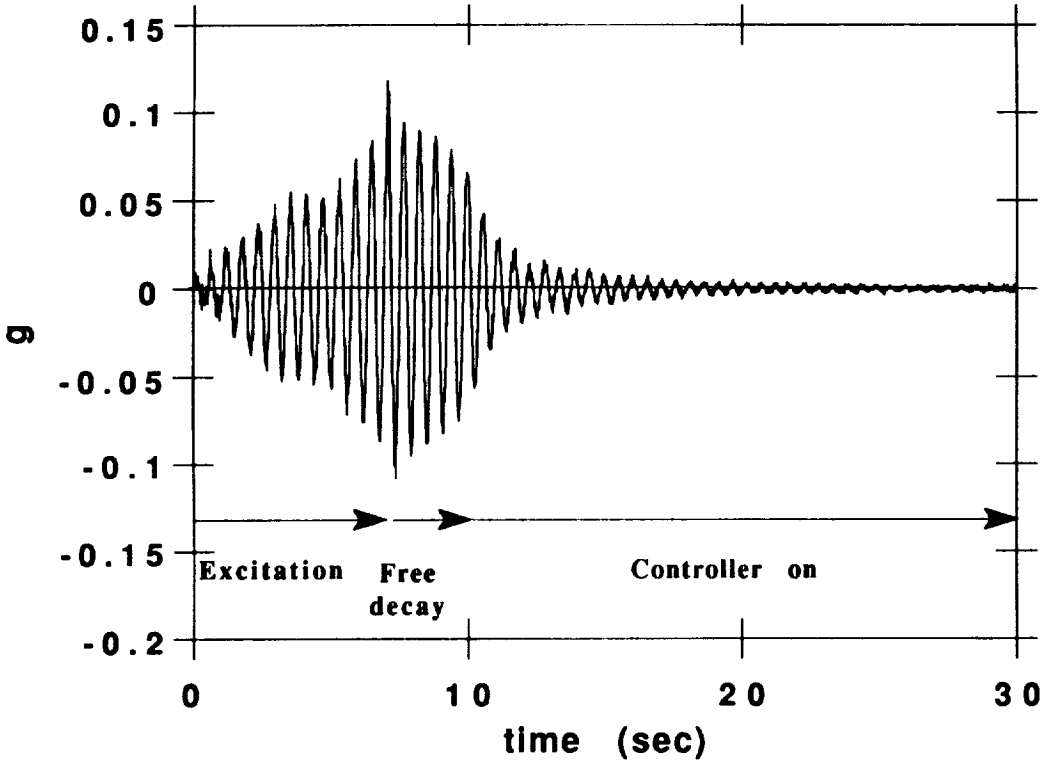


Figure 12h. Accelerometer #4 time history for closed loop test with 16 state decoupled controller - CCS.

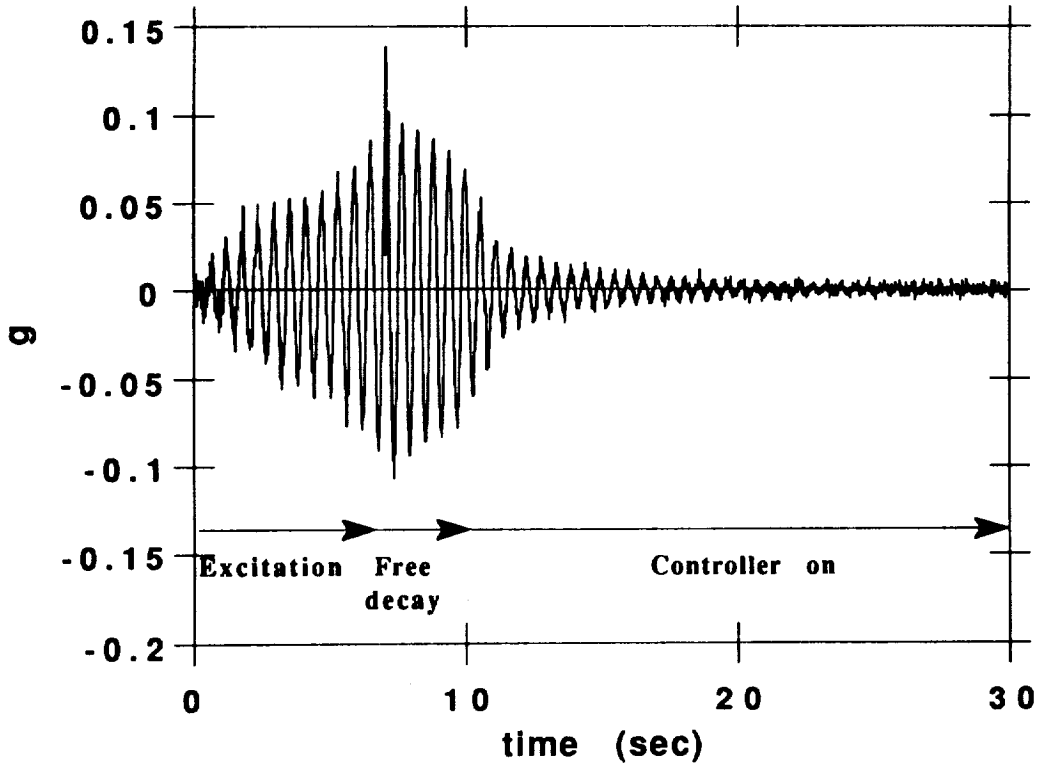


Figure 12m. Accelerometer #7 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

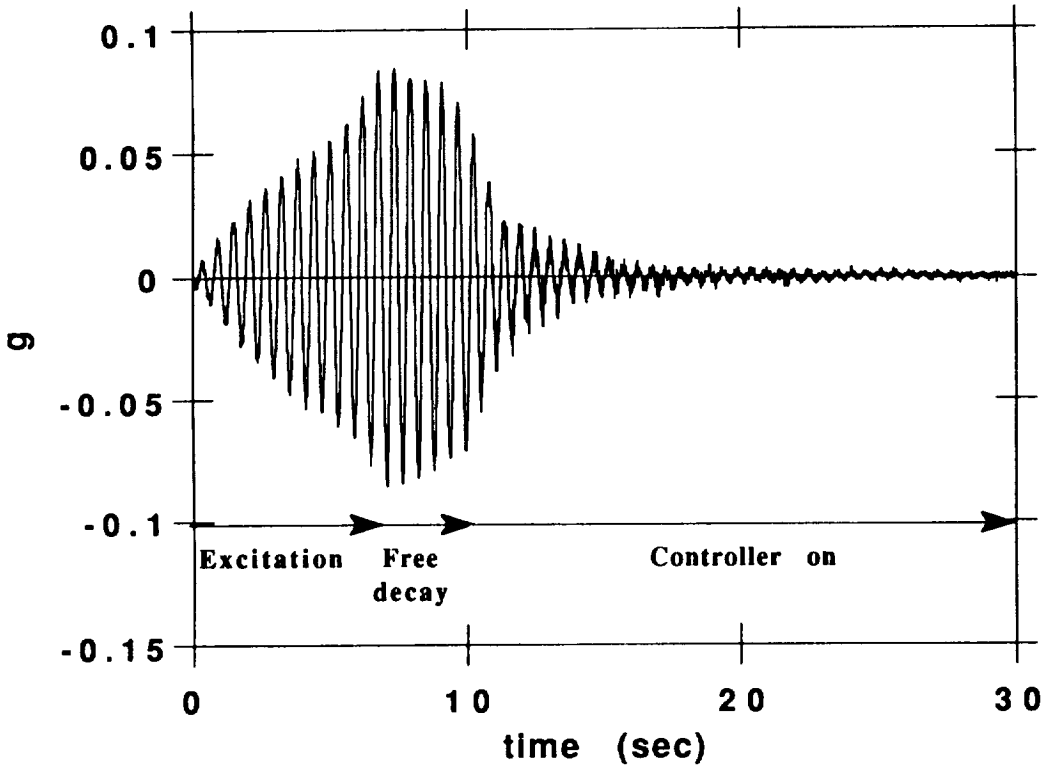


Figure 12n. Accelerometer #7 time history for closed loop test with 16 state decoupled controller - CCS.

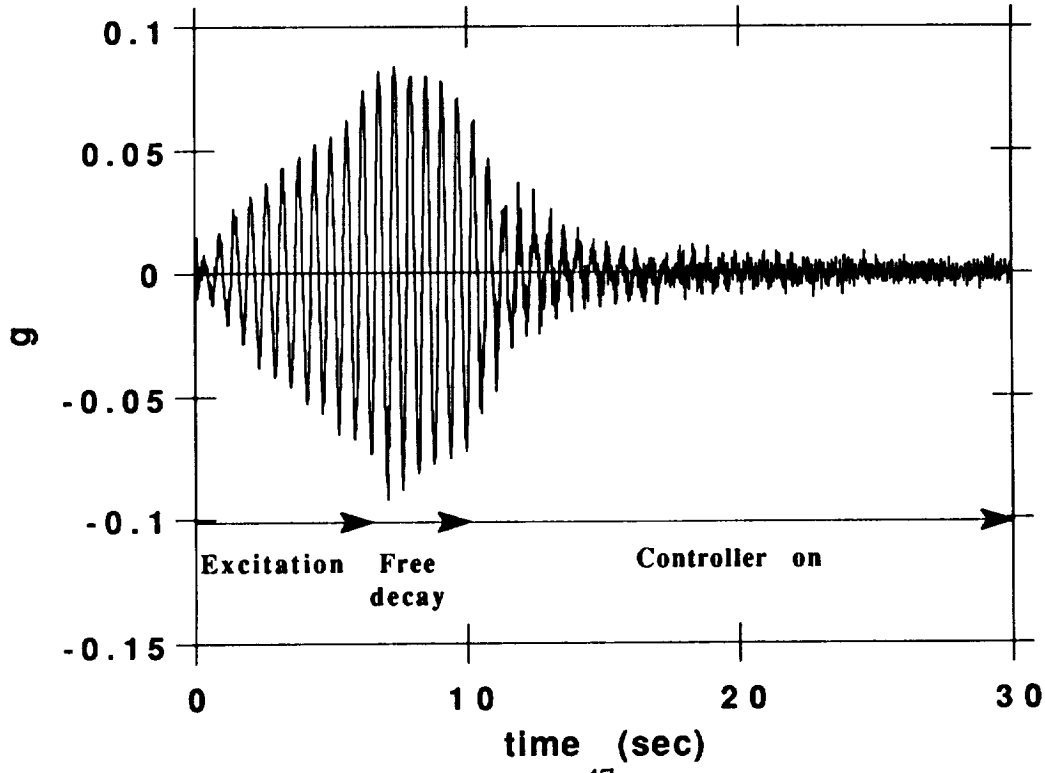


Figure 12k. Accelerometer #6 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

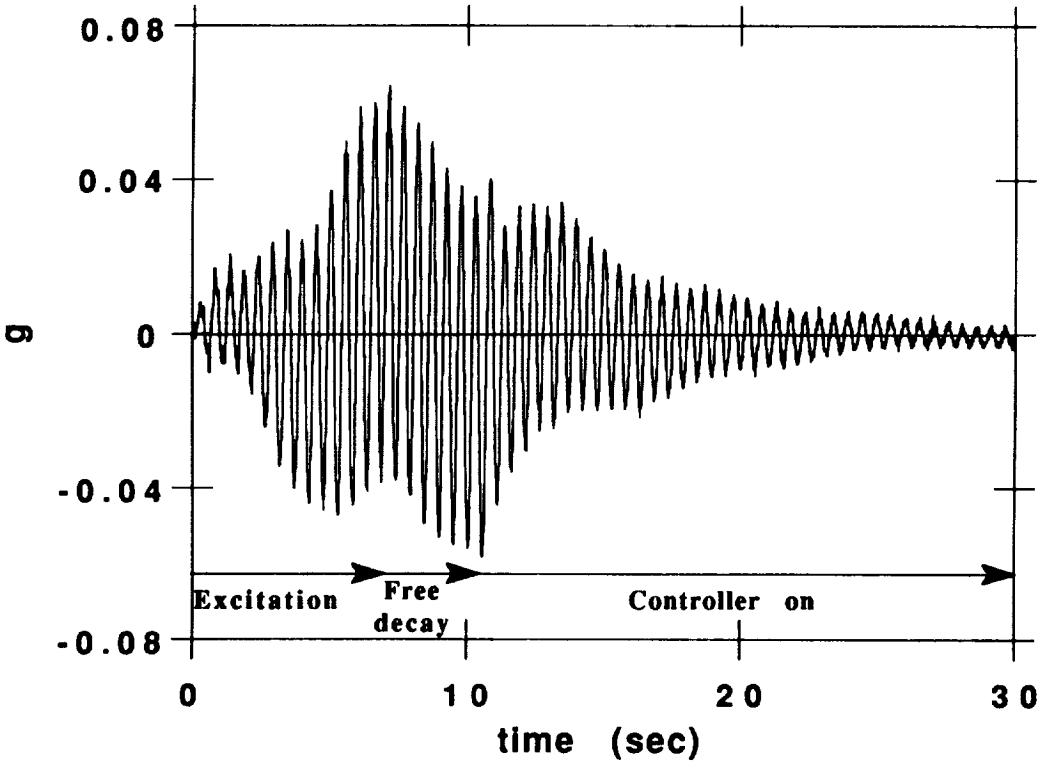


Figure 12l. Accelerometer #6 time history for closed loop test with 16 state decoupled controller - CCS.

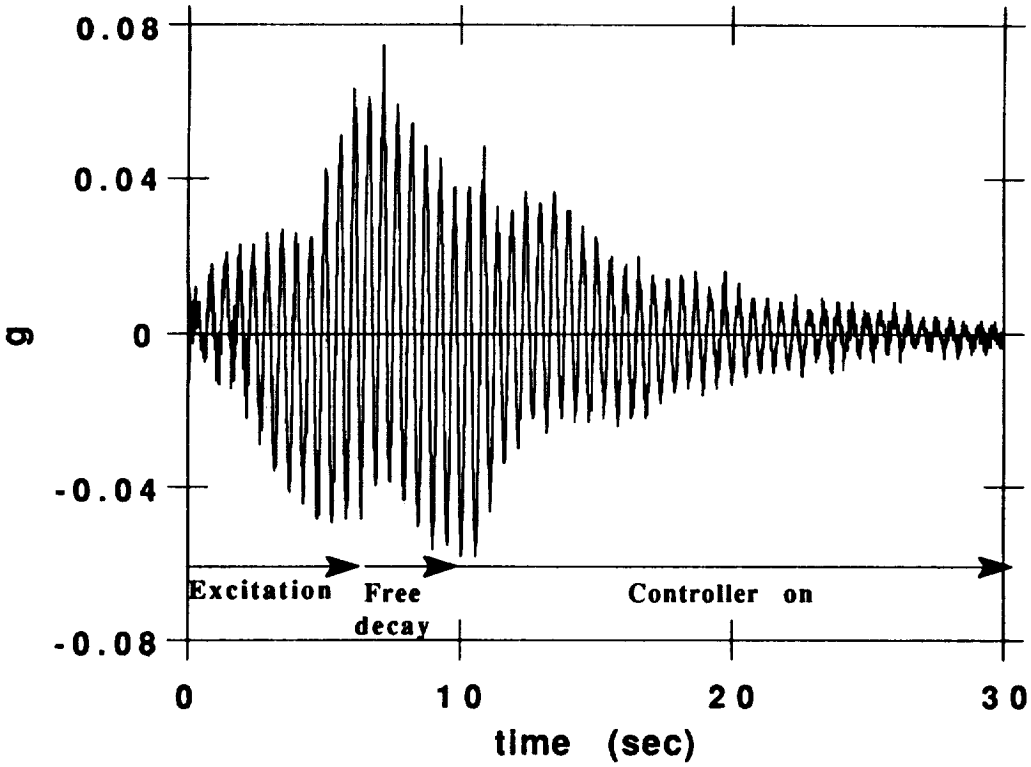


Figure 12i. Accelerometer #5 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

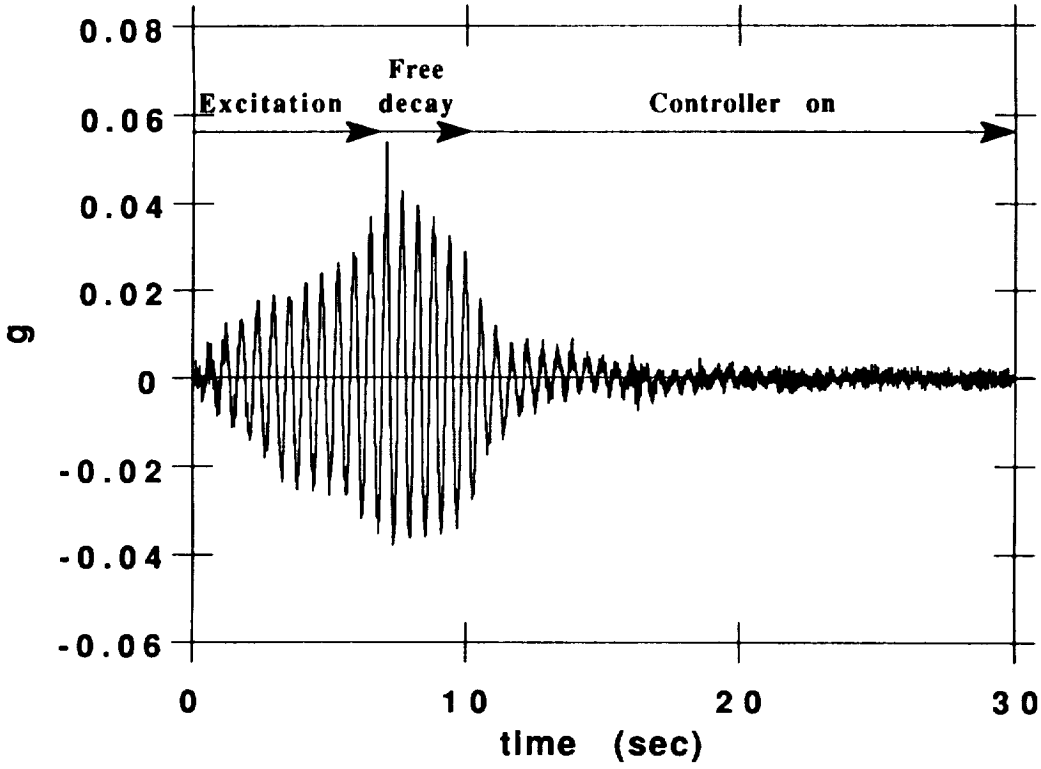


Figure 12j. Accelerometer #5 time history for closed loop test with 16 state decoupled controller - CCS.

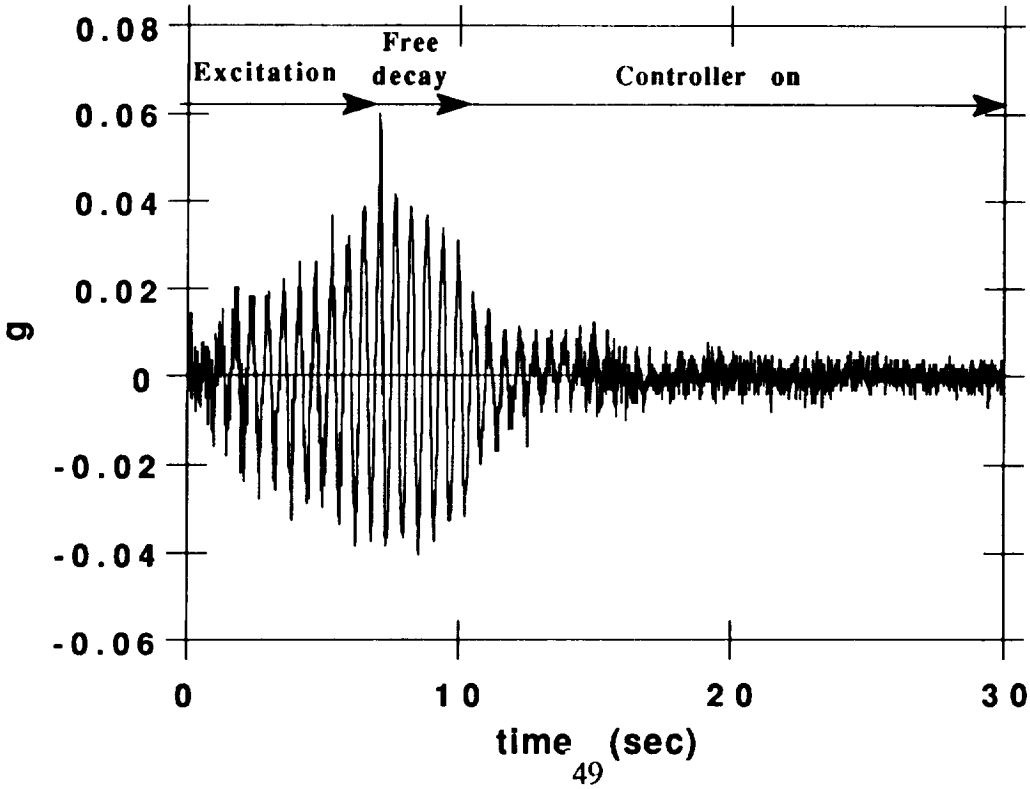


Figure 12e. Accelerometer #3 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

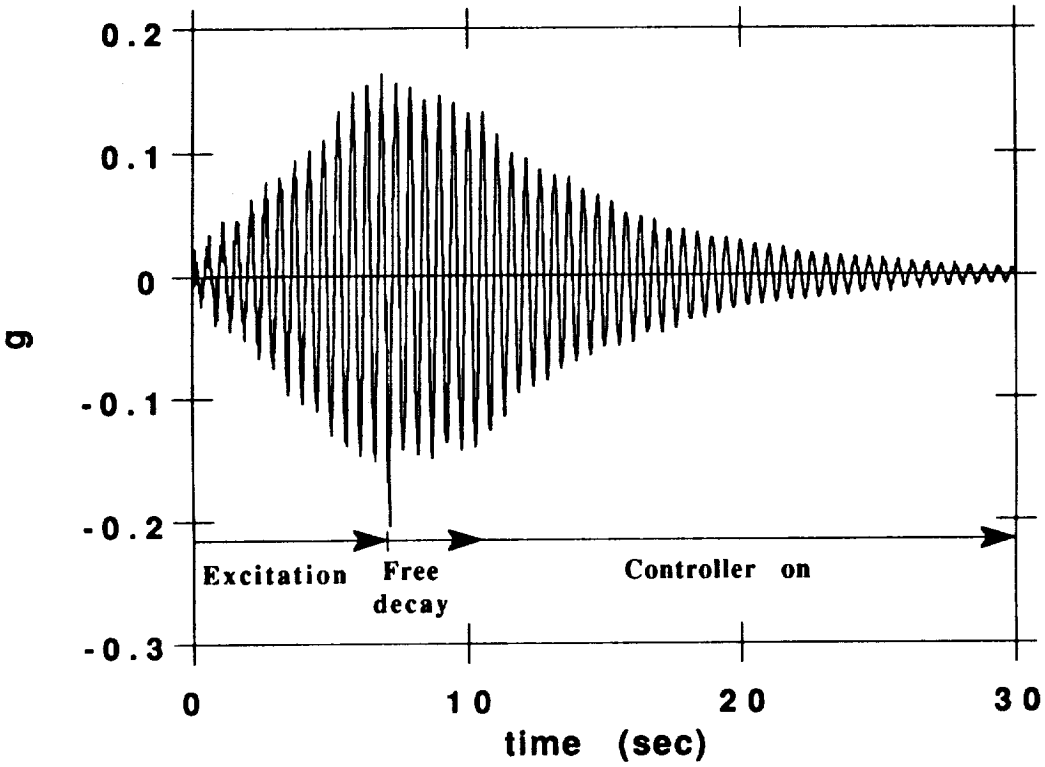


Figure 12f. Accelerometer #3 time history for closed loop test with 16 state decoupled controller - CCS.

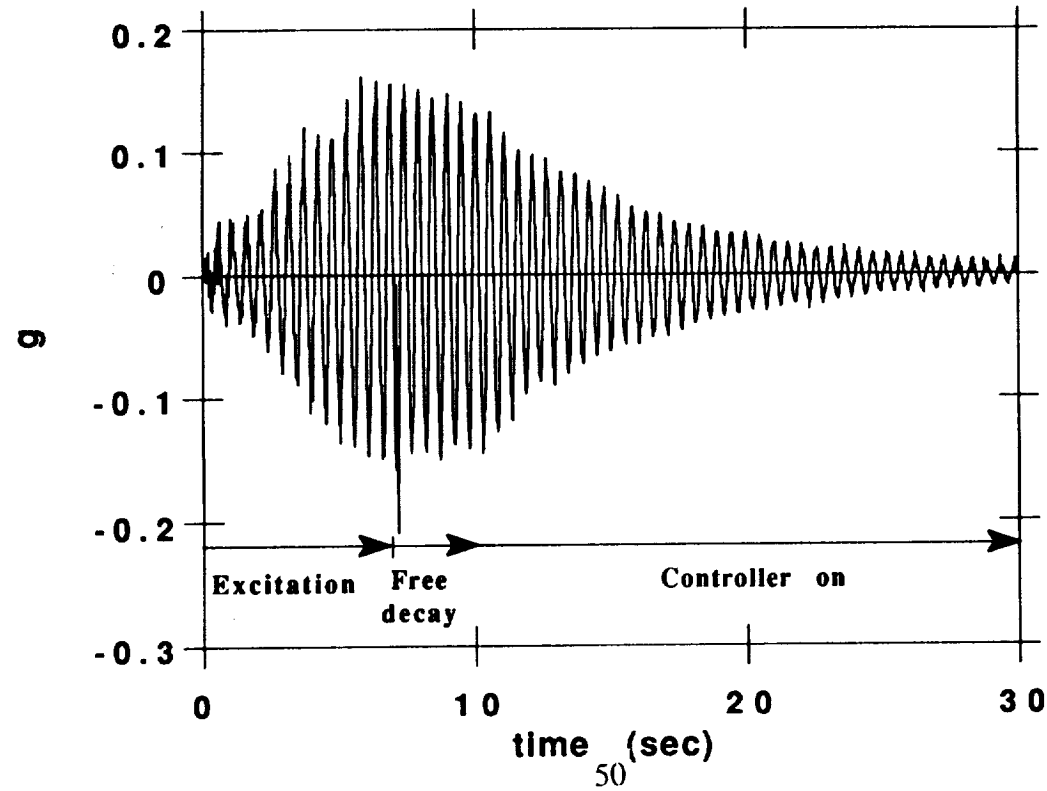


Figure 12c. Accelerometer #2 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

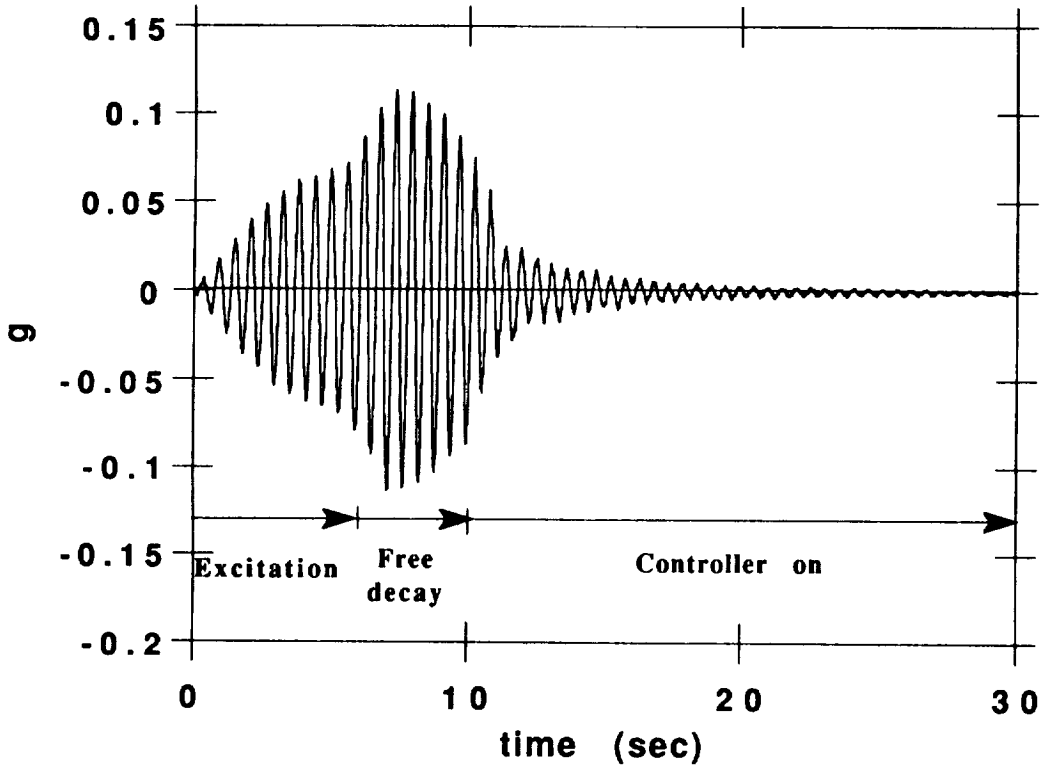


Figure 12d. Accelerometer #2 time history for closed loop test with 16 state decoupled controller - CCS.

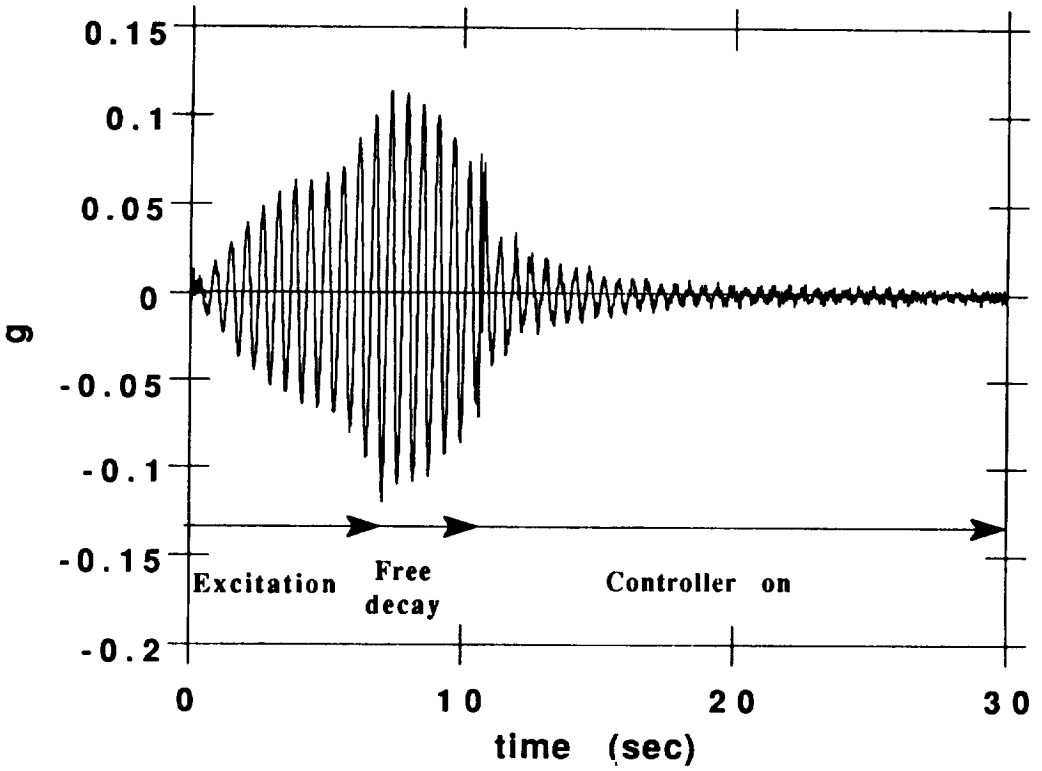


Figure 12o. Accelerometer #8 time history for closed loop test with 16 state decoupled controller - SSRL VAX.

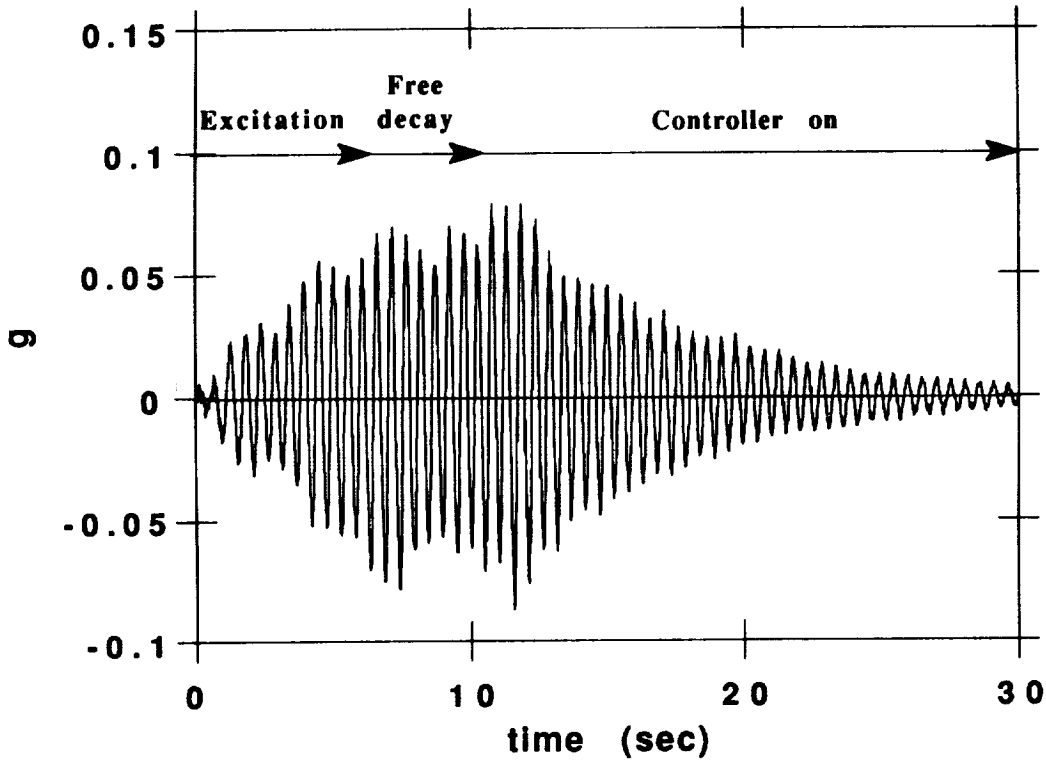


Figure 12p. Accelerometer #8 time history for closed loop test with 16 state decoupled controller - CCS.

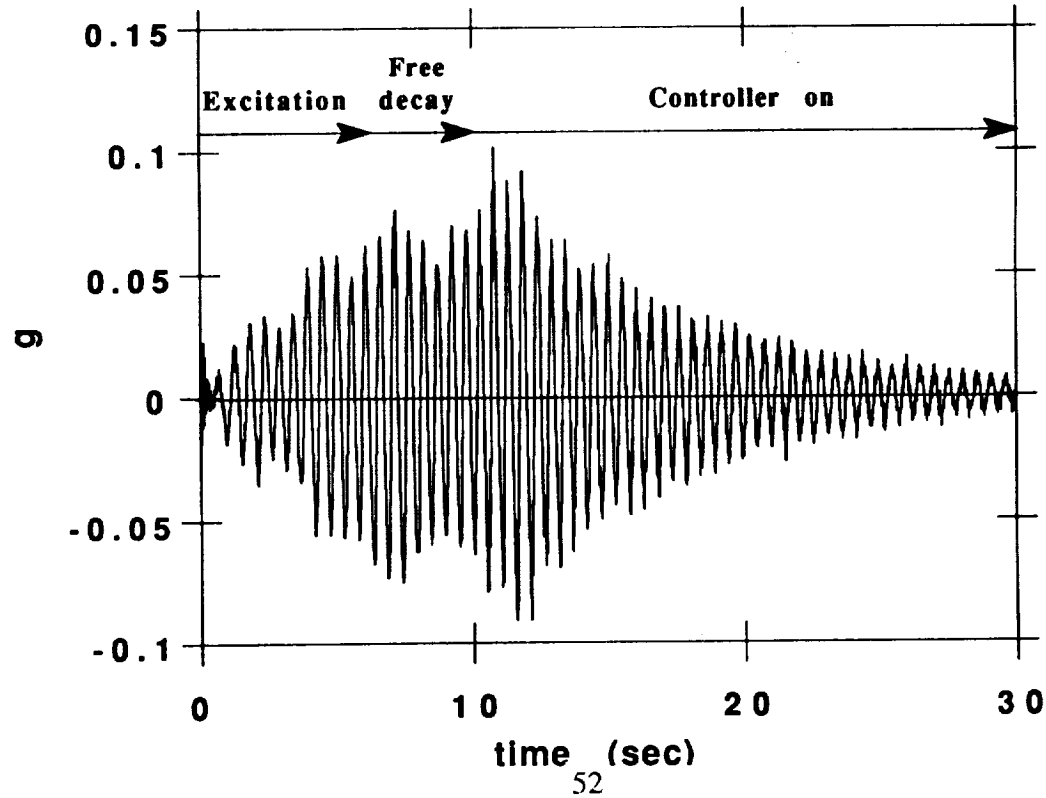


Figure 13a. Thruster #1 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

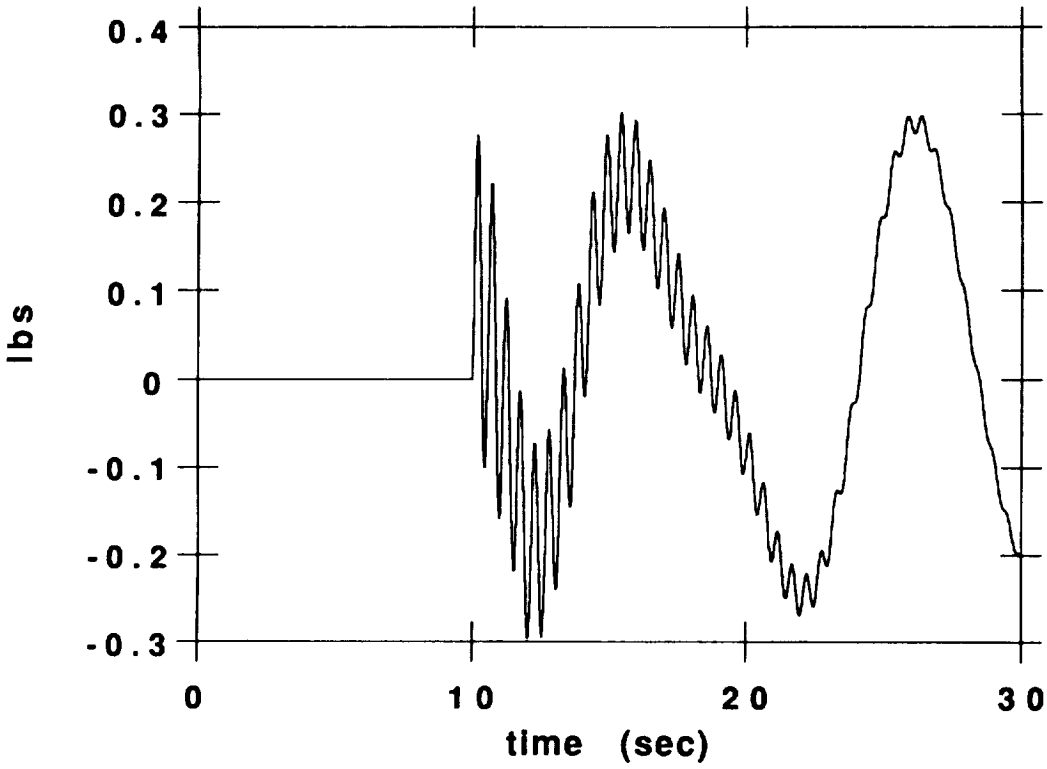


Figure 13b. Thruster #1 command time history for closed loop test with 16 state decoupled controller - CCS.

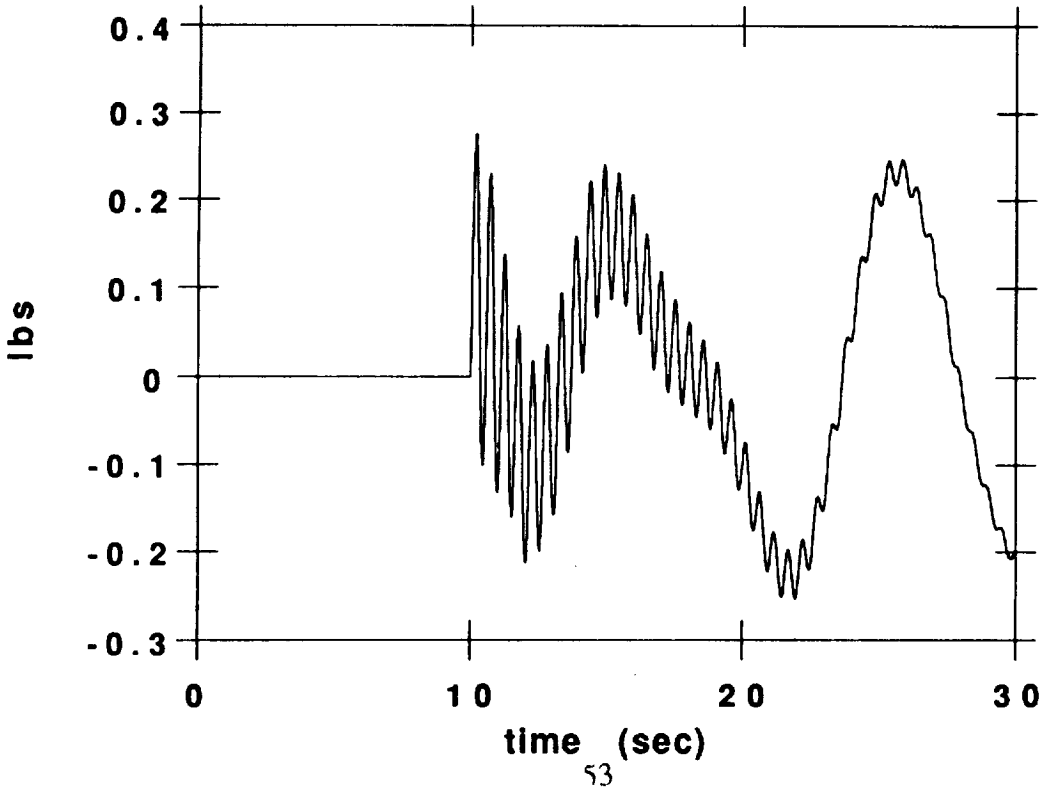


Figure 13c. Thruster #2 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

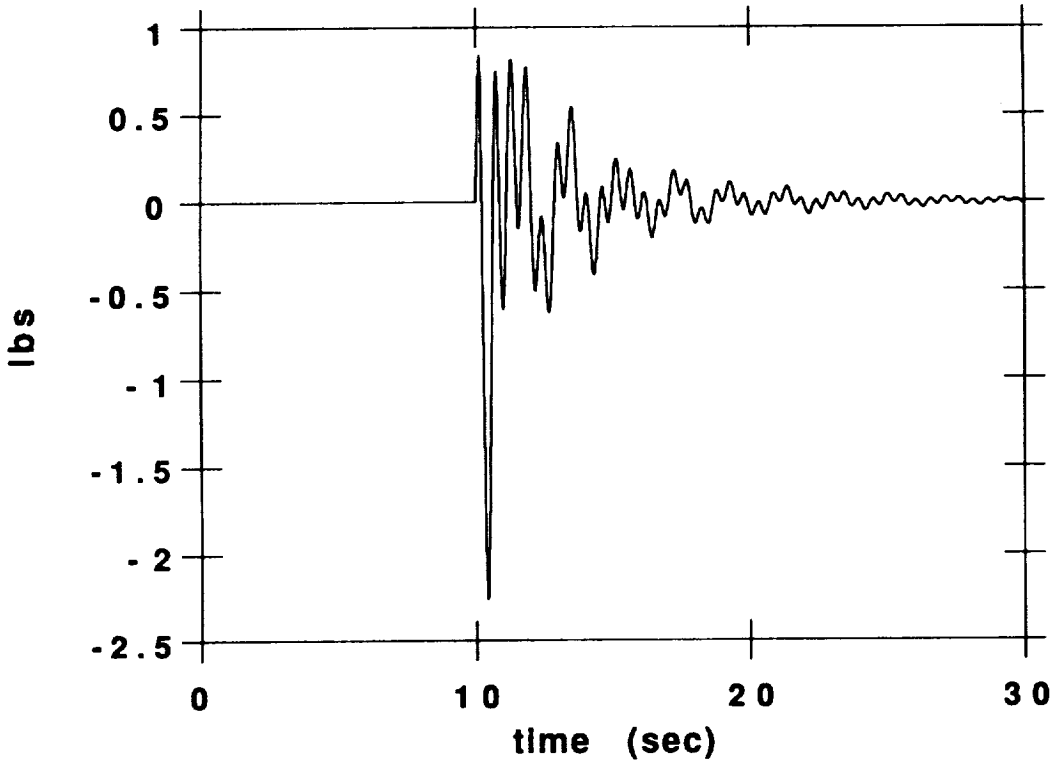


Figure 13d. Thruster #2 command time history for closed loop test with 16 state decoupled controller - CCS.

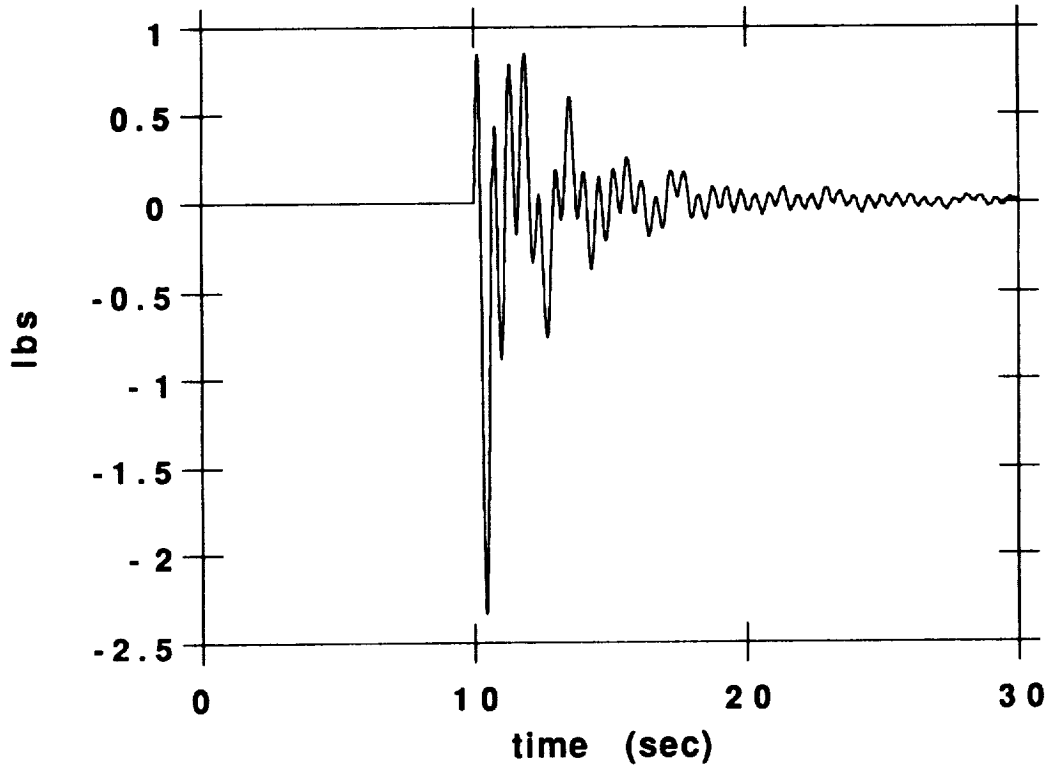


Figure 13e. Thruster #3 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

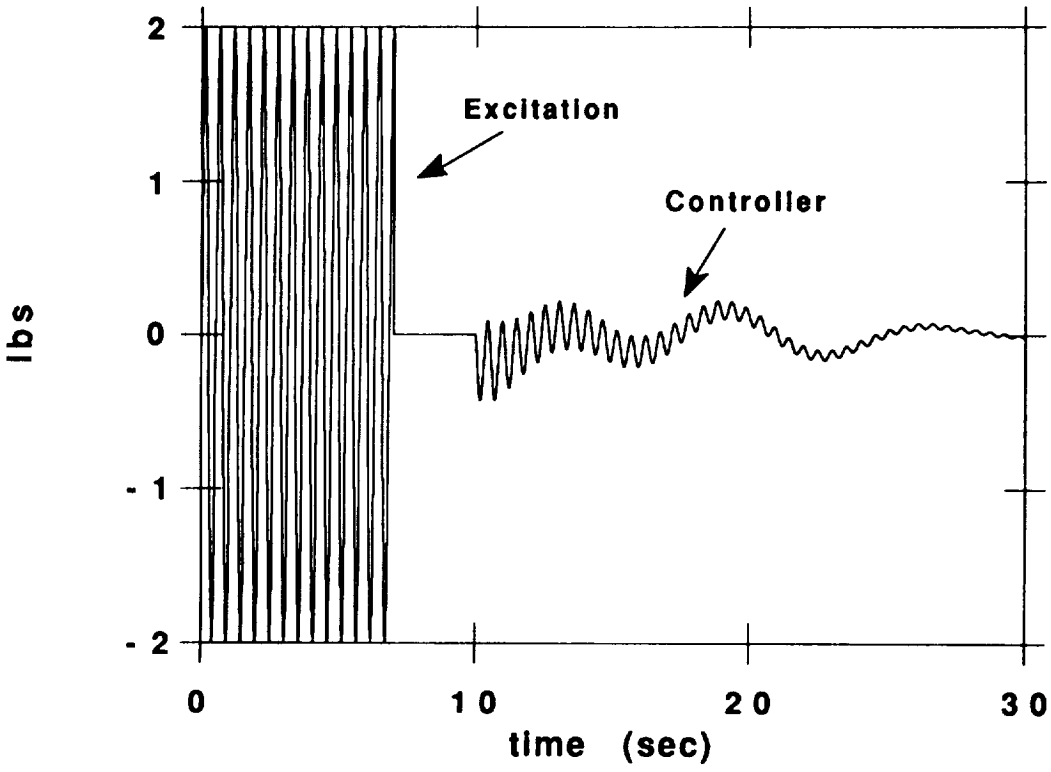


Figure 13f. Thruster #3 command time history for closed test with 16 state decoupled controller - CCS.

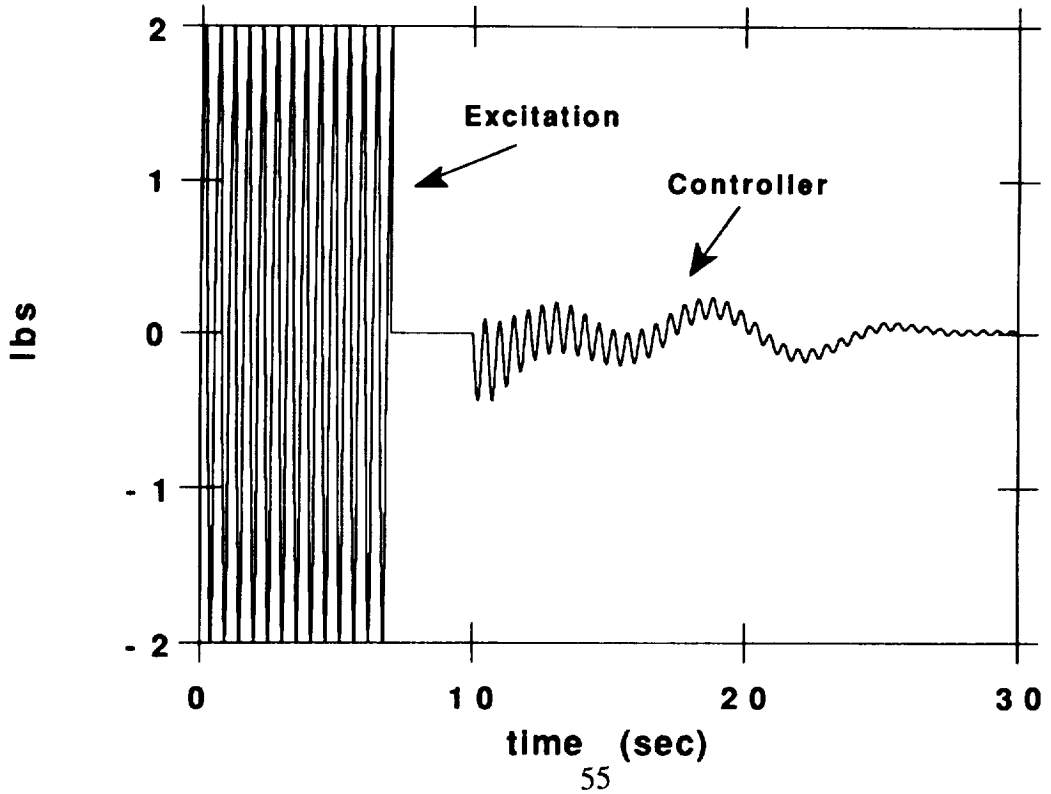


Figure 13g. Thruster #4 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

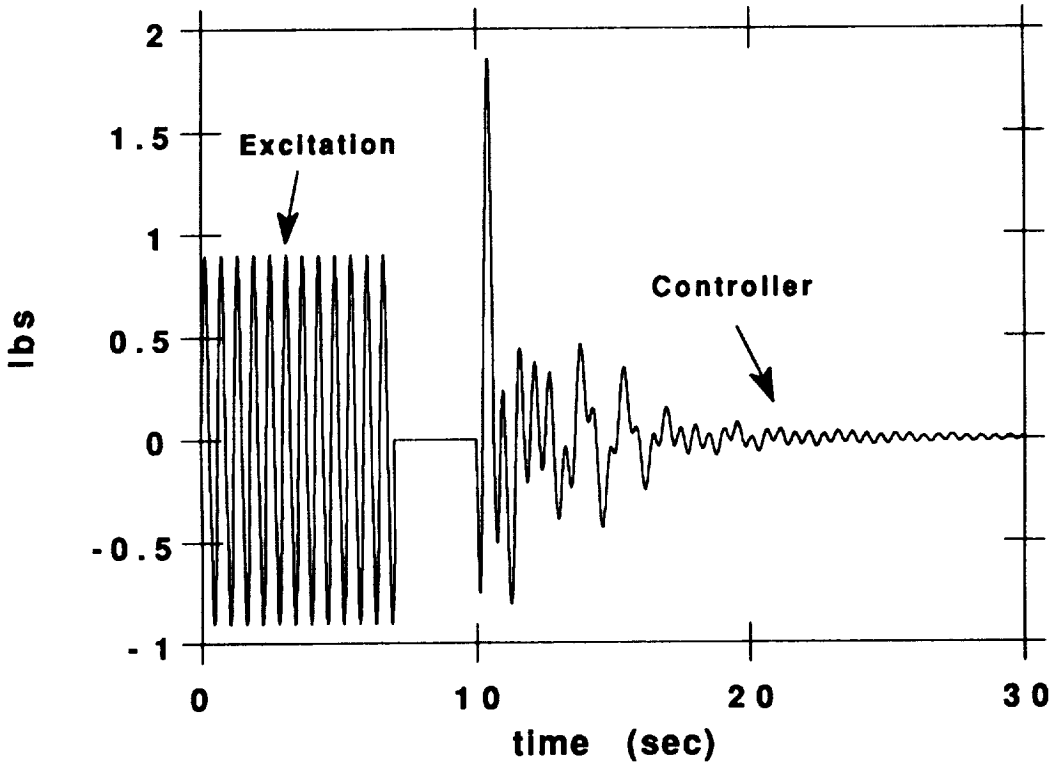


Figure 13h. Thruster #4 command time history for closed loop test with 16 state decoupled controller - CCS.

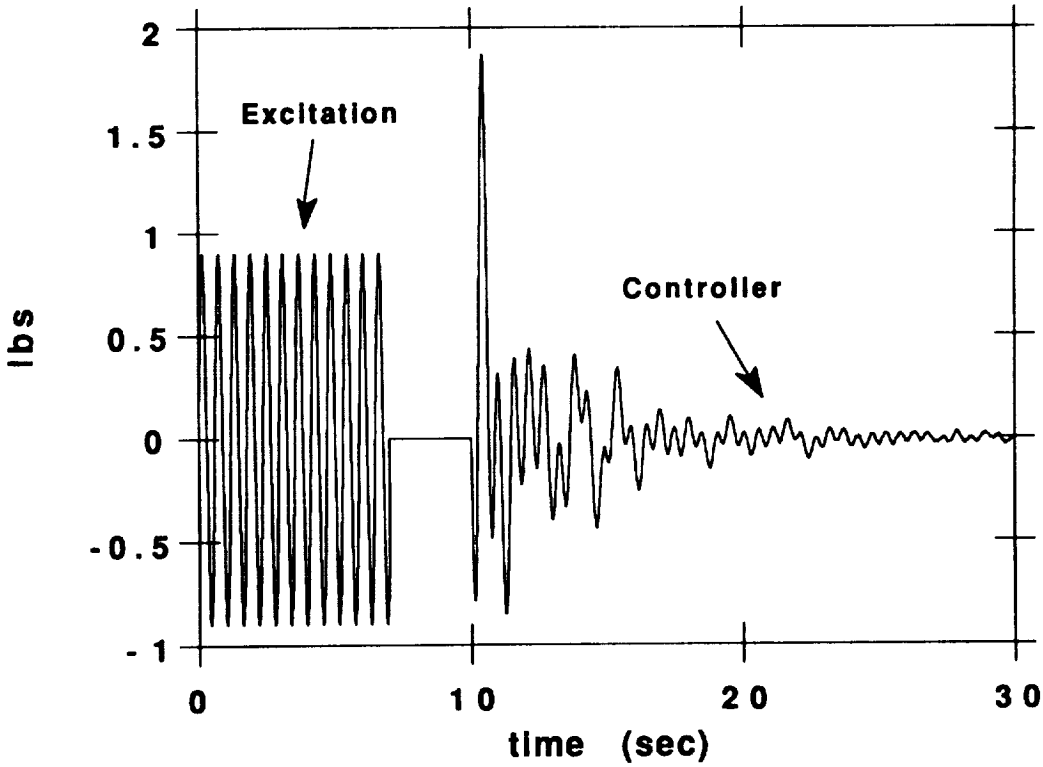


Figure 13i. Thruster #5 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

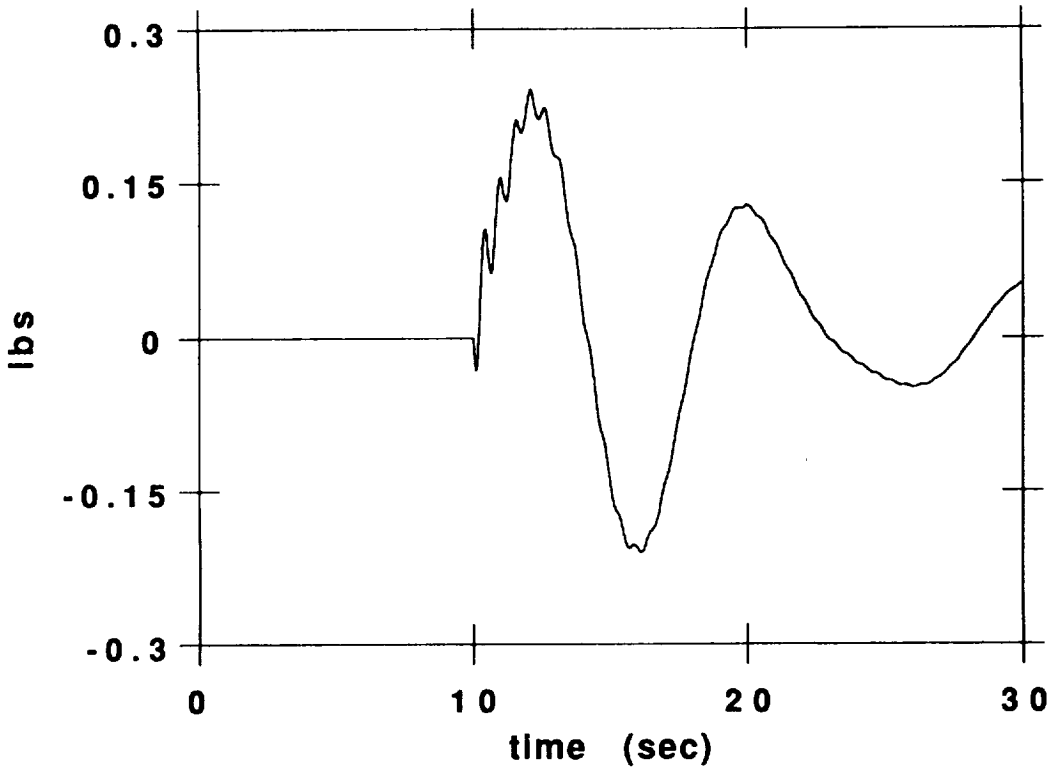


Figure 13j. Thruster #5 command time history for closed loop test with 16 state decoupled controller - CCS.

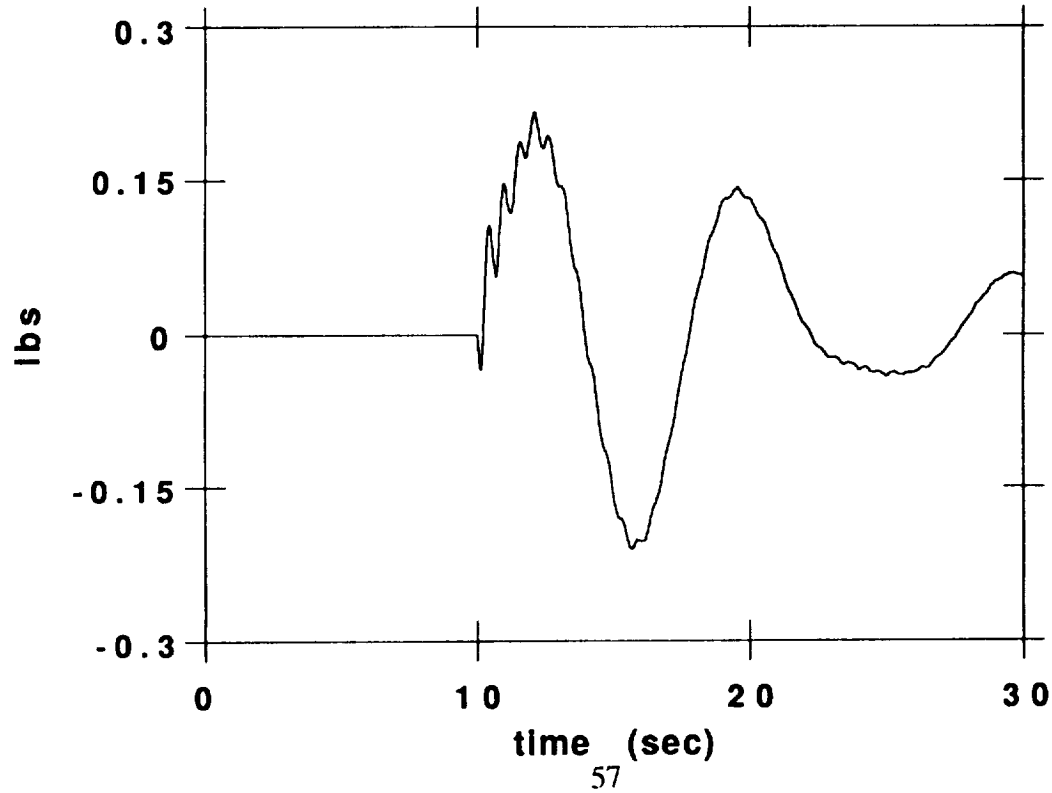


Figure 13k. Thruster #6 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

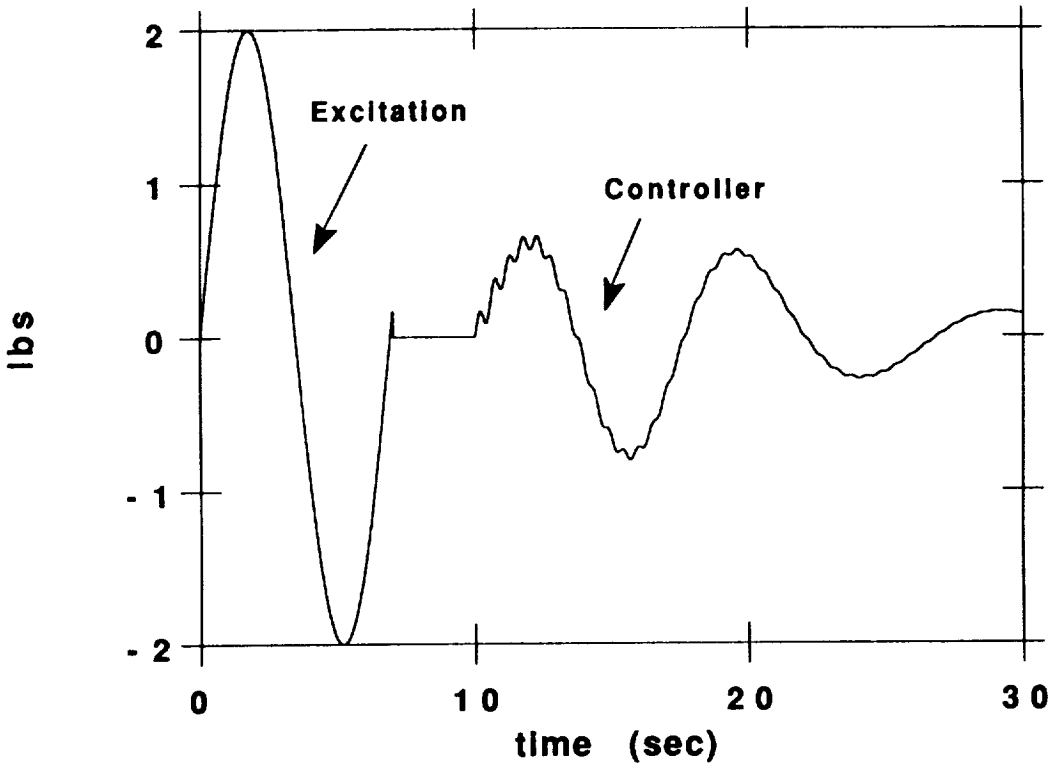


Figure 13l. Thruster #6 command time history for closed loop test with 16 state decoupled controller - CCS.

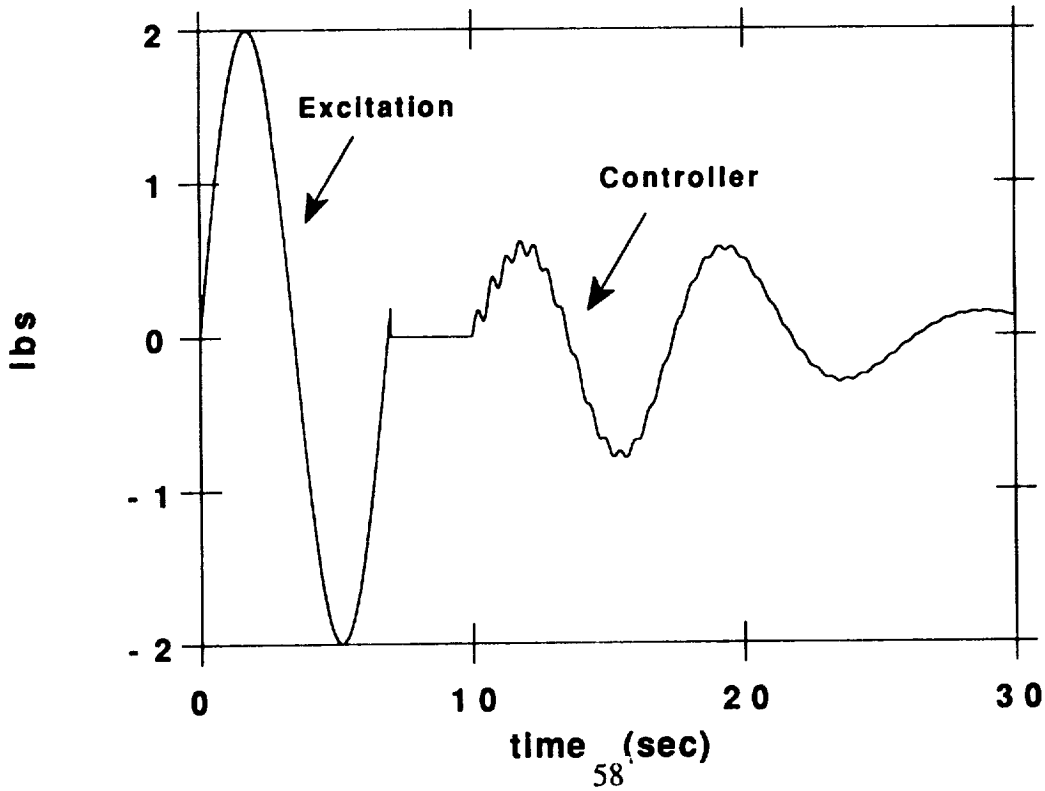


Figure 13m. Thruster #7 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

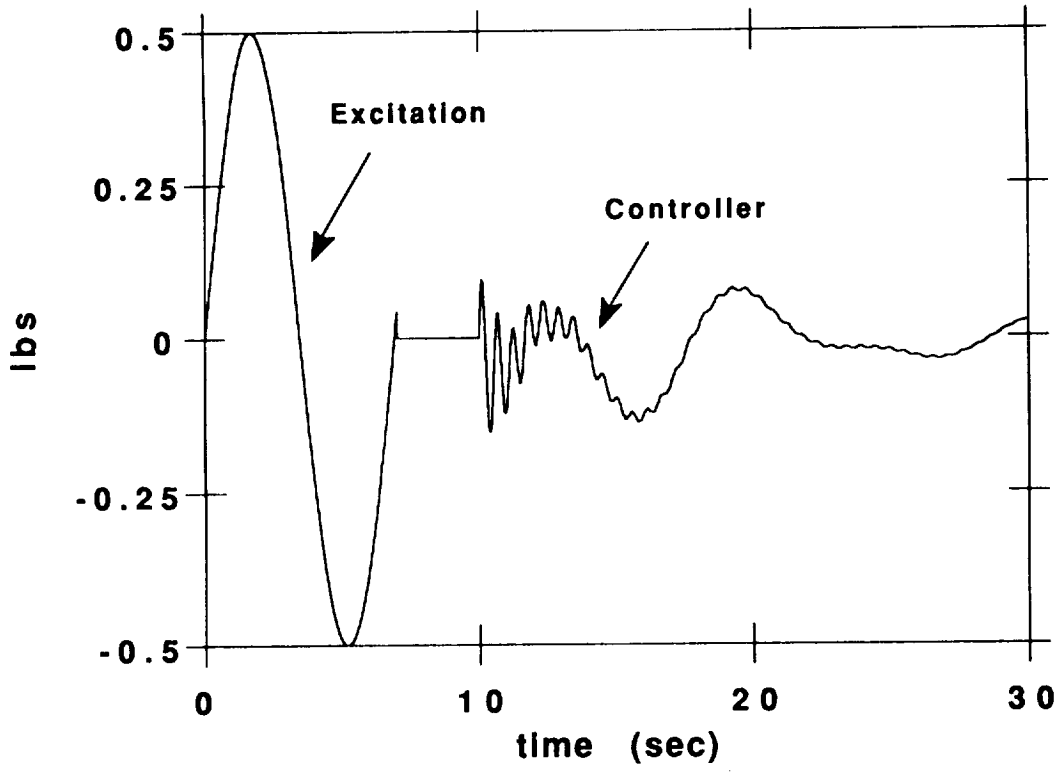


Figure 13n. Thruster #7 command time history for closed loop test with 16 state decoupled controller - CCS.

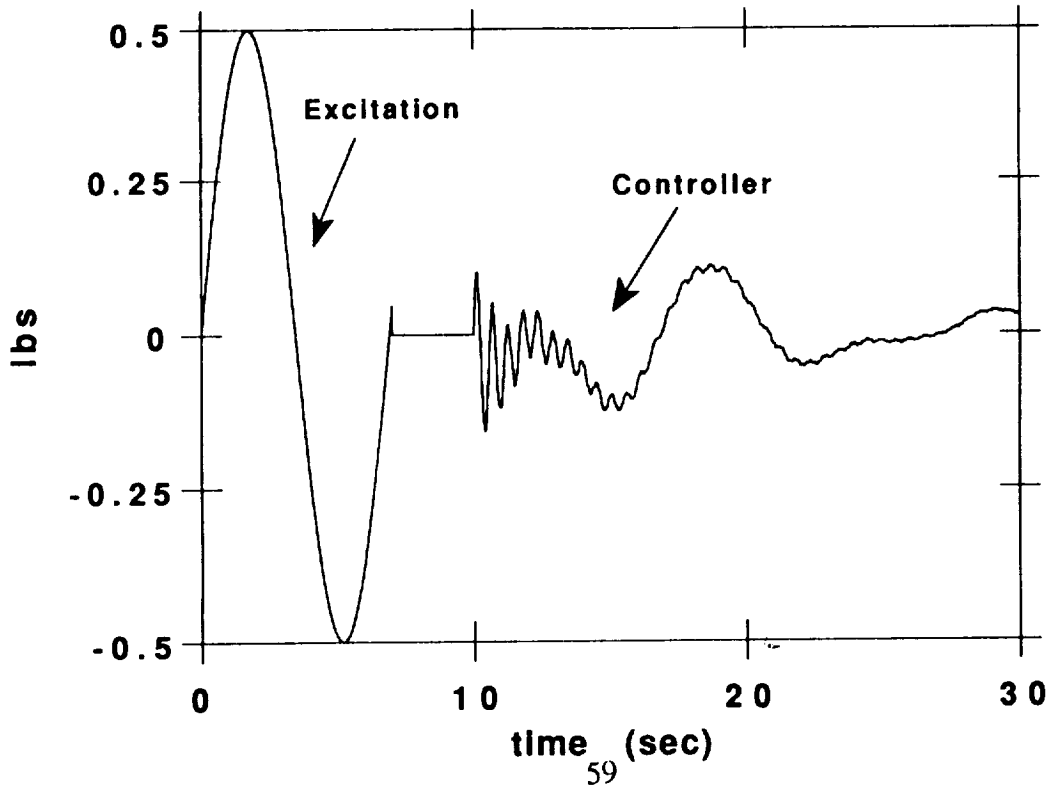


Figure 13o. Thruster #8 command time history for closed loop test with 16 state decoupled controller - SSRL VAX.

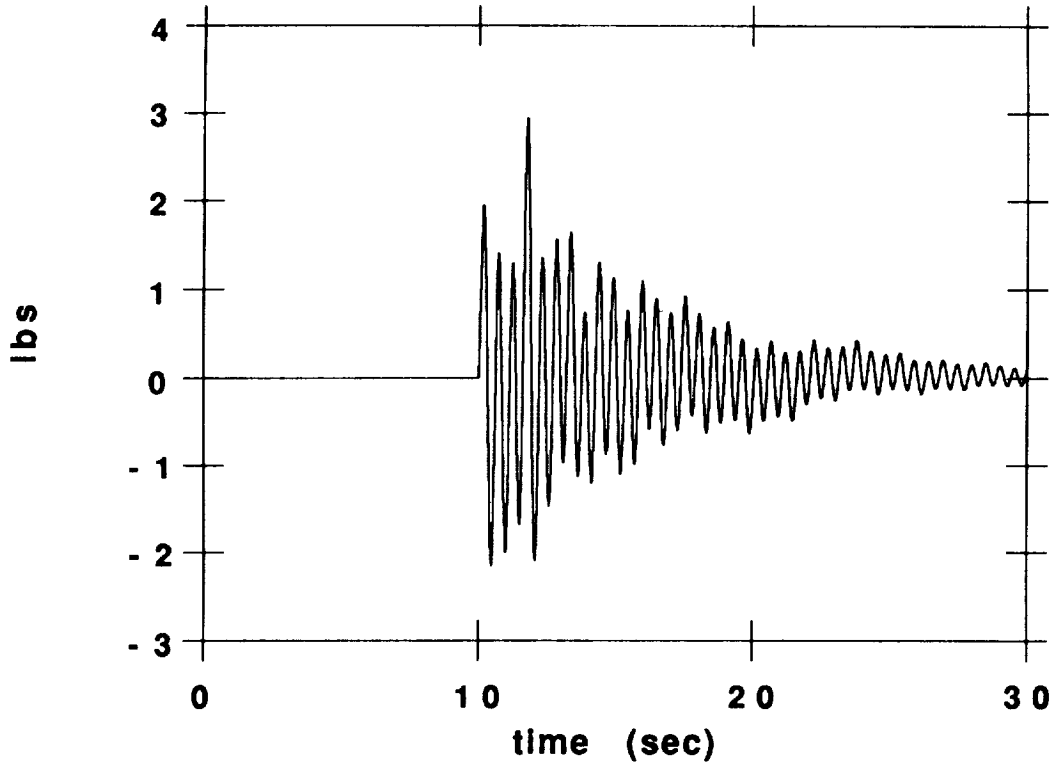


Figure 13p. Thruster #8 command time history for closed loop test with 16 state decoupled controller - CCS.

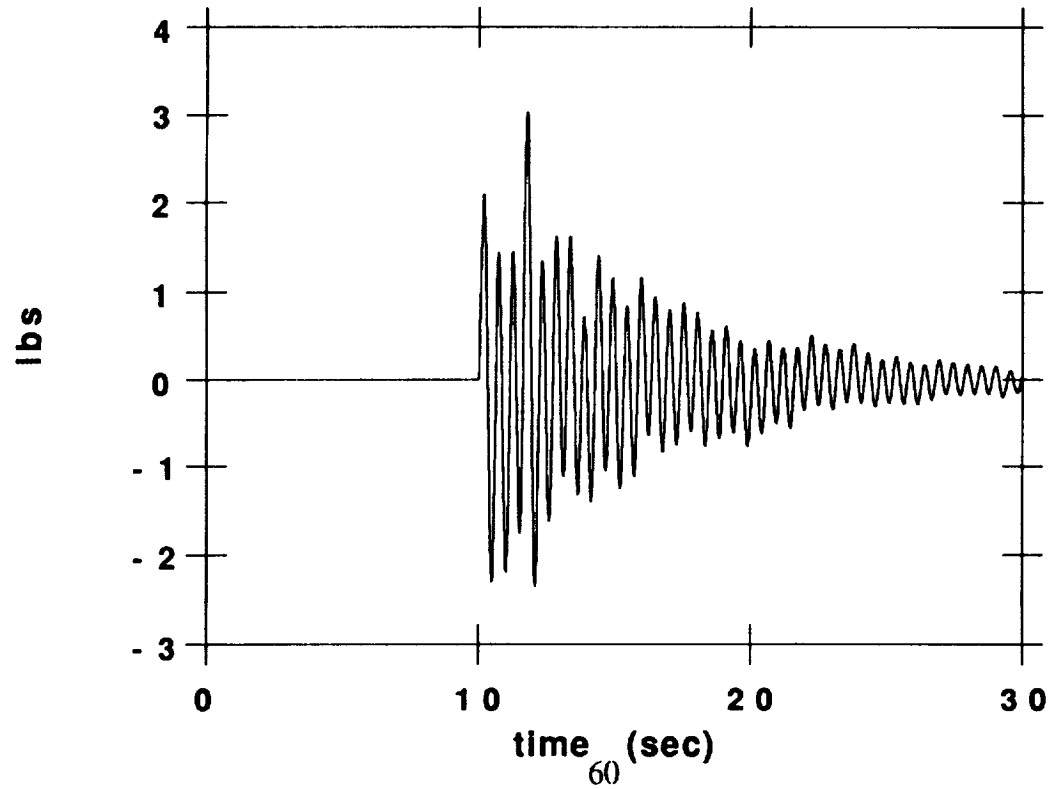


Figure 14a. Accelerometer #1 time history for closed loop test with 42 state H-infinity controller.

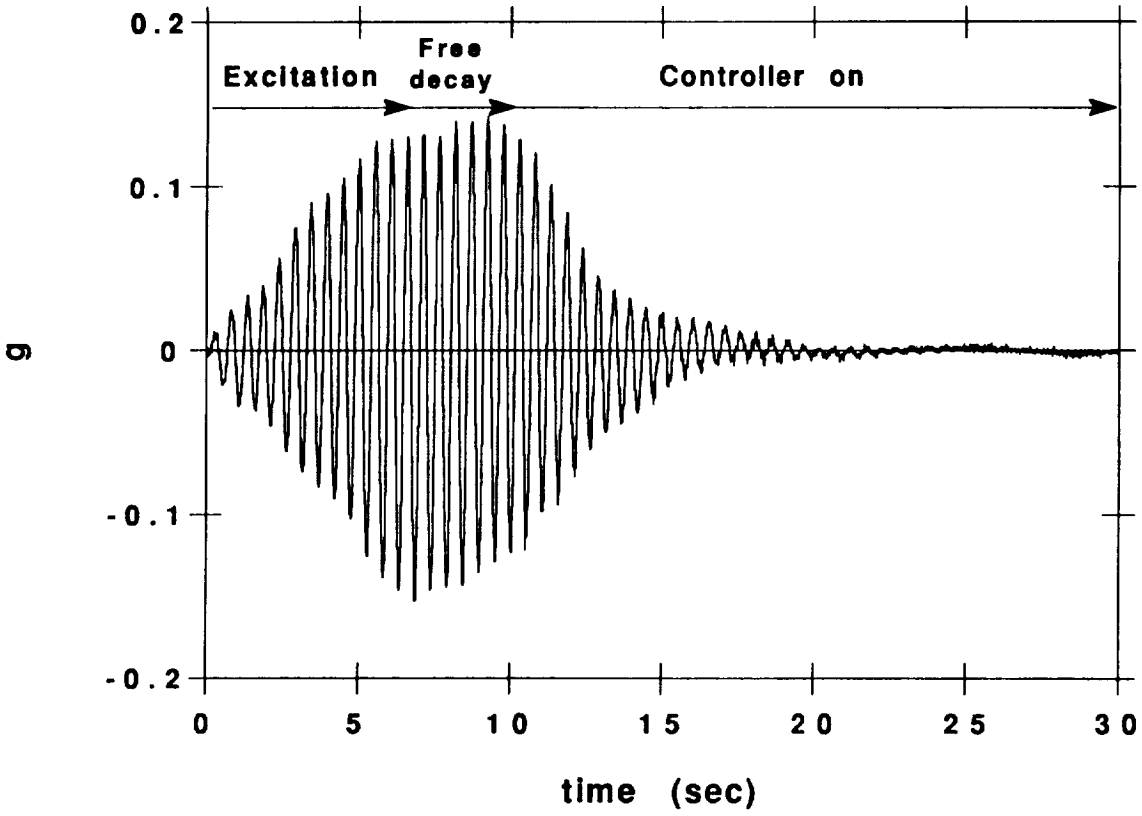


Figure 14b. Accelerometer #2 time history for closed loop test with 42 state H-infinity controller.

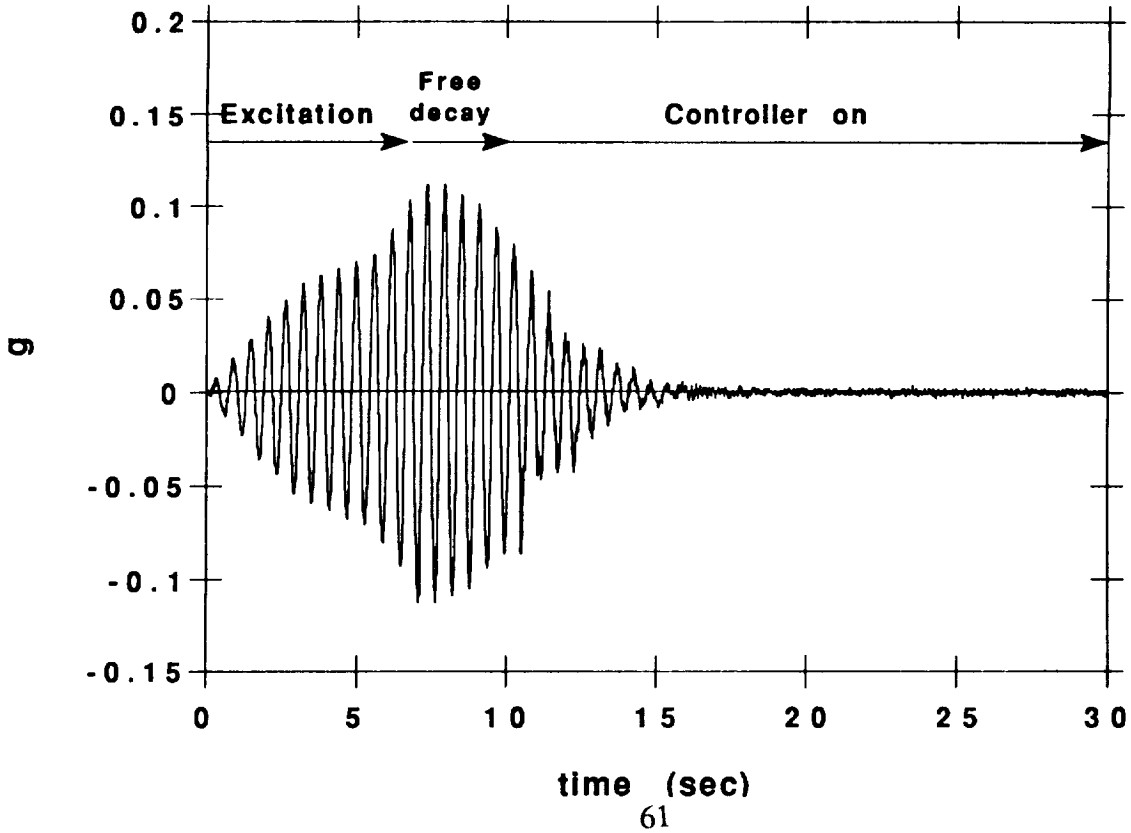


Figure 14c. Accelerometer #3 time history for closed loop test with 42 state H-infinity controller.

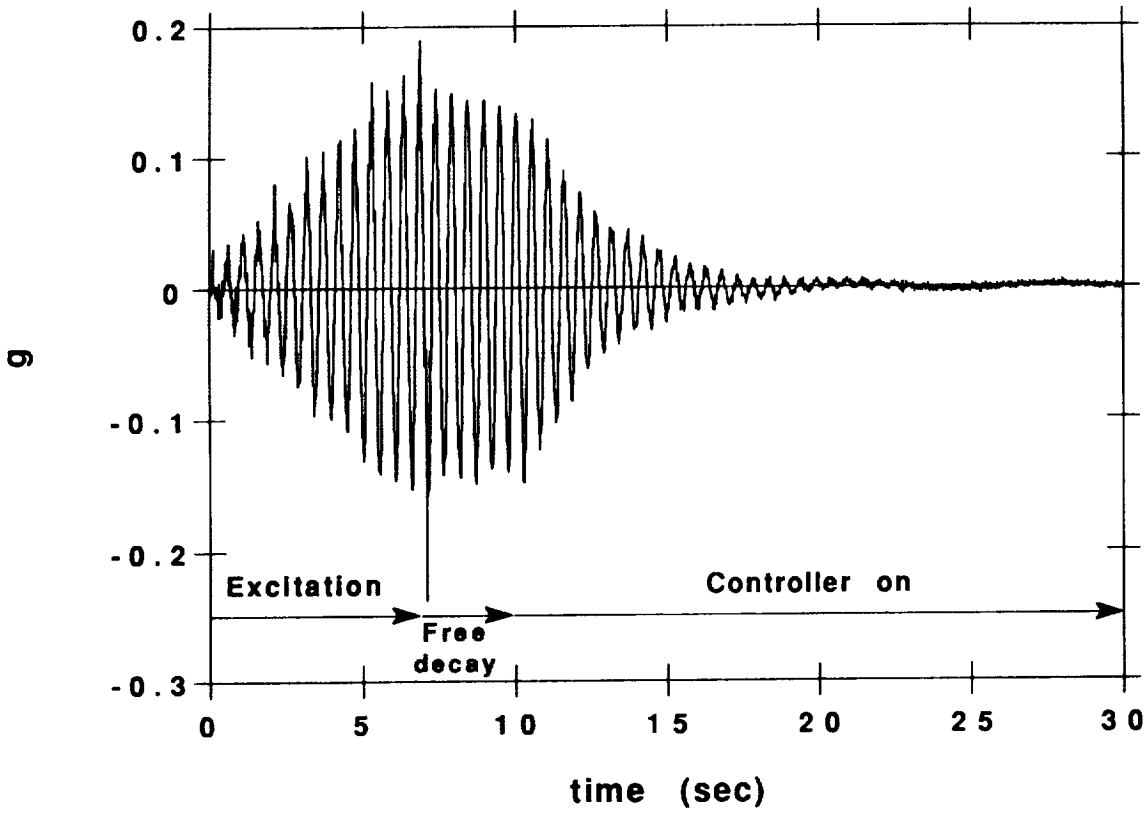


Figure 14d. Accelerometer #4 time history for closed loop test with 42 state H-infinity controller.

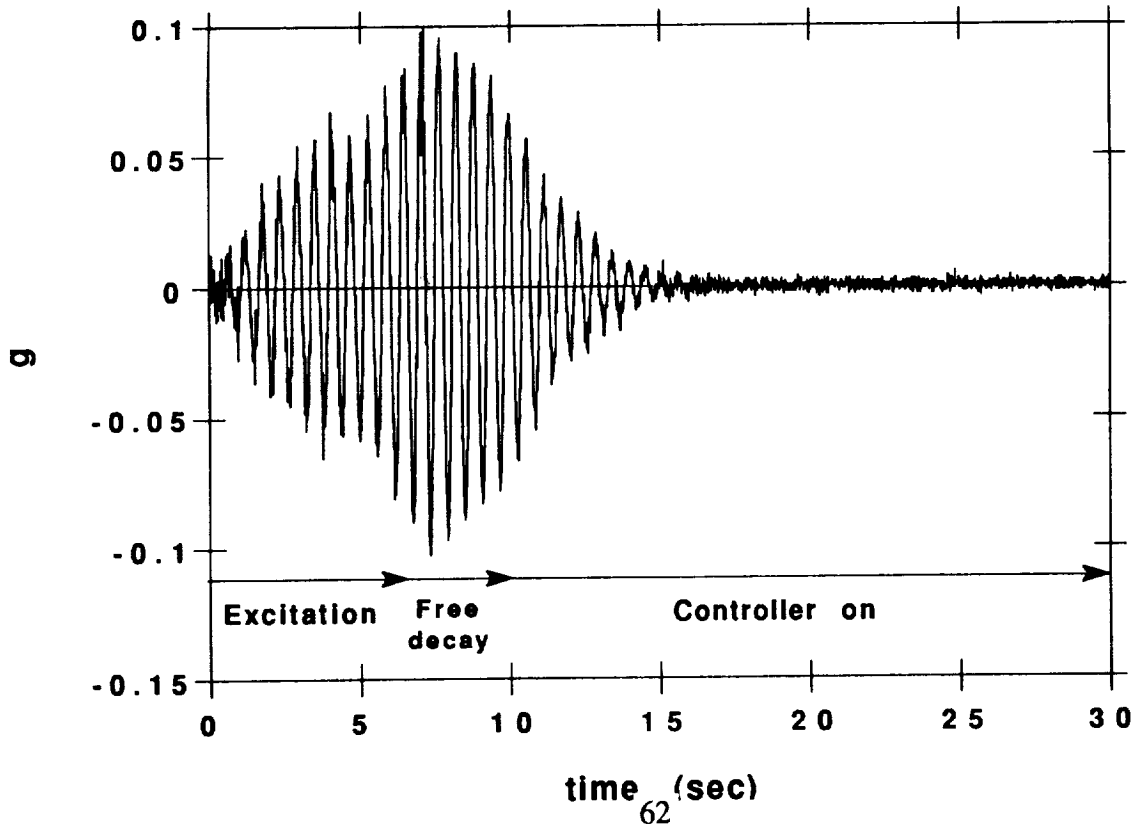


Figure 14e. Accelerometer #5 time history for closed loop test with 42 state H-infinity controller.

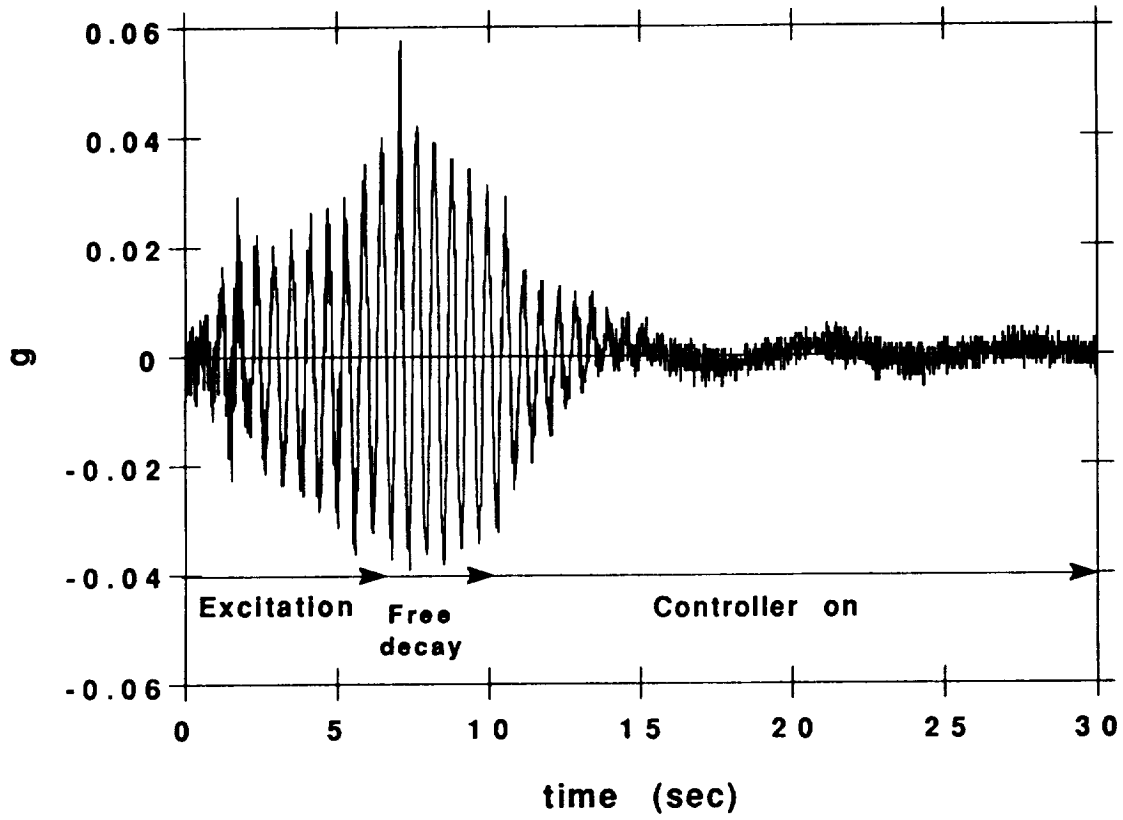


Figure 14f. Accelerometer #6 time history for closed loop test with 42 state H-infinity controller.

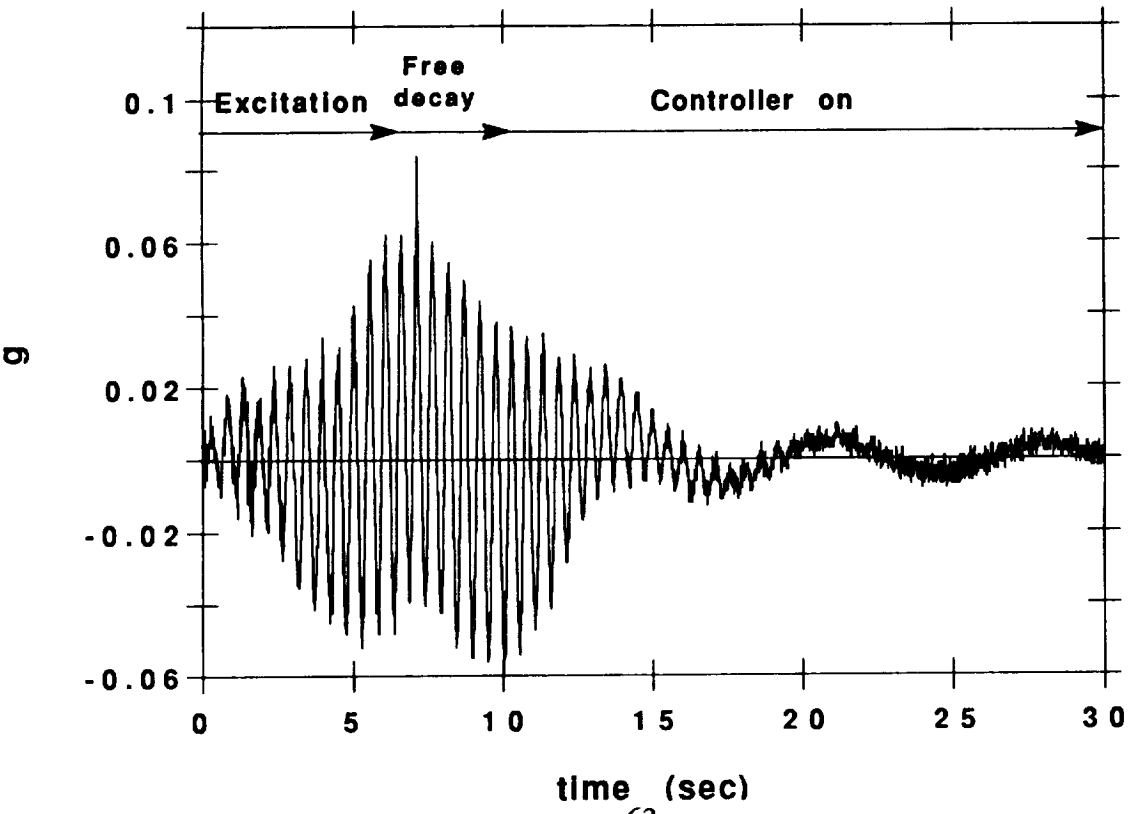


Figure 14g. Accelerometer #7 time history for closed loop test with 42 state H-infinity controller.

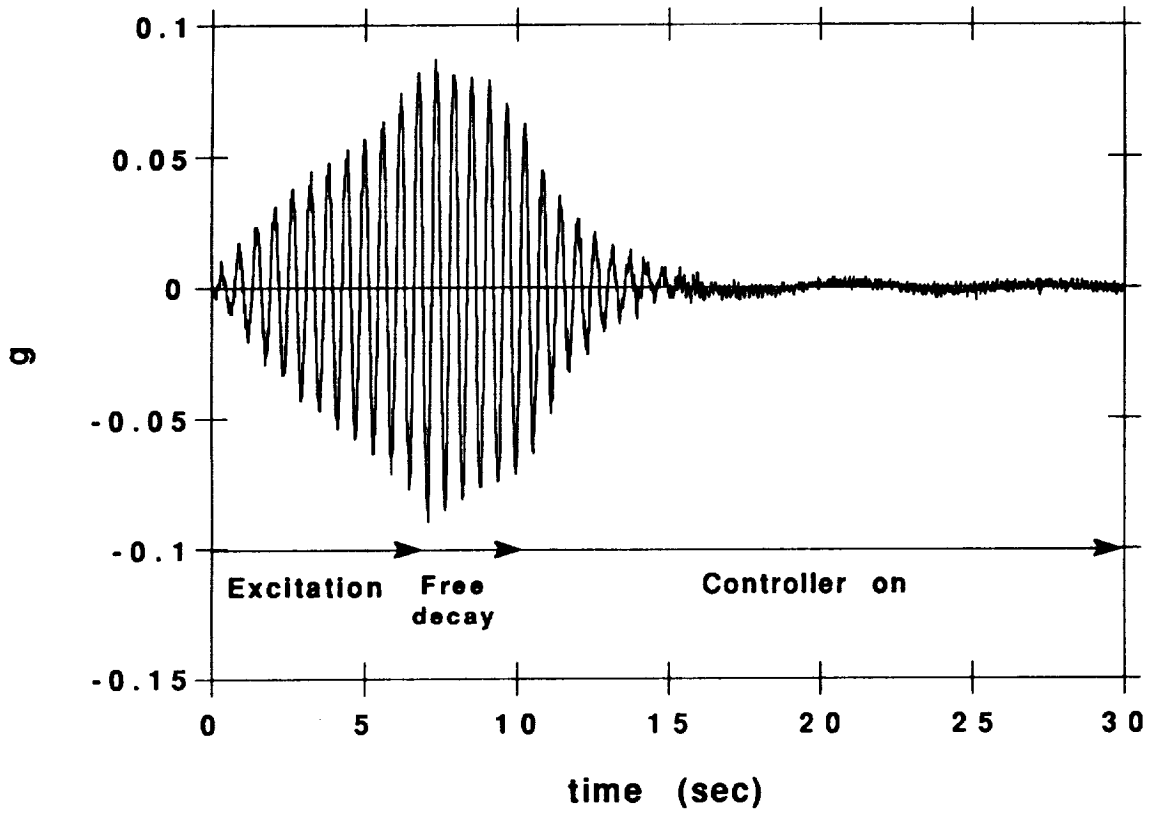


Figure 14h. Accelerometer #8 time history for closed loop test with 42 state H-infinity controller.

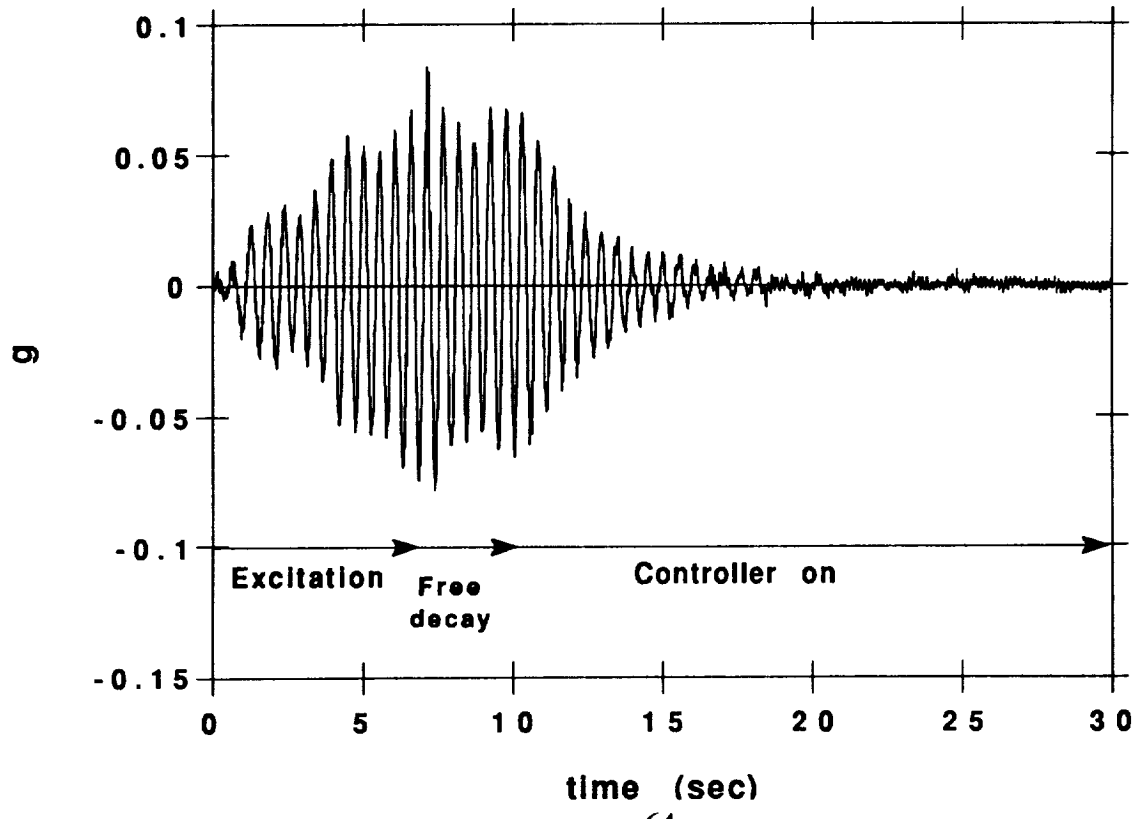


Figure 15a. Thruster #1 command time history for closed loop test with 42 state H-infinity controller.

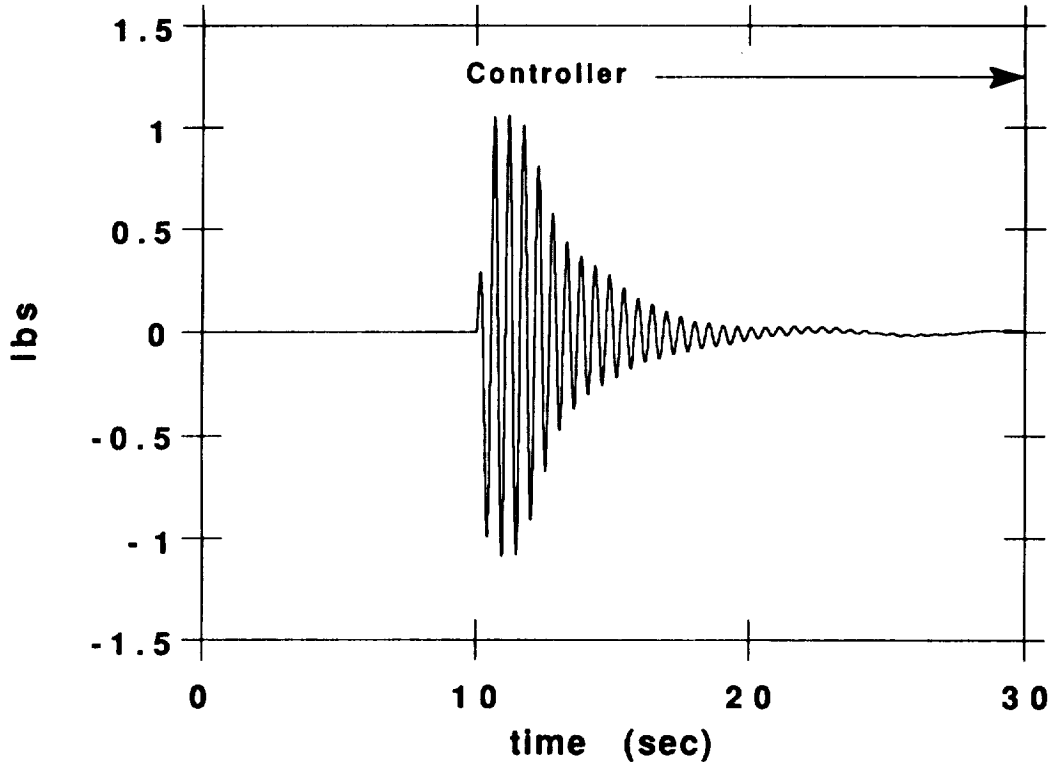


Figure 15b. Thruster #2 command time history for closed loop test with 42 state H-infinity controller.

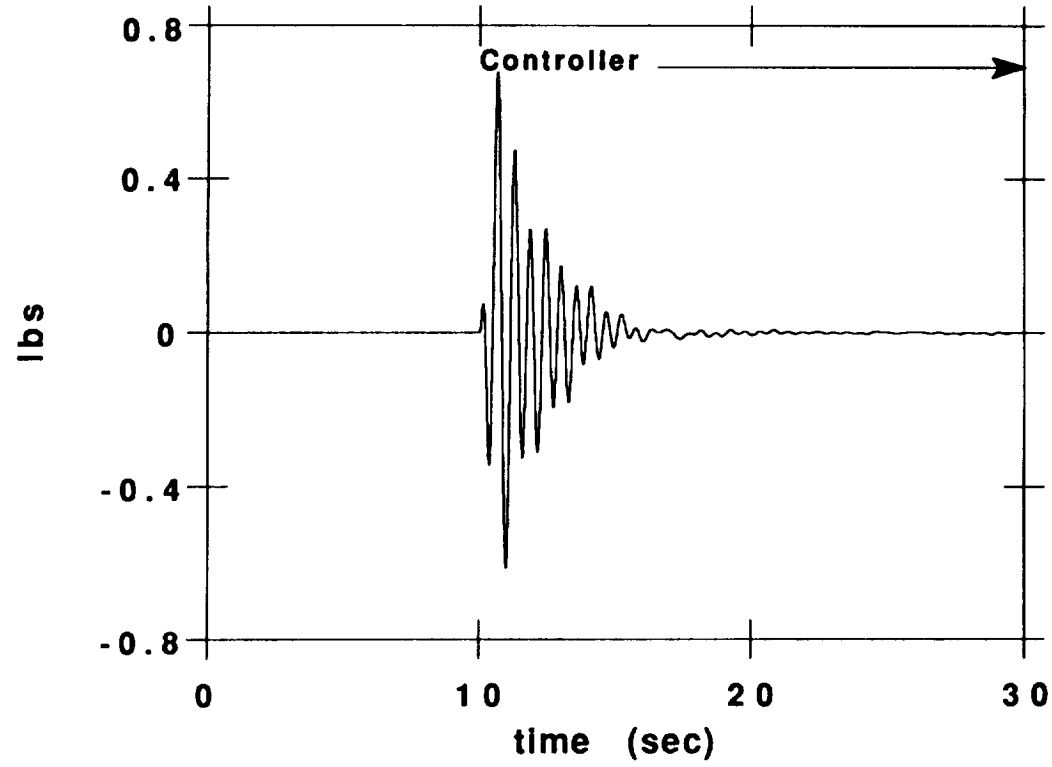


Figure 15c. Thruster #3 command time history for closed loop test with 42 state H-infinity controller.

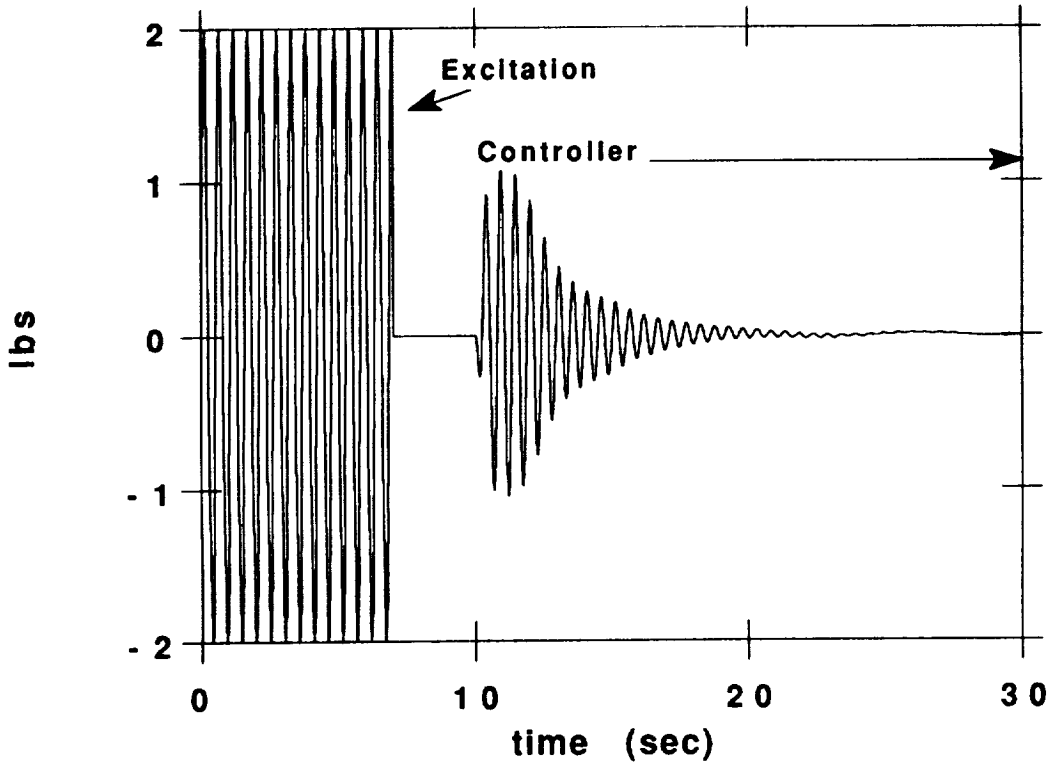


Figure 15d. Thruster #4 command time history for closed loop test with 42 state H-infinity controller.

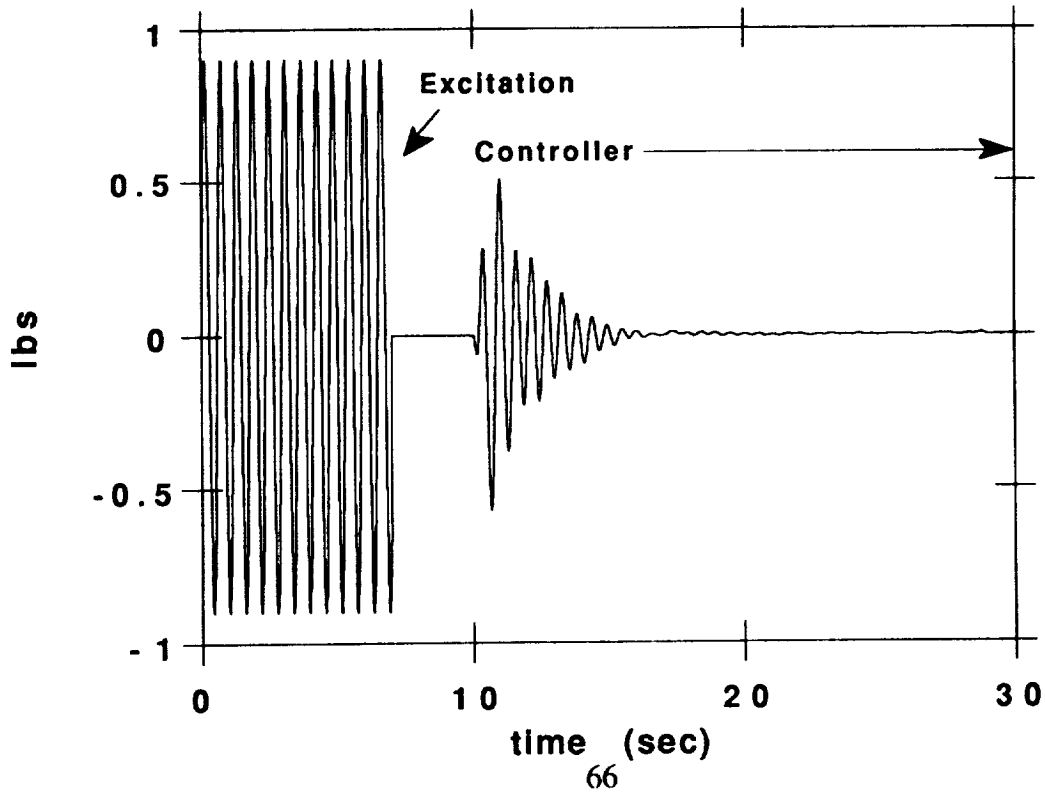


Figure 15e. Thruster #5 command time history for closed loop test with 42 state H-infinity controller.

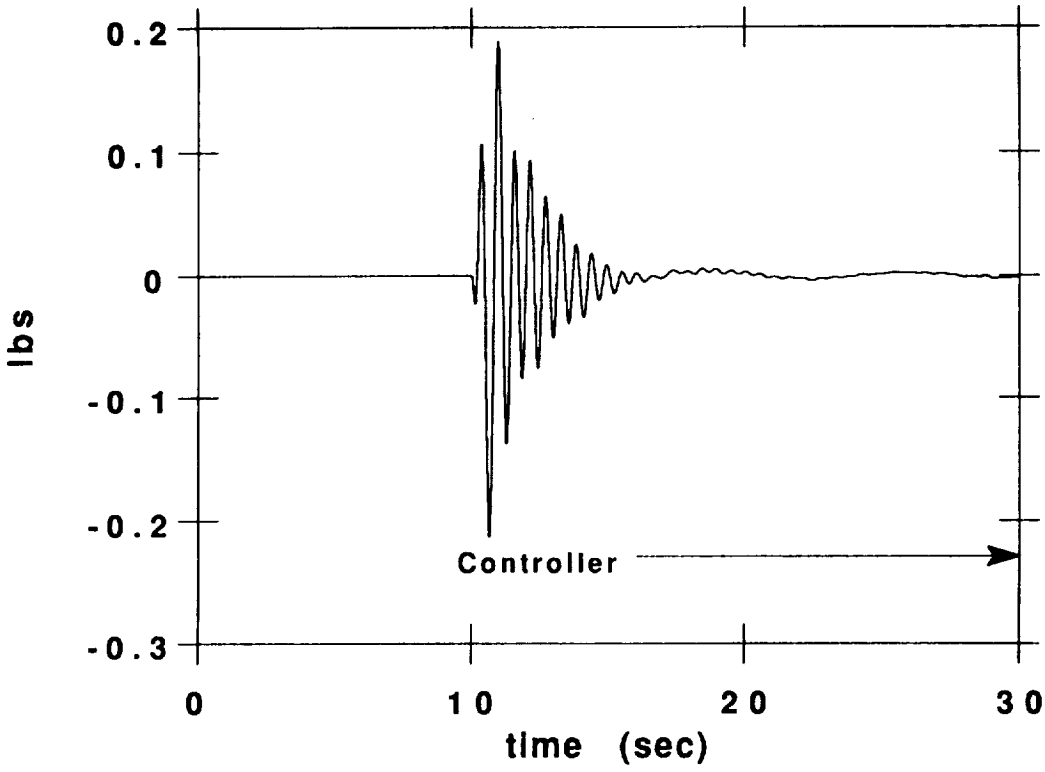


Figure 15f. Thruster #6 command time history for closed loop test with 42 state H-infinity controller.

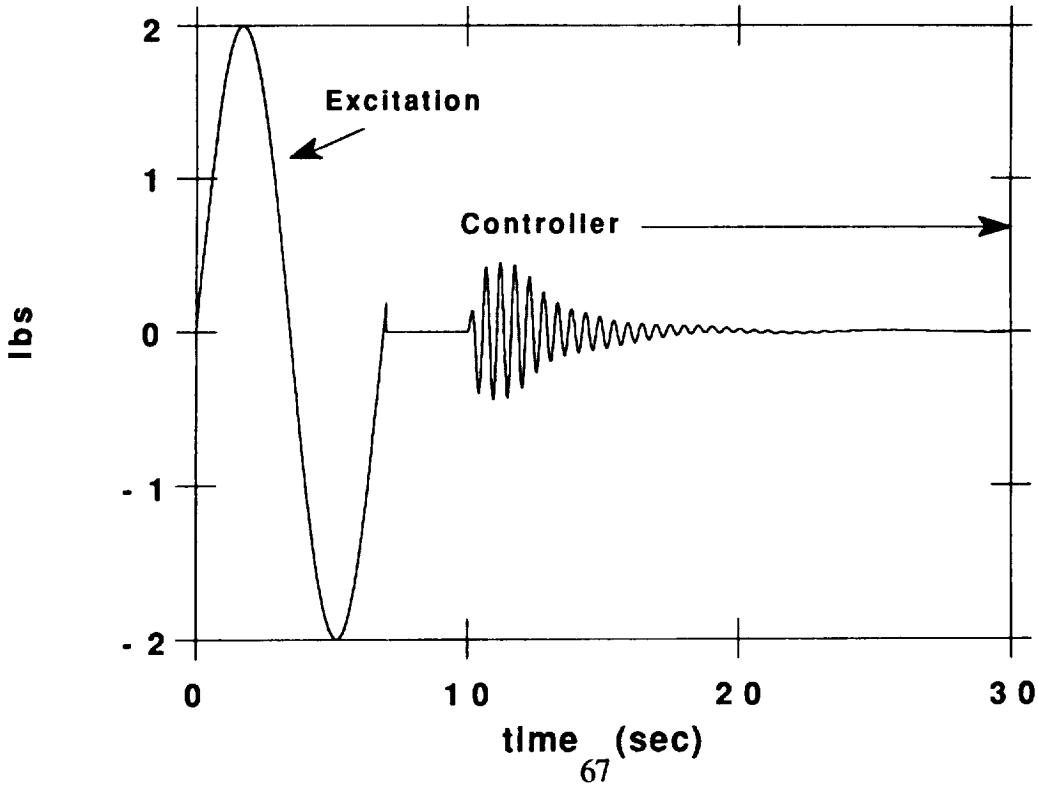


Figure 15g. Thruster #7 command time history for closed loop test with 42 state H-infinity controller.

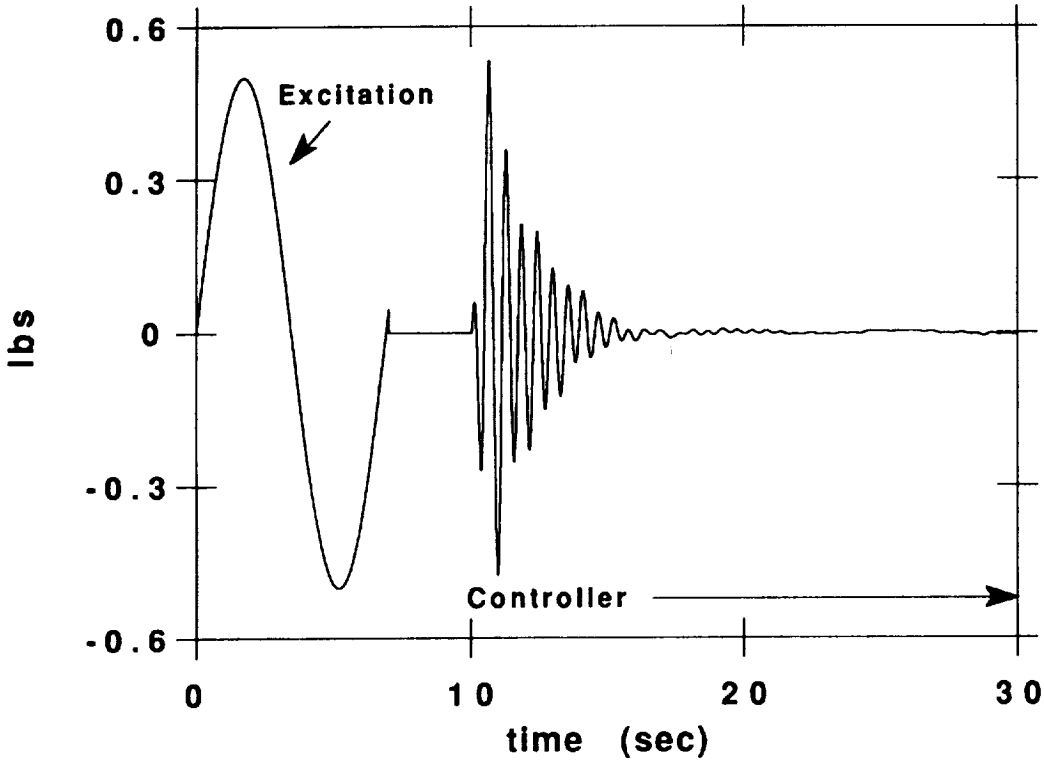


Figure 15h. Thruster #8 command time history for closed loop test with 42 state H-infinity controller.

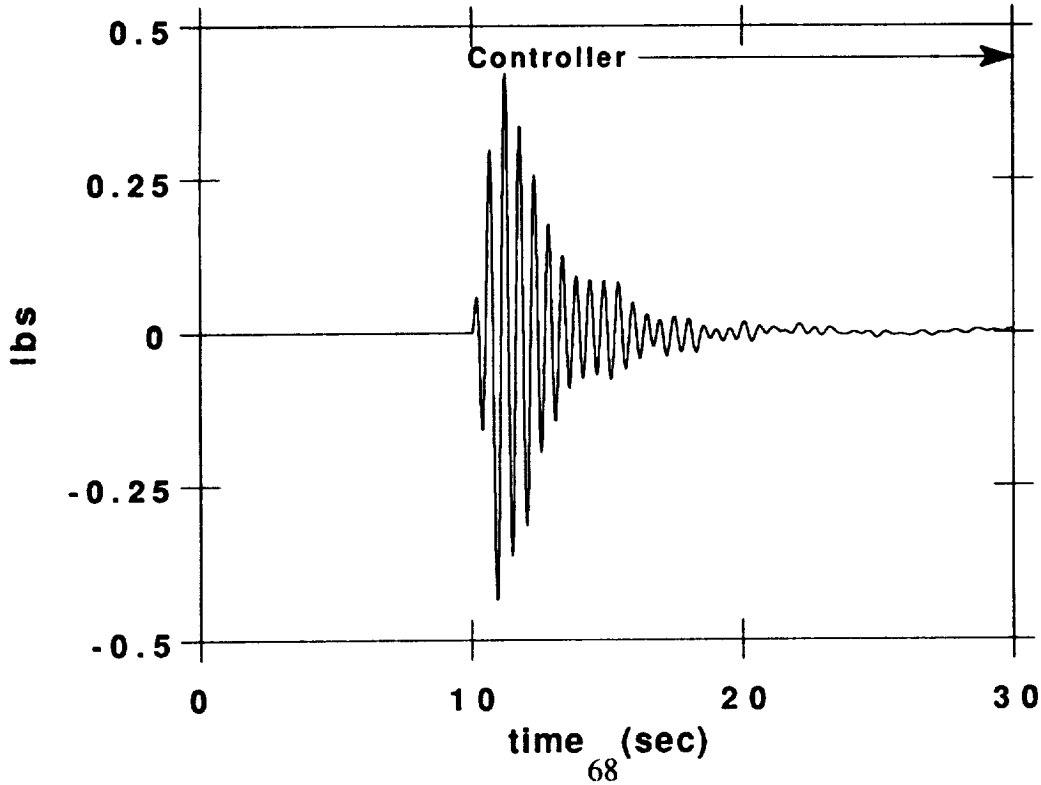


Figure 16a. Accelerometer #1 time history for closed loop test with 60 state H-infinity controller.

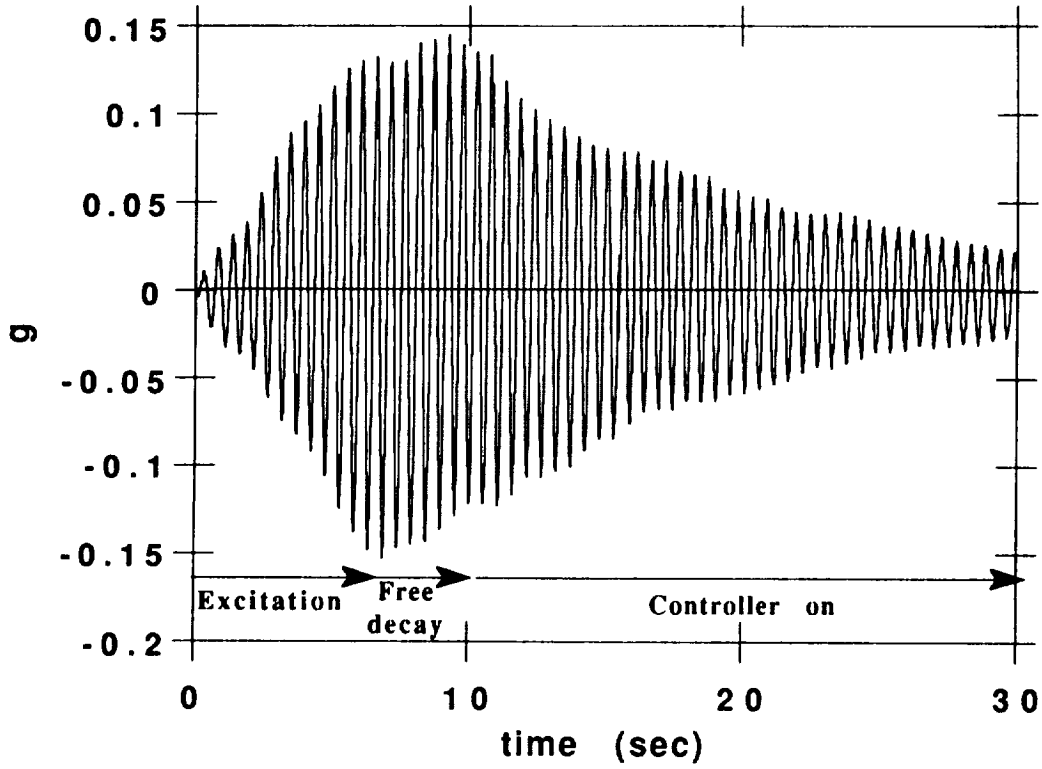


Figure 16b. Accelerometer #2 time history for closed loop test with 60 state H-infinity controller.

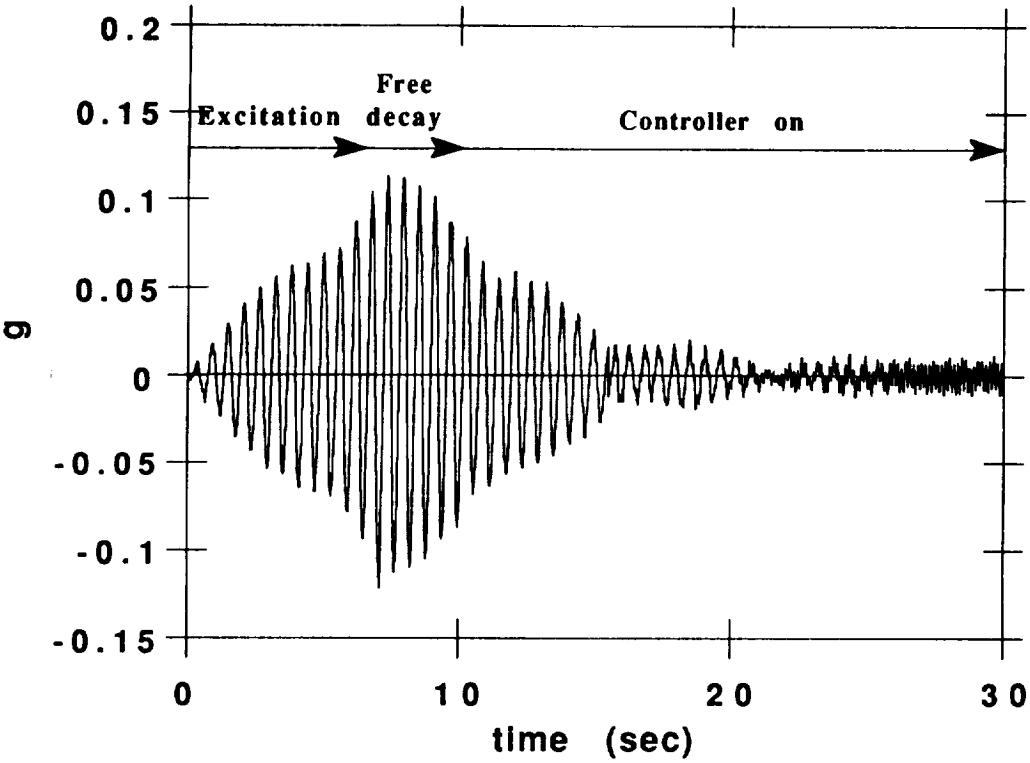


Figure 16c. Accelerometer #3 time history for closed loop test with 60 state H-infinity controller.

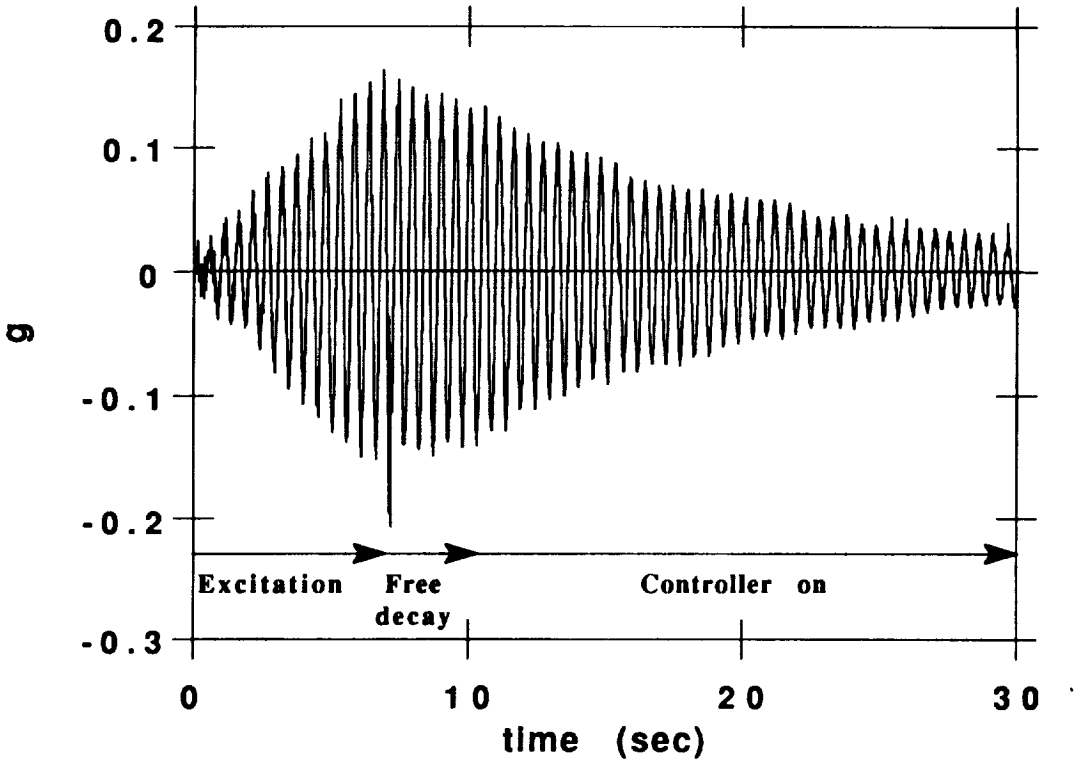


Figure 16d. Accelerometer #4 time history for closed loop test with 60 state H-infinity controller.

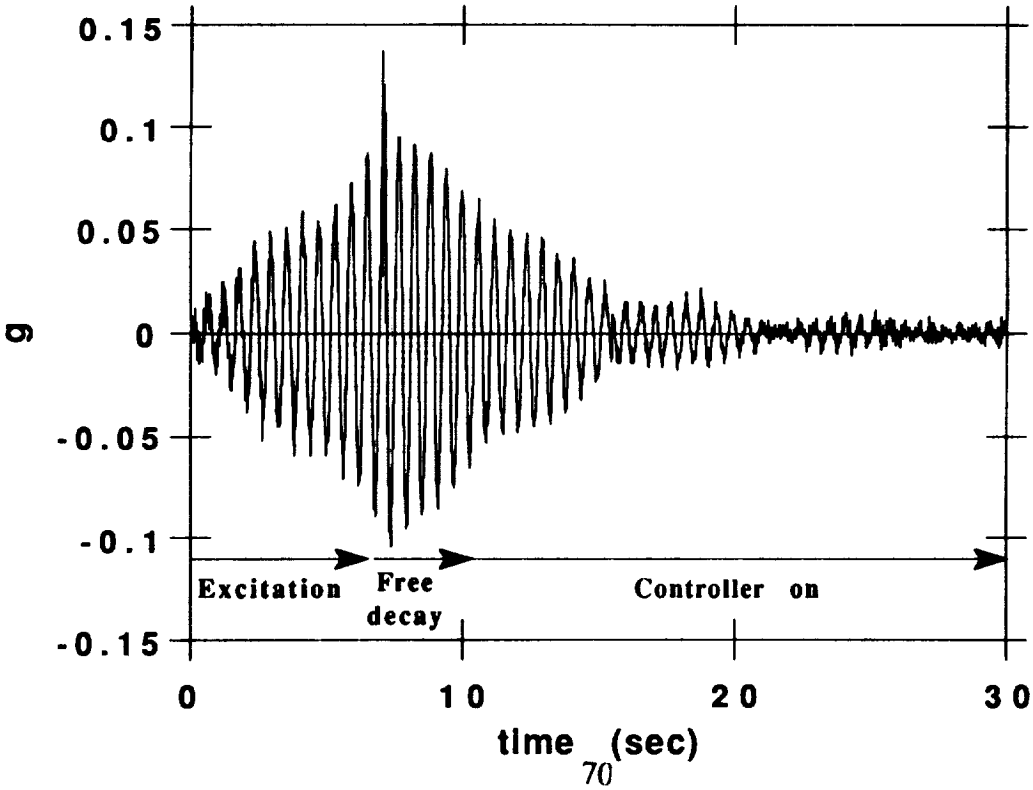


Figure 16e. Accelerometer #5 time history for closed loop test with 60 state H-infinity controller.

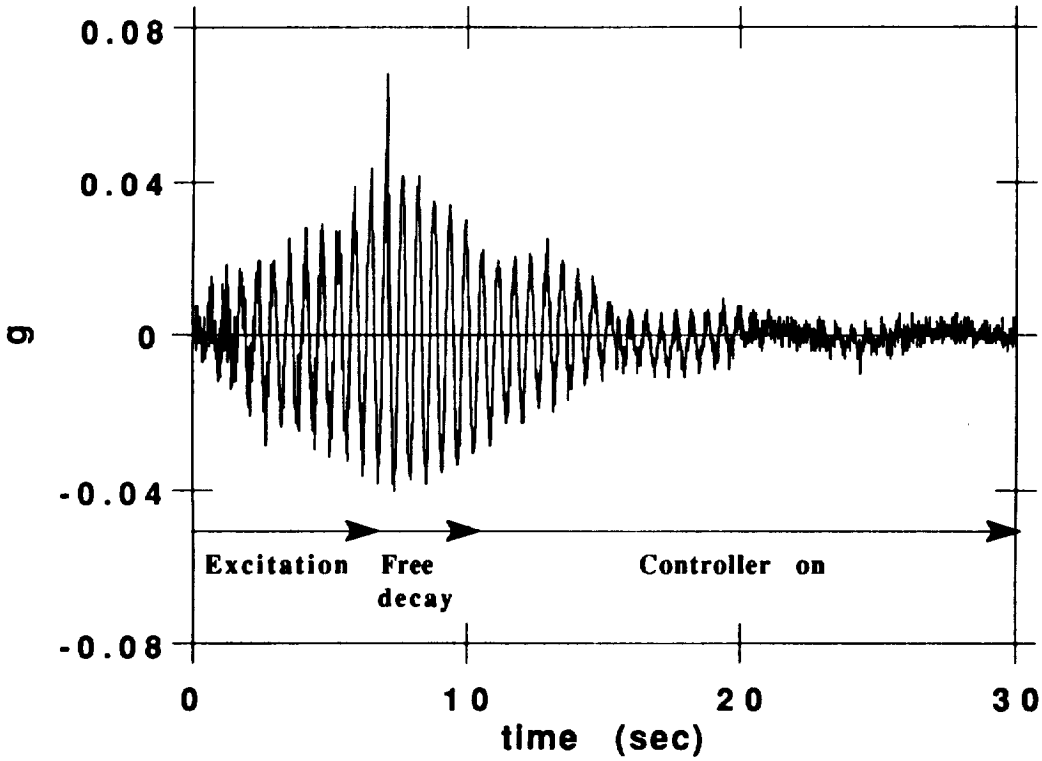


Figure 16f. Accelerometer #6 time history for closed loop test with 60 state H-infinity controller.

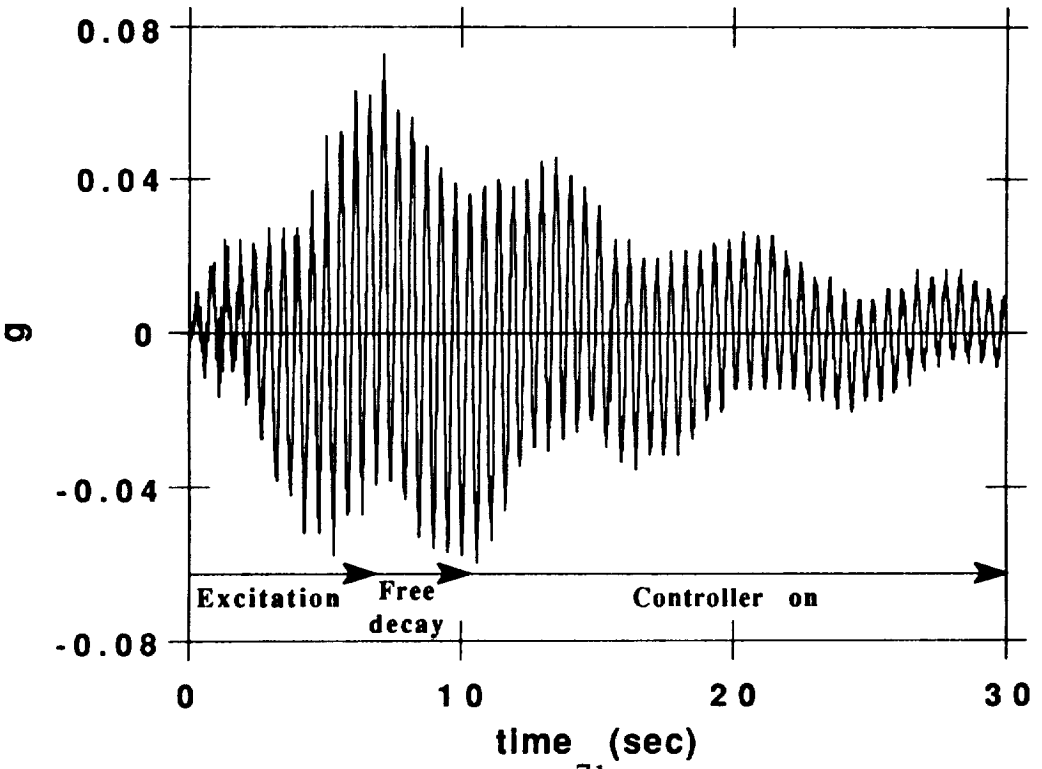


Figure 16g. Accelerometer #7 time history for closed loop test with 60 state H-infinity controller.

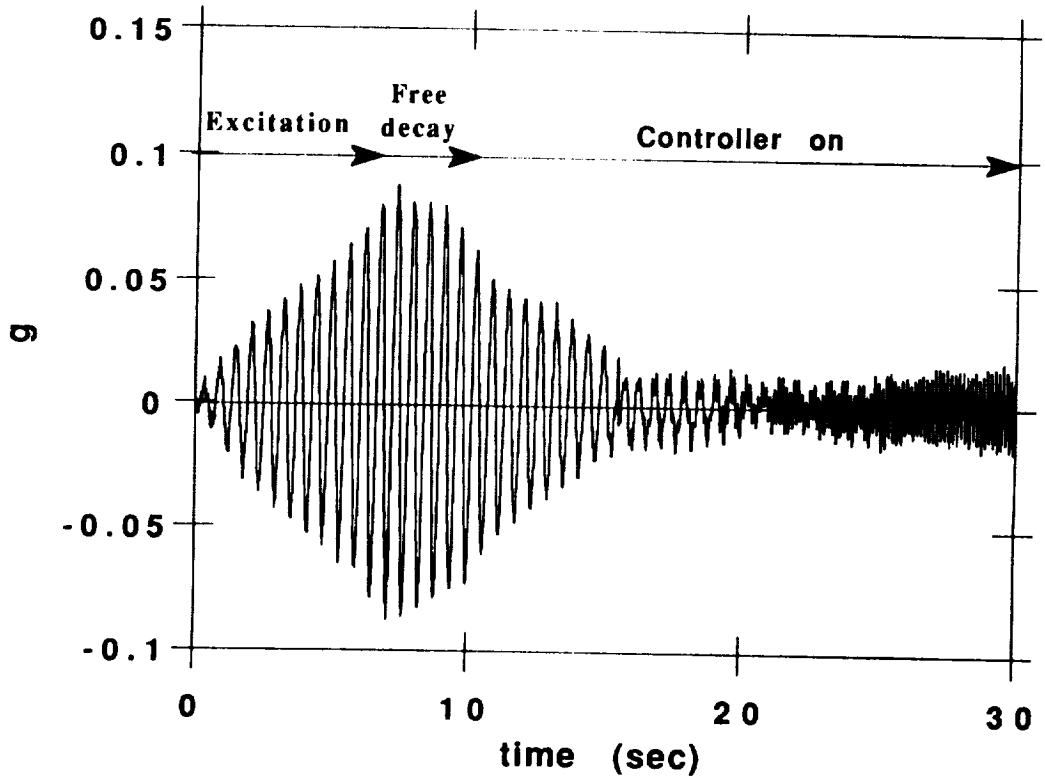


Figure 16h. Accelerometer #8 time history for closed loop test with 60 state H-infinity controller.

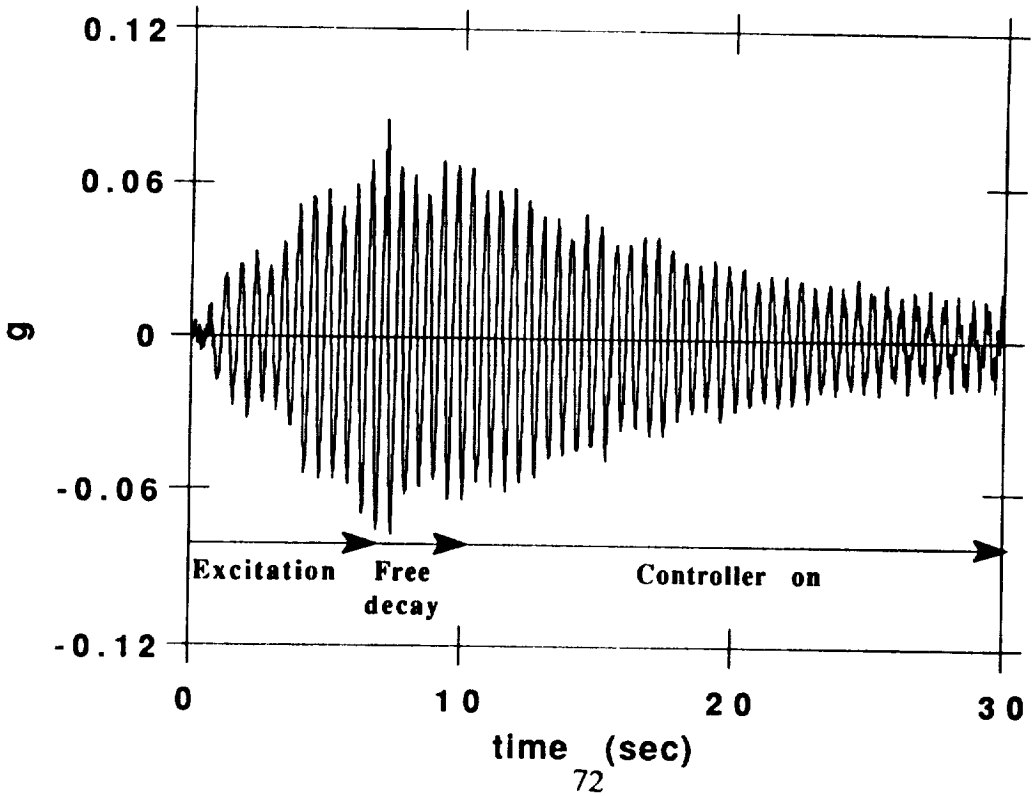


Figure 17a. Thruster #1 command time history for closed loop test with 60 state H-infinity controller.

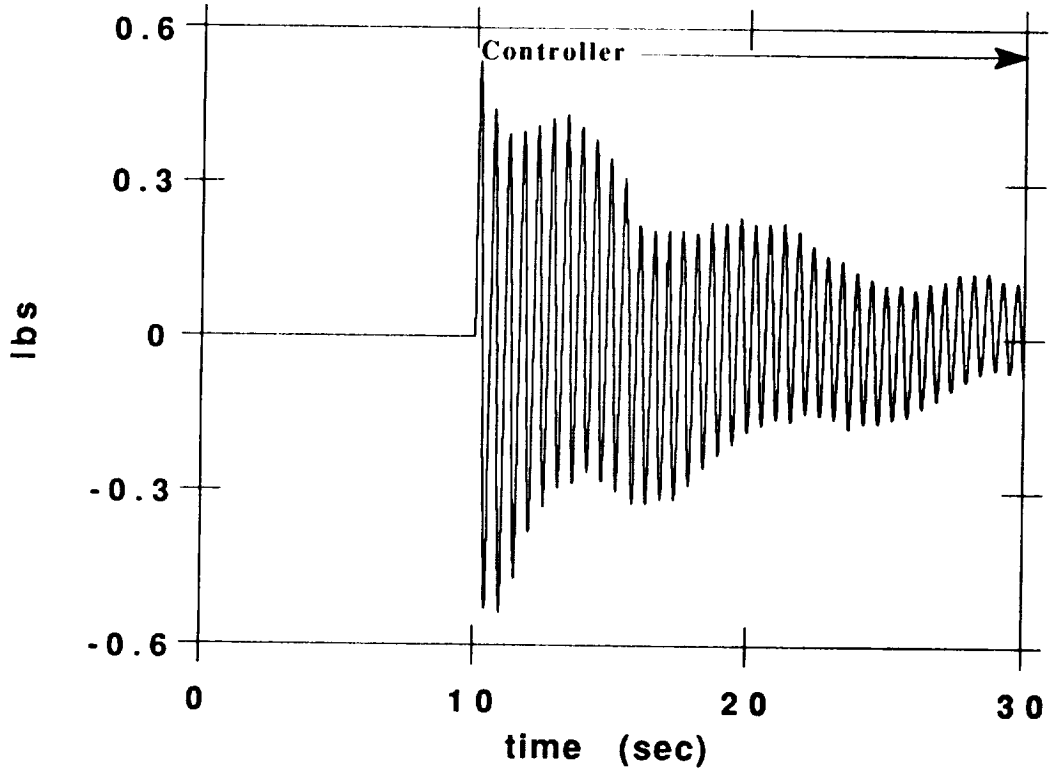


Figure 17b. Thruster #2 command time history for closed loop test with 60 state H-infinity controller.

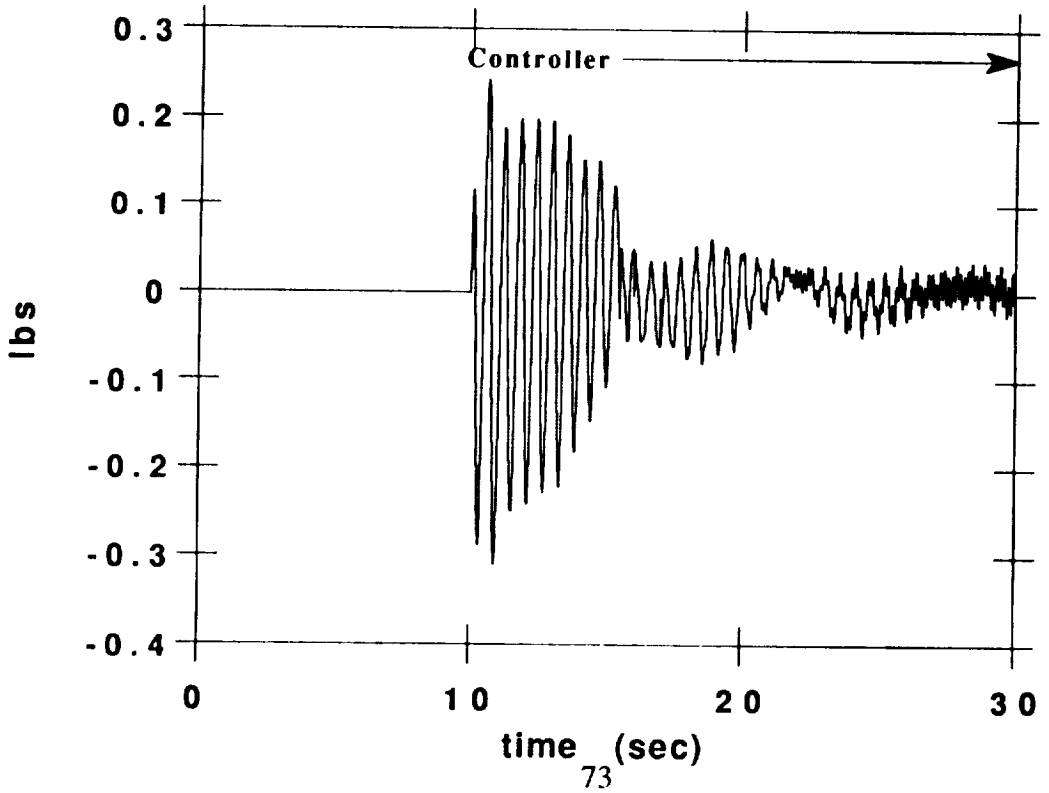


Figure 17c. Thruster #3 command time history for closed loop test with 60 state H-infinity controller.

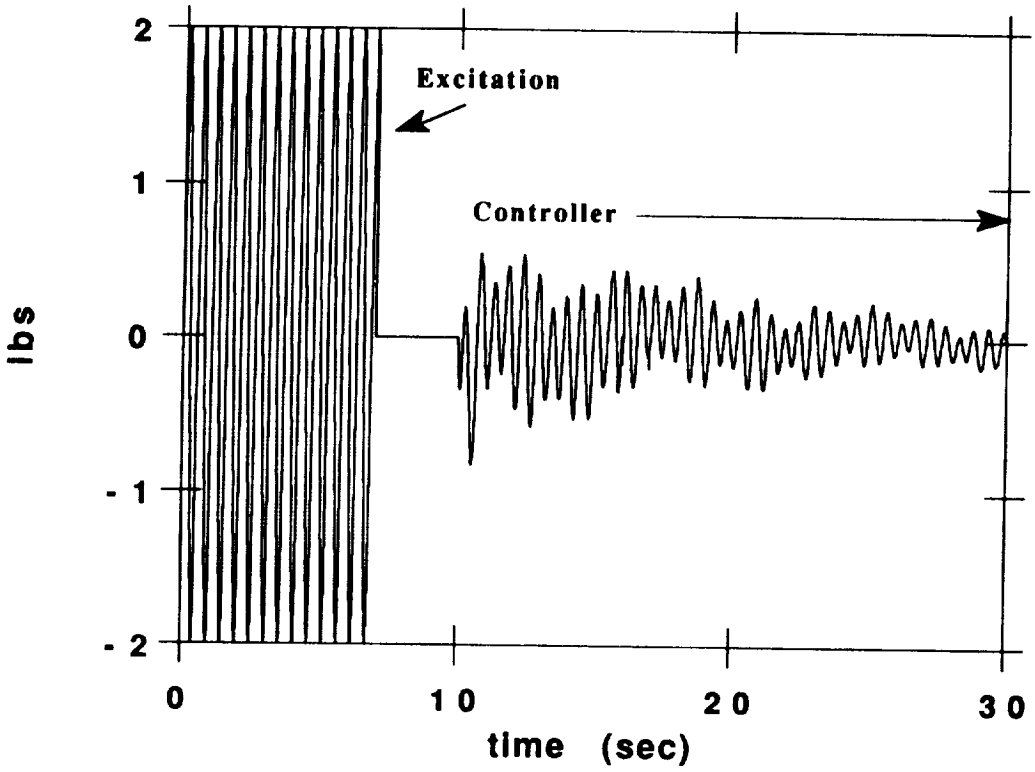


Figure 17d. Thruster #4 command time history for closed loop test with 60 state H-infinity controller.

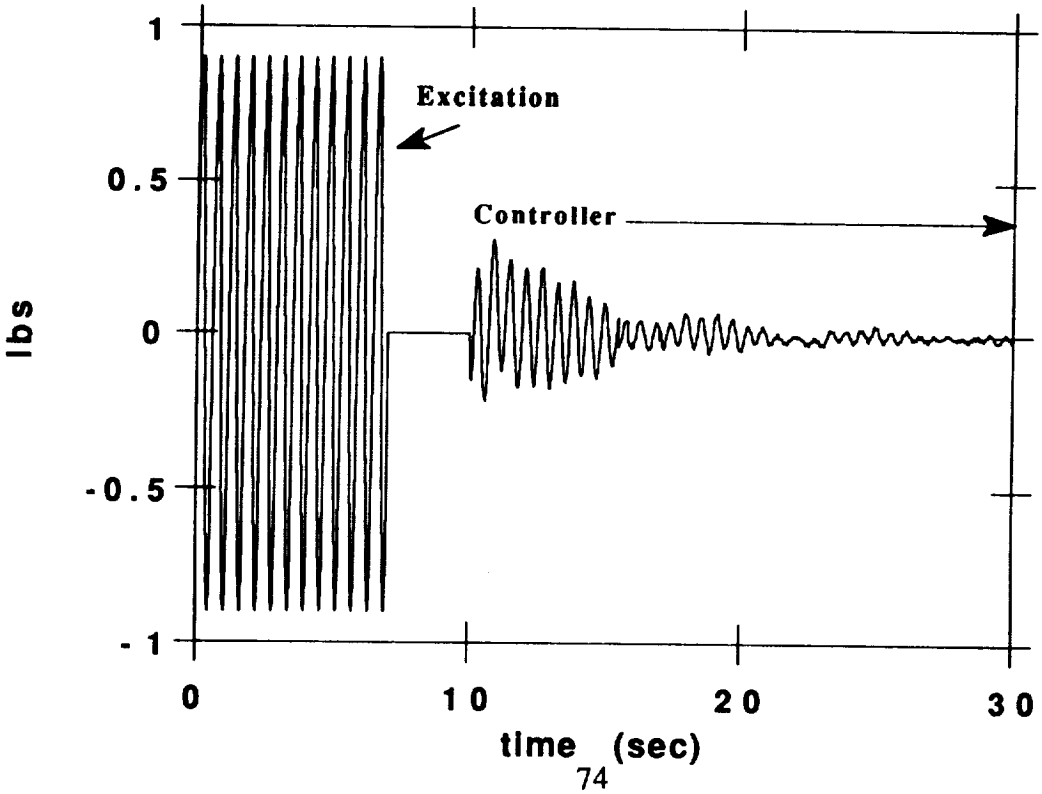


Figure 17e. Thruster #5 command time history for closed loop test with 60 state H-infinity controller.

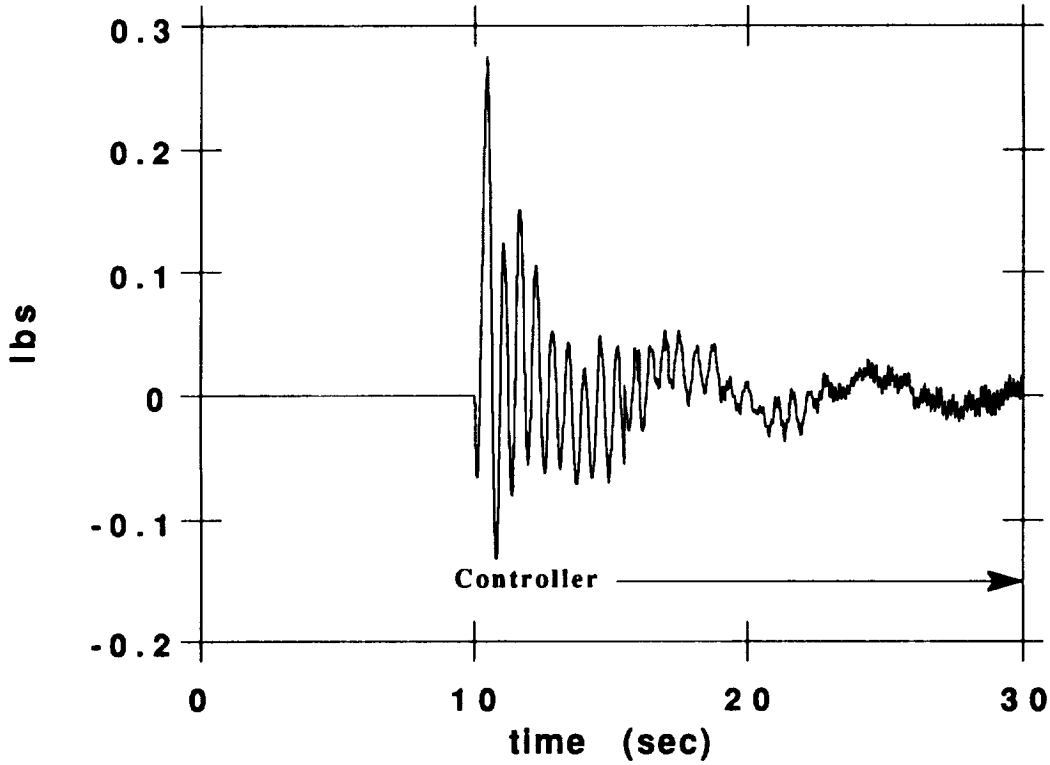


Figure 17f. Thruster #6 command time history for closed loop test with 60 state H-infinity controller.

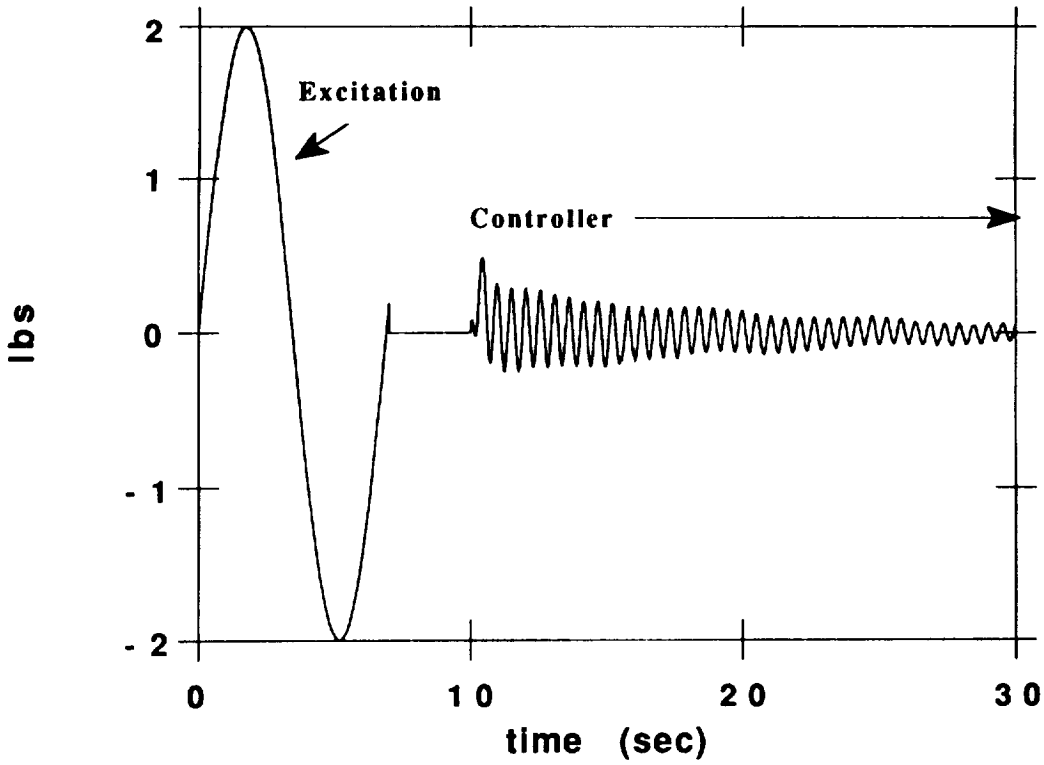


Figure 17g. Thruster #7 command time history for closed loop test with 60 state H-infinity controller.

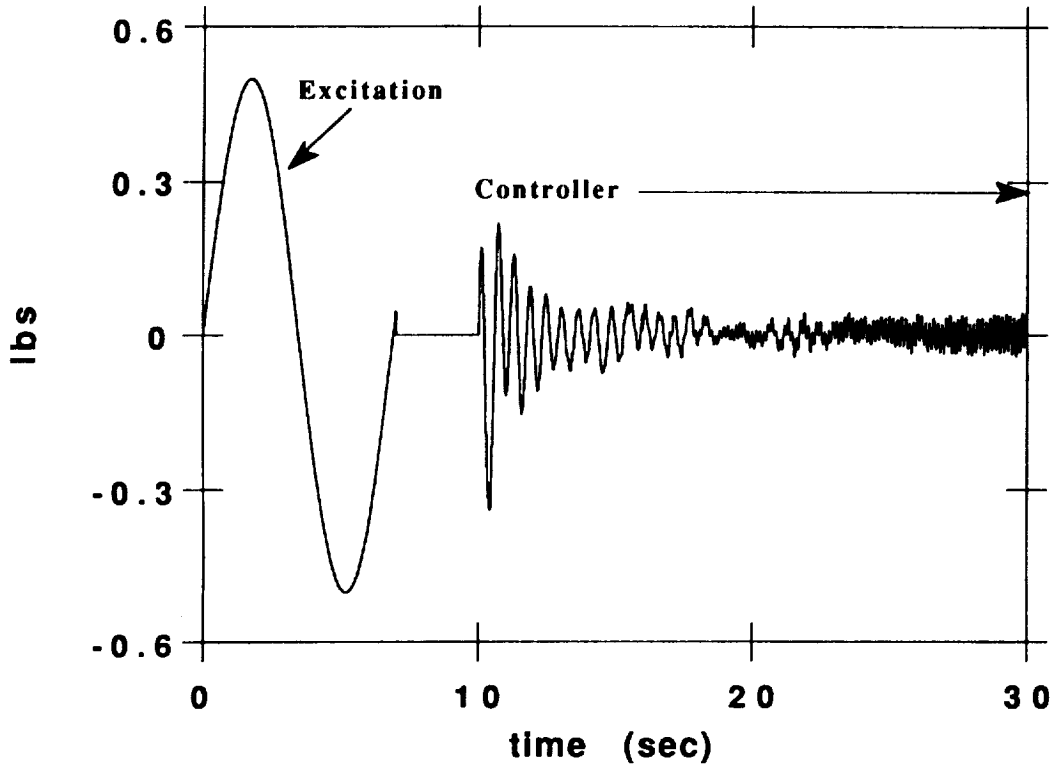


Figure 17h. Thruster #8 command time history for closed loop test with 60 state H-infinity controller.

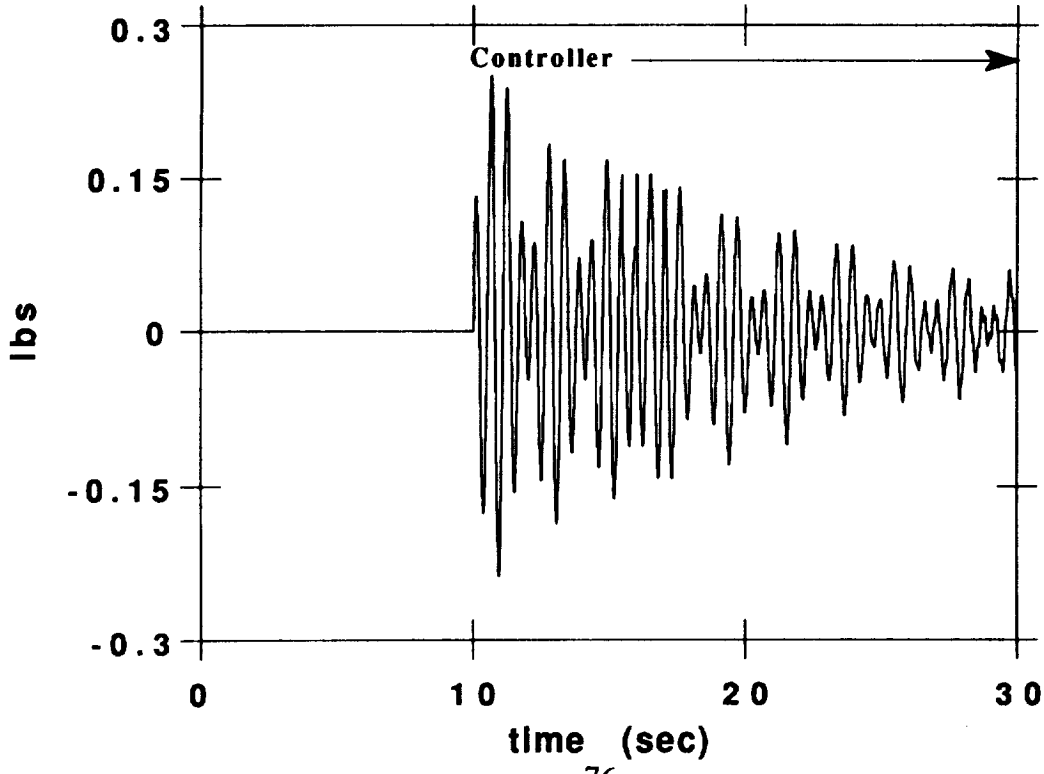
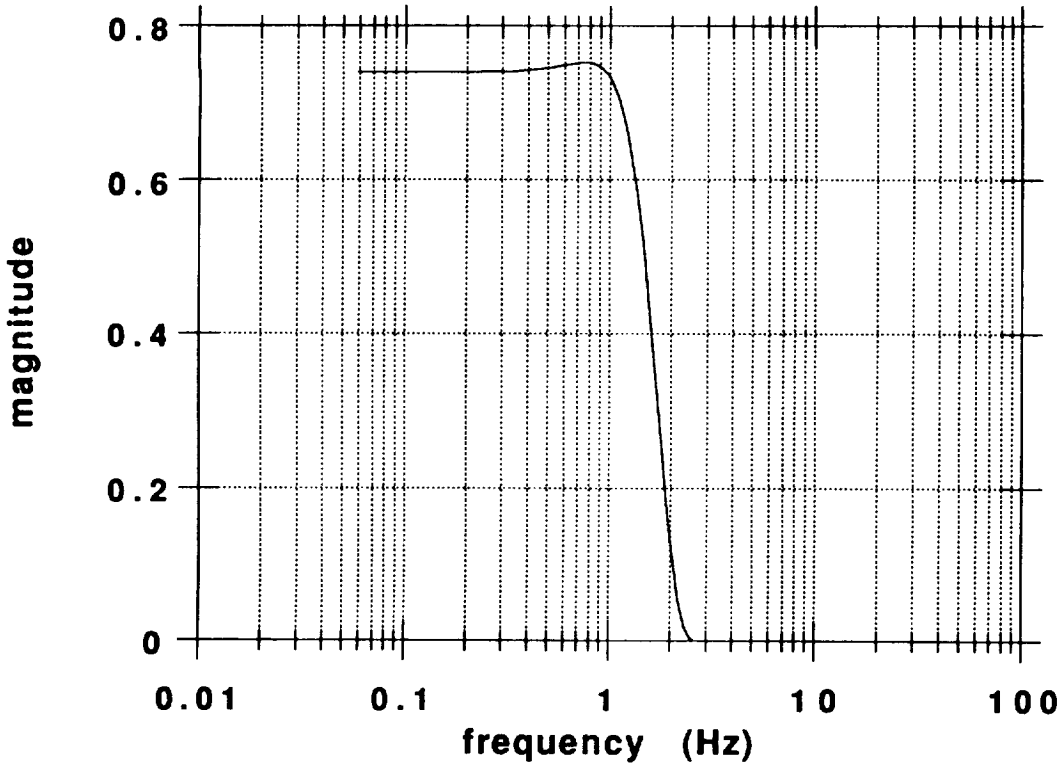


Figure 18a. Magnitude and phase plots of frequency response of RIU digital filter #2, sample rate = 60 Hz.



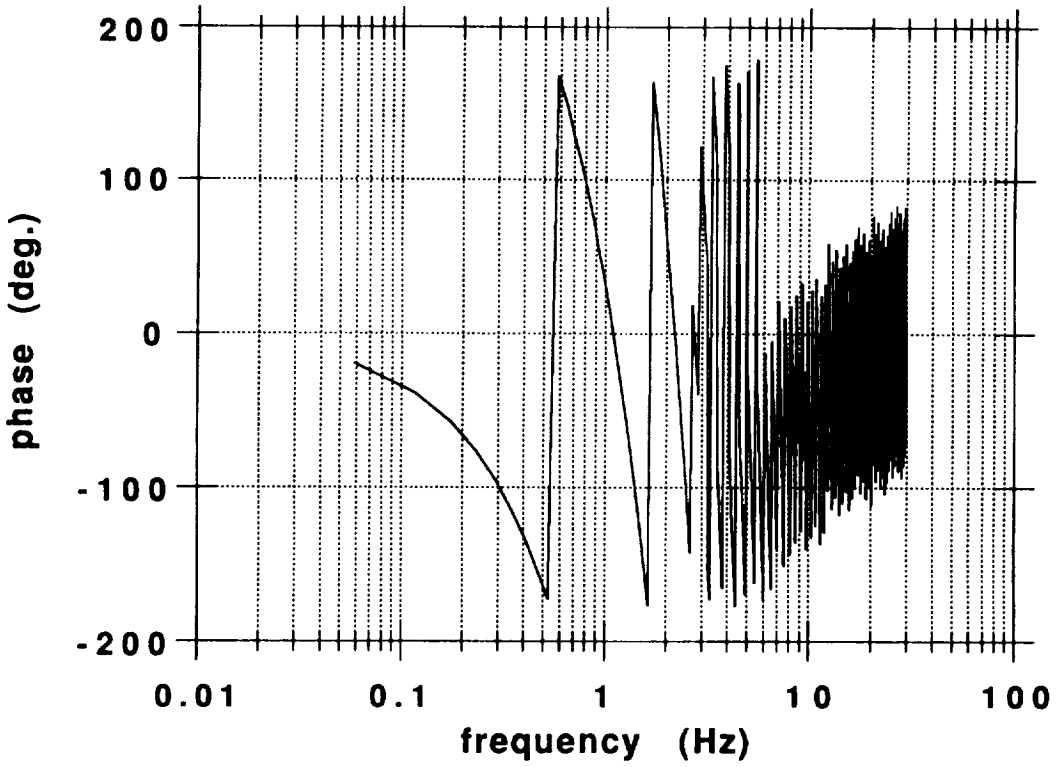
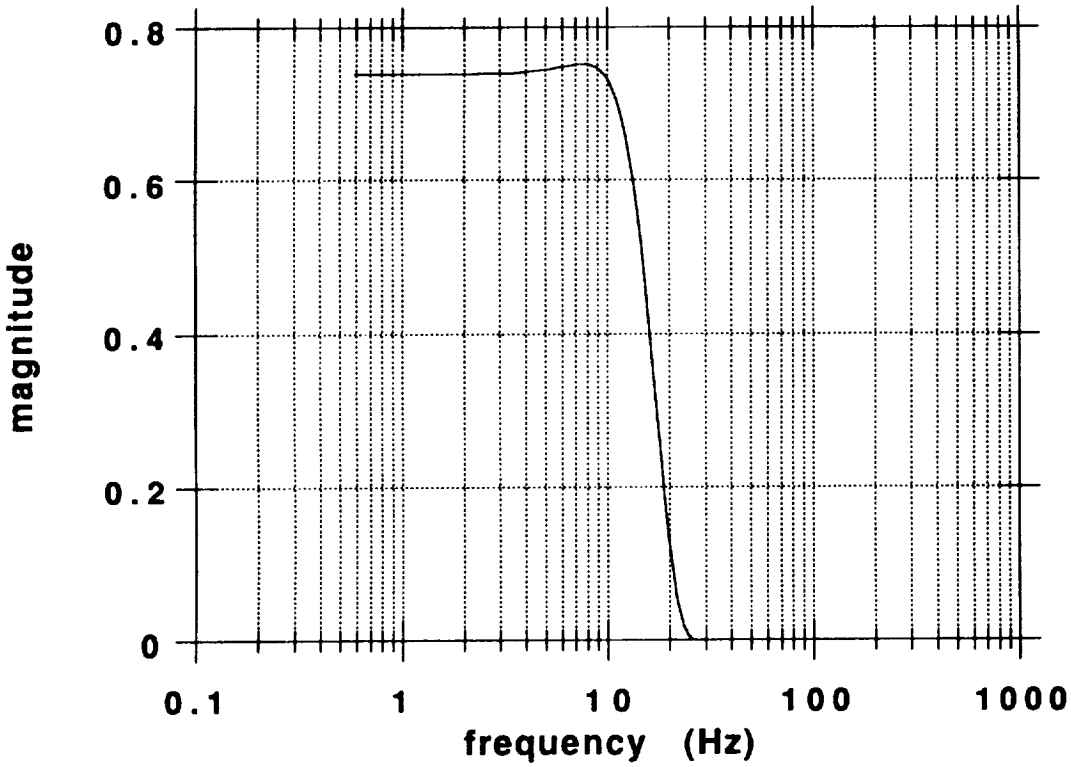


Figure 18b. Magnitude and phase plots of frequency response of RIU digital filter #2, sample rate = 600 Hz.



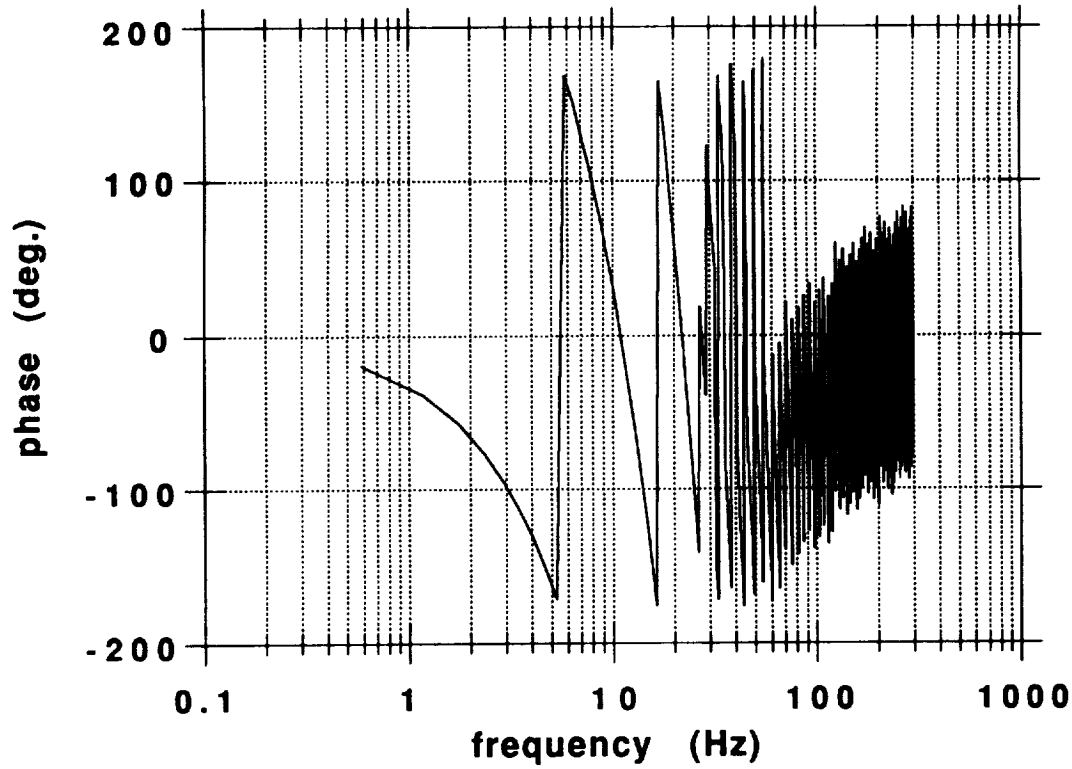
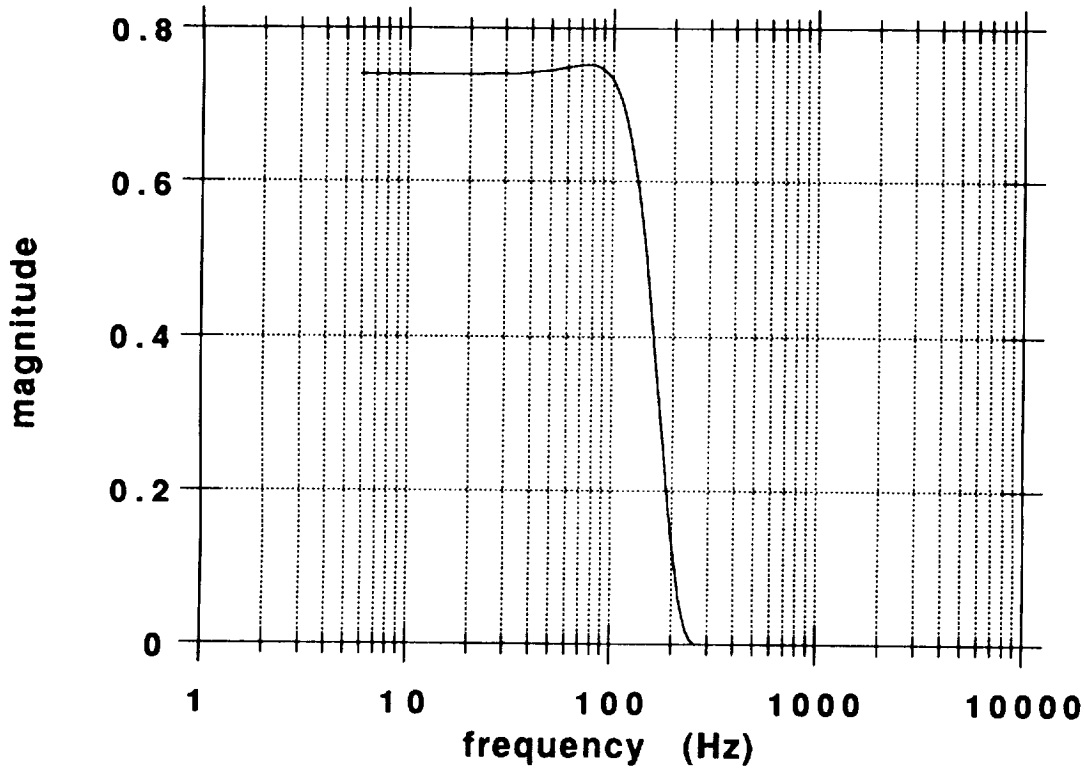


Figure 18c. Magnitude and phase plots of frequency response of RIU digital filter #2, sample rate = 6000 Hz.



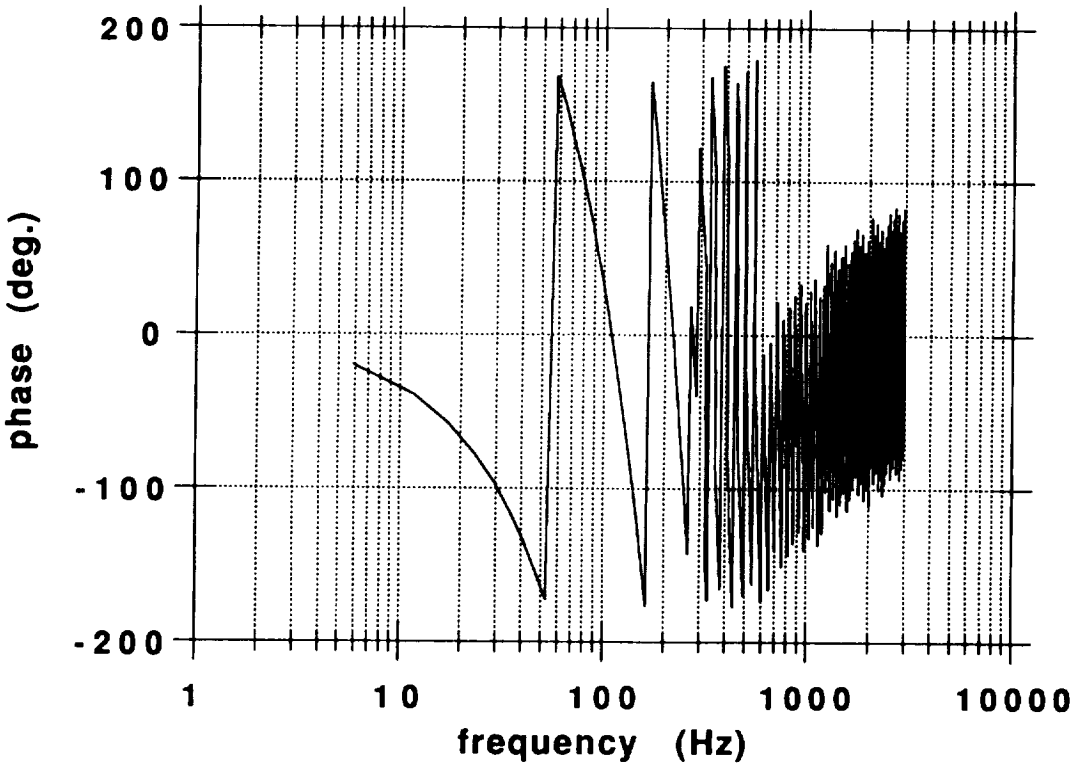


Figure 19a. Magnitude and phase plots of frequency response of RIU digital filter #3, sample rate = 60 Hz.

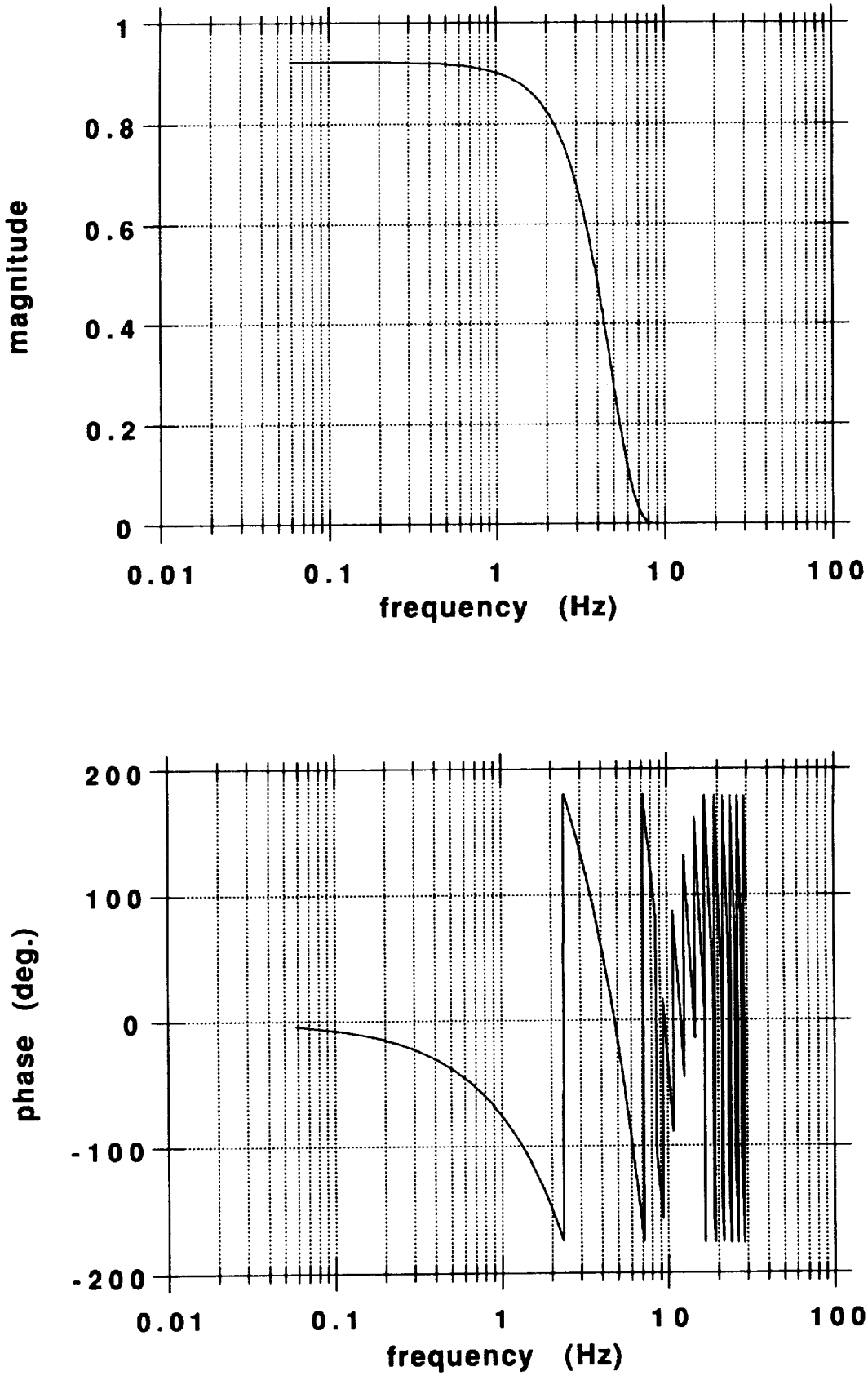
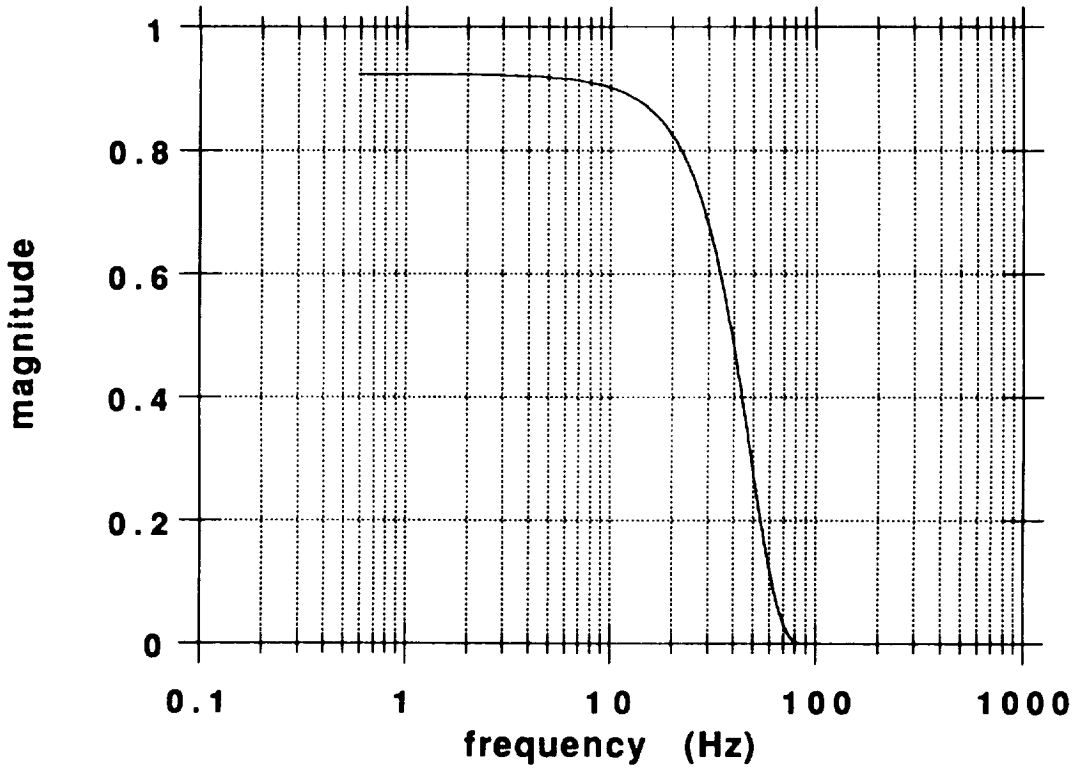


Figure 19b. Magnitude and phase plots of frequency response of RIU digital filter #3, sample rate = 600 Hz.



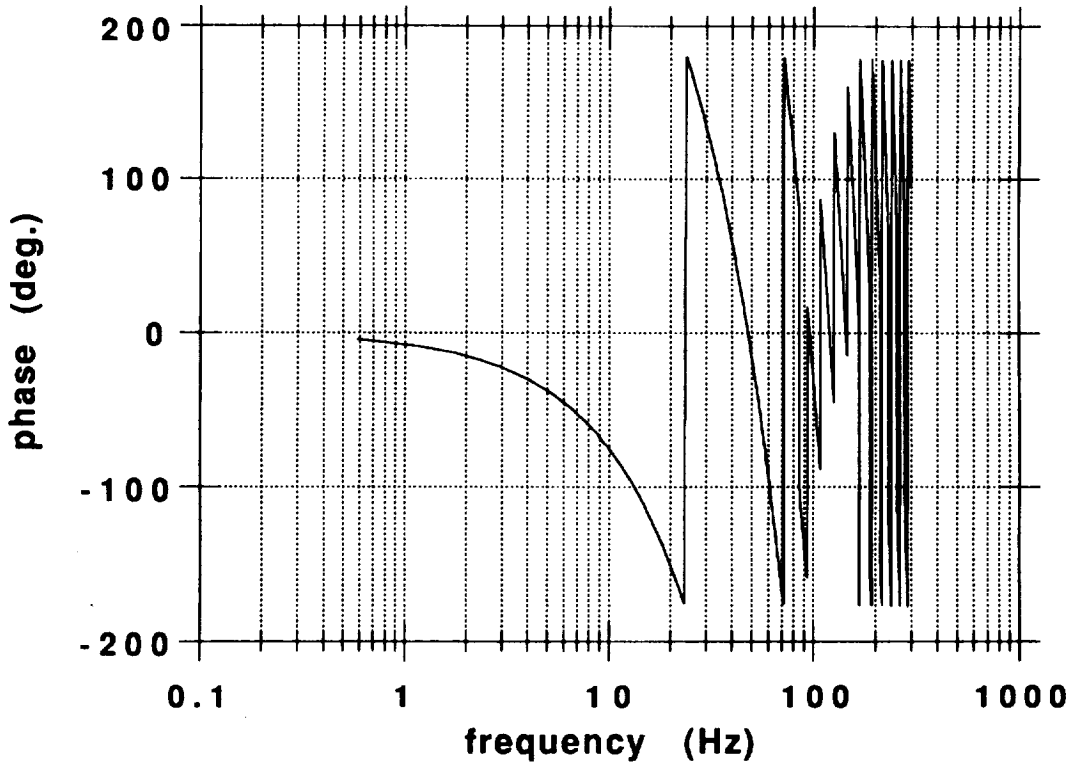
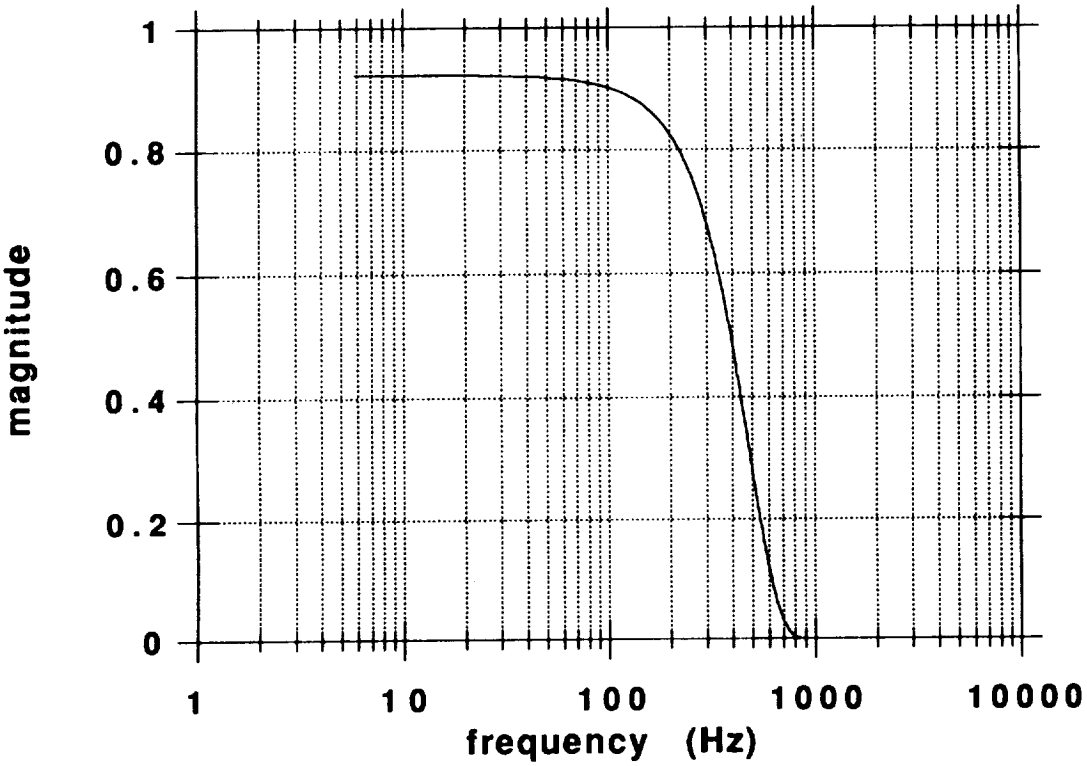


Figure 19c. Magnitude and phase plots of frequency response of RIU digital filter #3, sample rate = 6000 Hz.



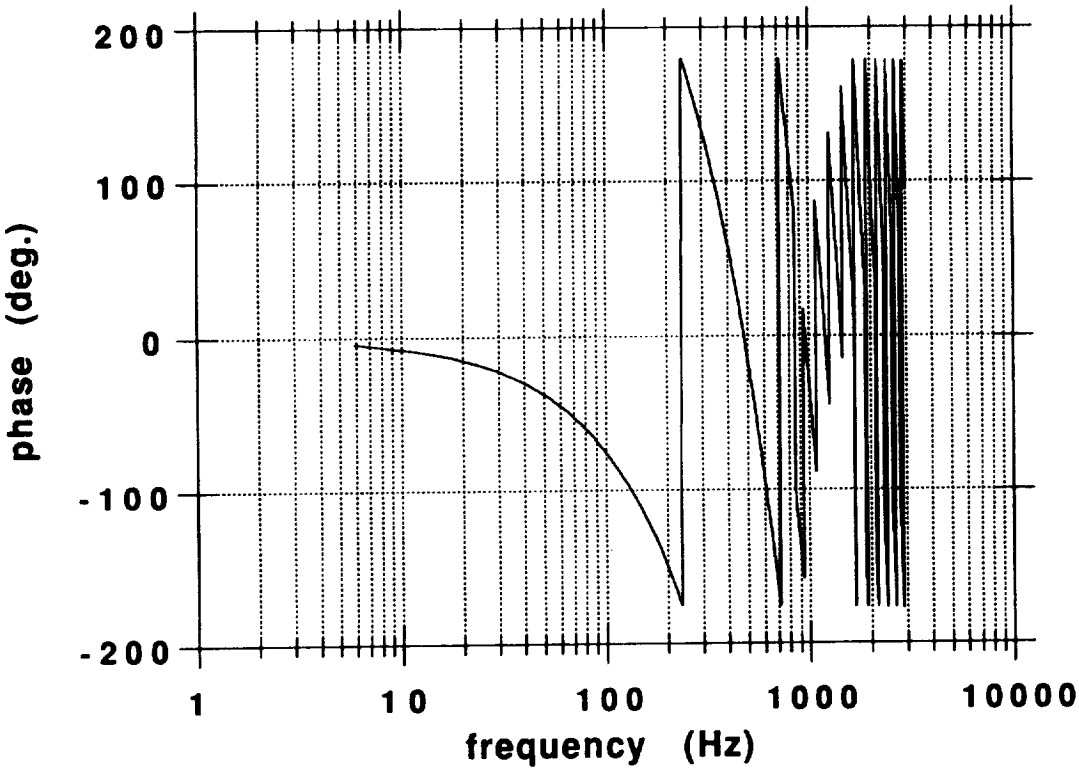


Figure 20a. Overlay plot of 0.1 Hz sine wave test, showing the raw and RIU digital filter #2 output time histories.

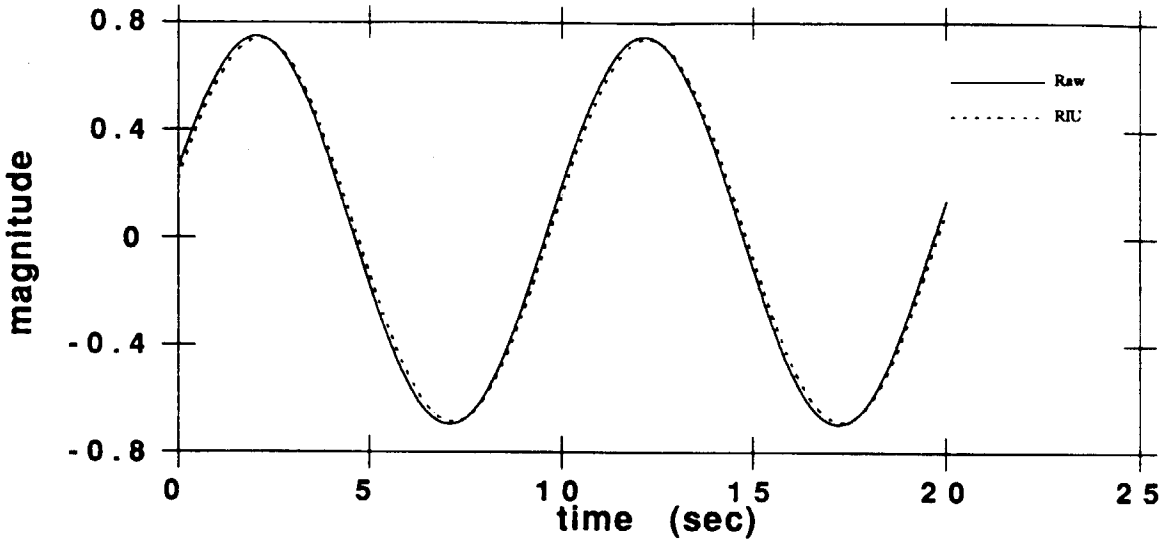


Figure 20b. Overlay plot comparing the measured output with a PRO-MATLAB simulation of RIU filter #2, for an 0.1 Hz sine wave input.

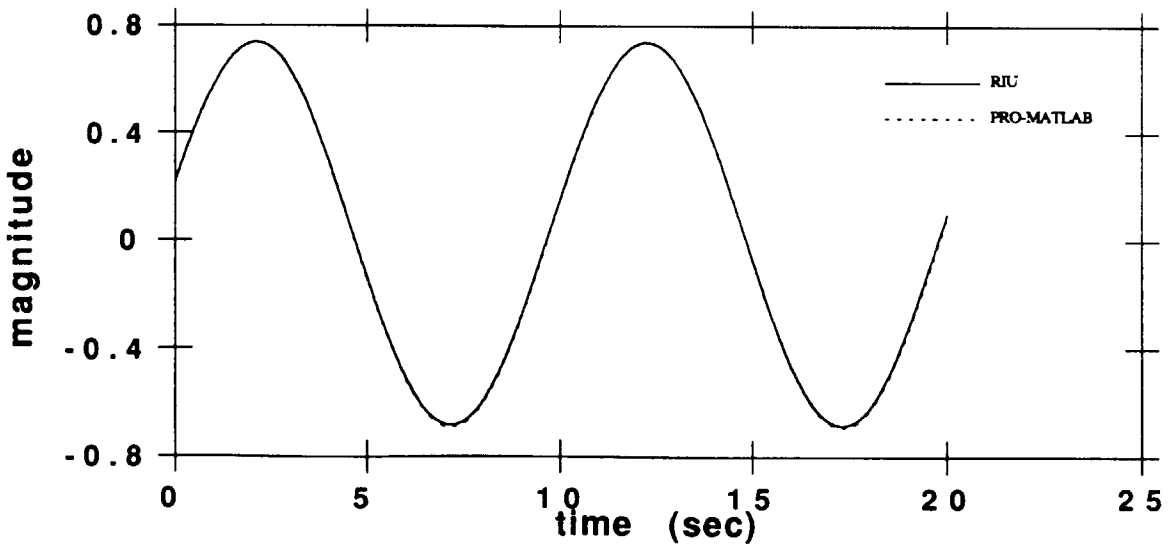


Figure 21a. Overlay plot of 1.0 Hz sine wave test, showing the raw and RIU digital filter #2 output time histories.

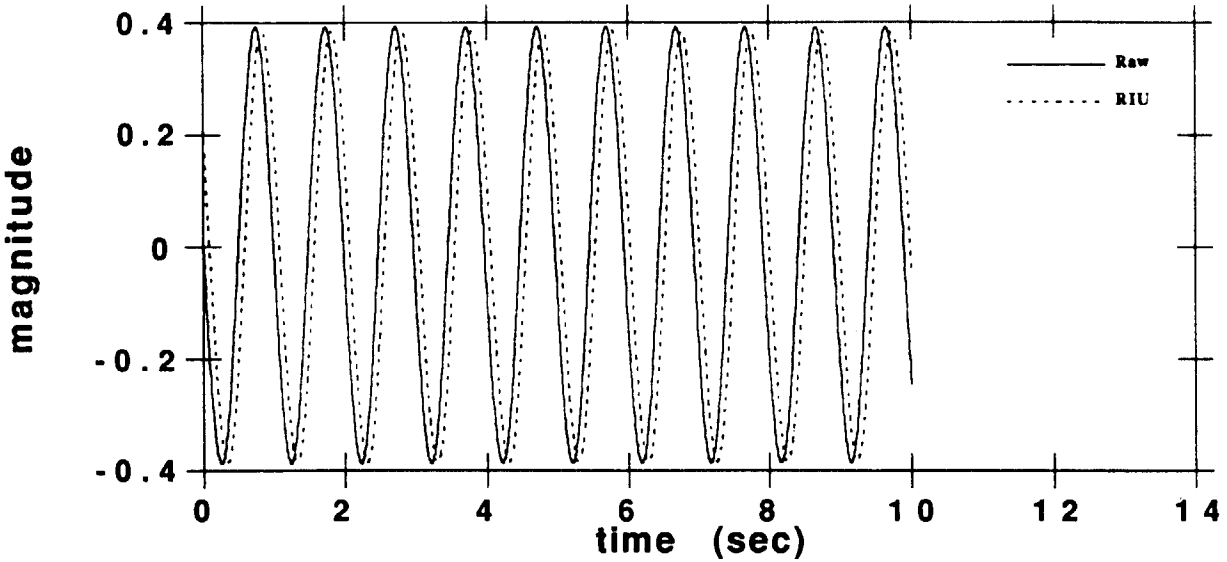


Figure 21b. Overlay plot comparing the measured output with a PRO·MATLAB simulation of RIU filter #2, for an 1.0 Hz sine wave input.

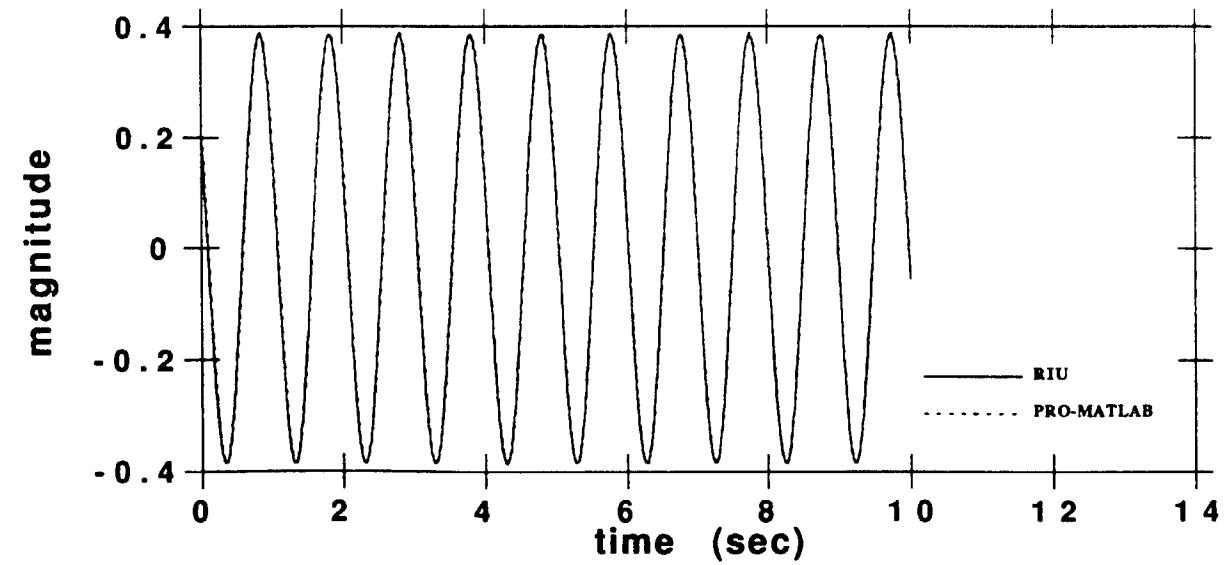


Figure 22a. Overlay plot of 8.0 Hz sine wave test, showing the raw and RIU digital filter #2 output time histories.

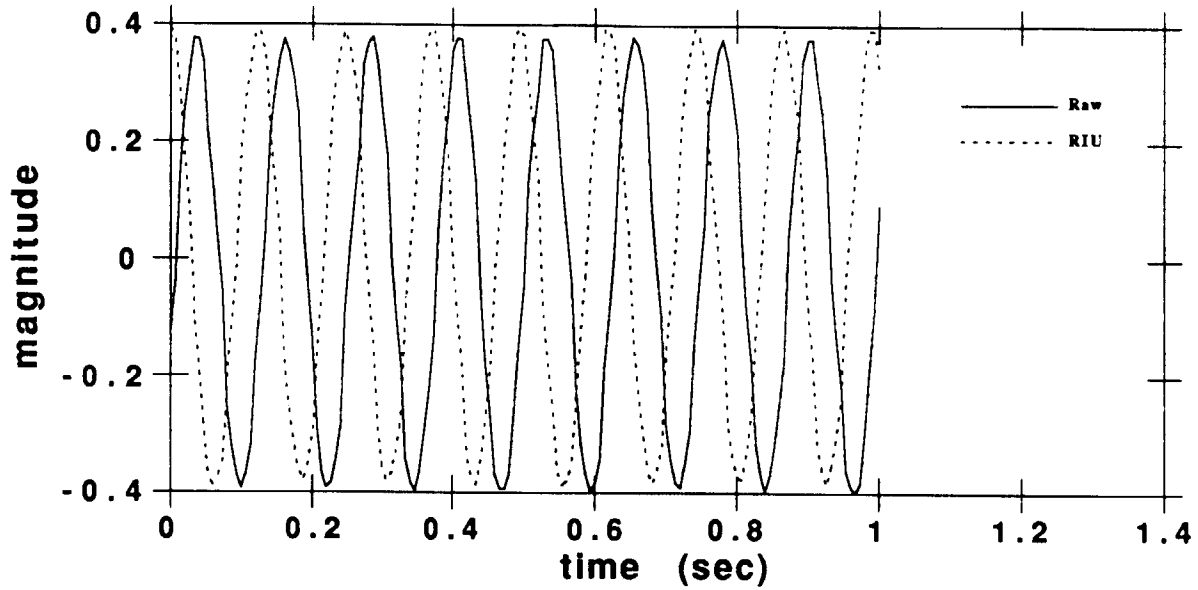


Figure 22b. Overlay plot comparing the measured output with a PRO-MATLAB simulation of RIU filter #2, for an 8.0 Hz sine wave input.

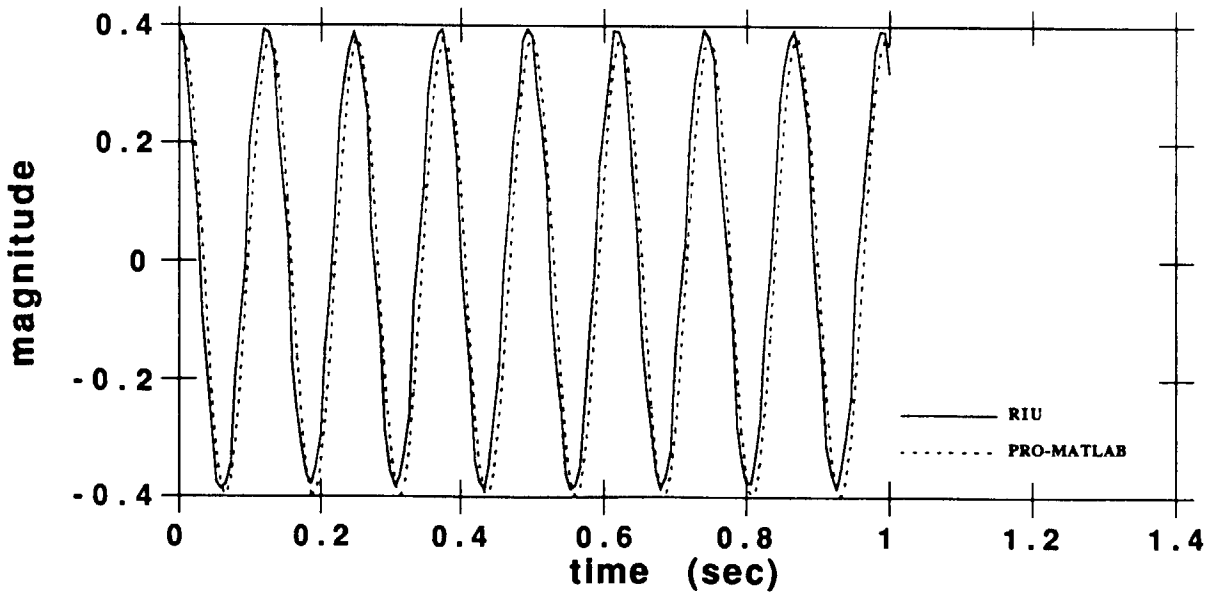


Figure 23a. Overlay plot of 0.1 Hz sine wave test, showing the raw and RIU digital filter #3 output time histories.

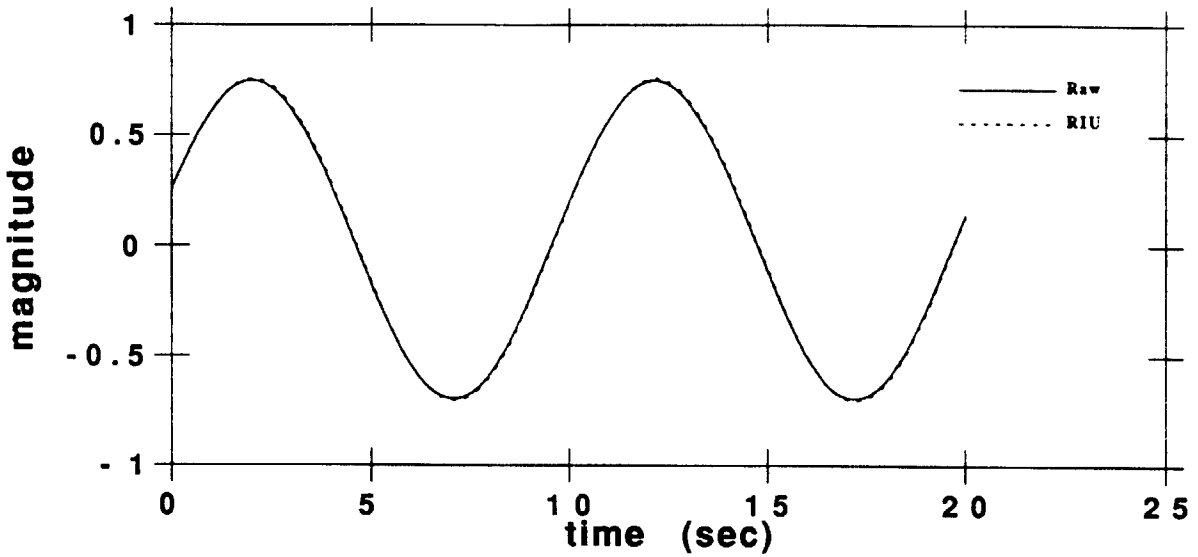


Figure 23b. Overlay plot comparing the measured output with a PRO-MATLAB simulation of RIU filter #3, for an 0.1 Hz sine wave input.

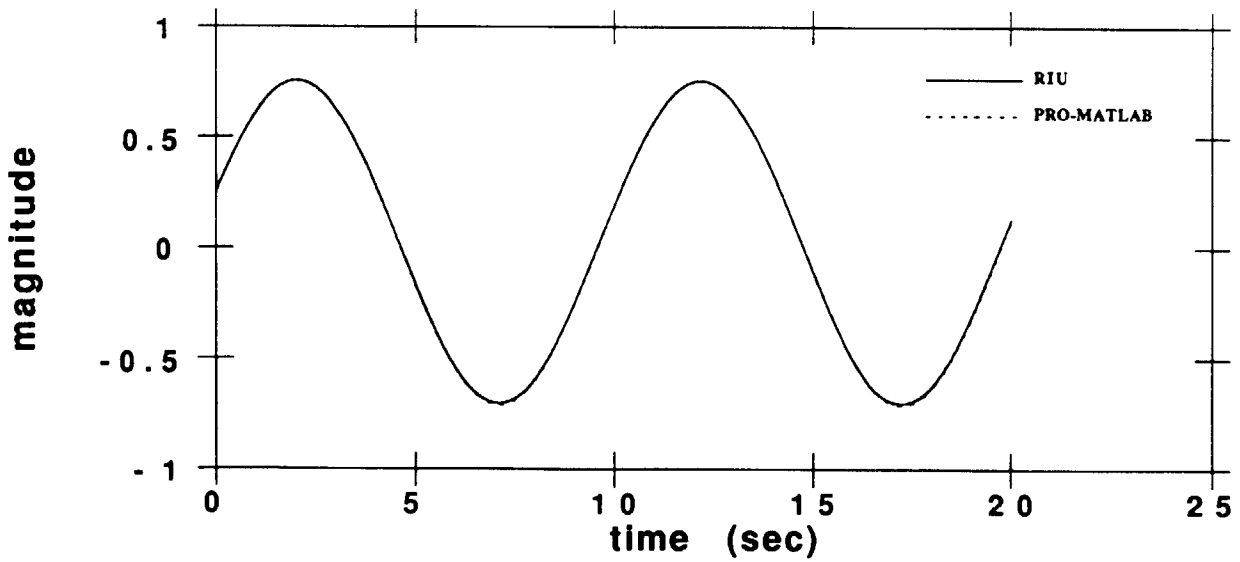


Figure 24a. Overlay plot of 1.0 Hz sine wave test, showing the raw and RIU digital filter #3 output time histories.

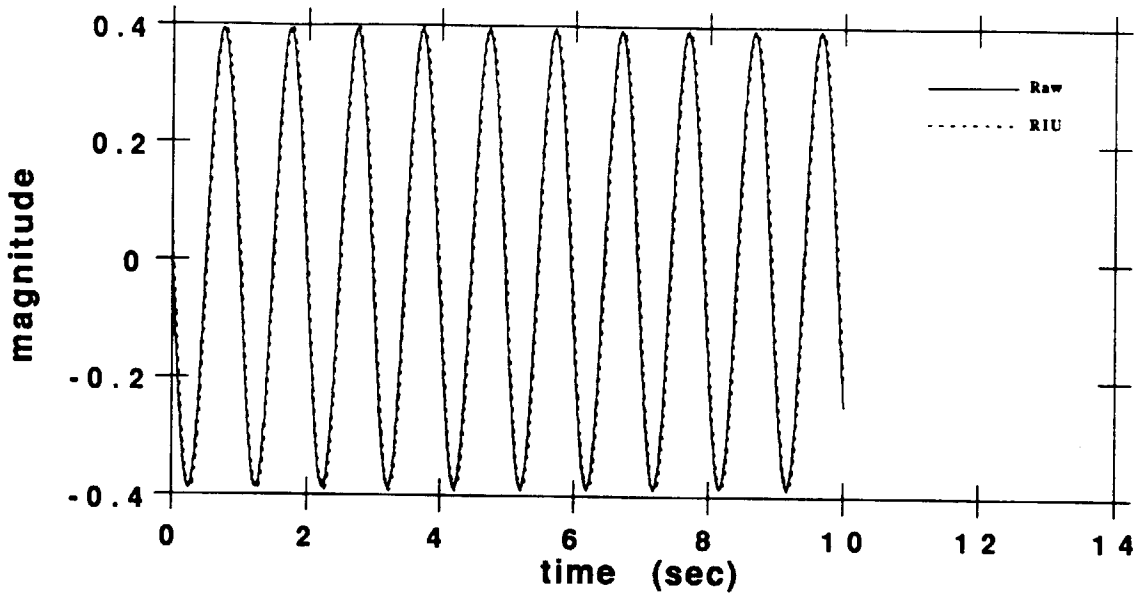


Figure 24b. Overlay plot comparing the measured output with a PRO-MATLAB simulation of RIU filter #3, for an 1.0 Hz sine wave input.

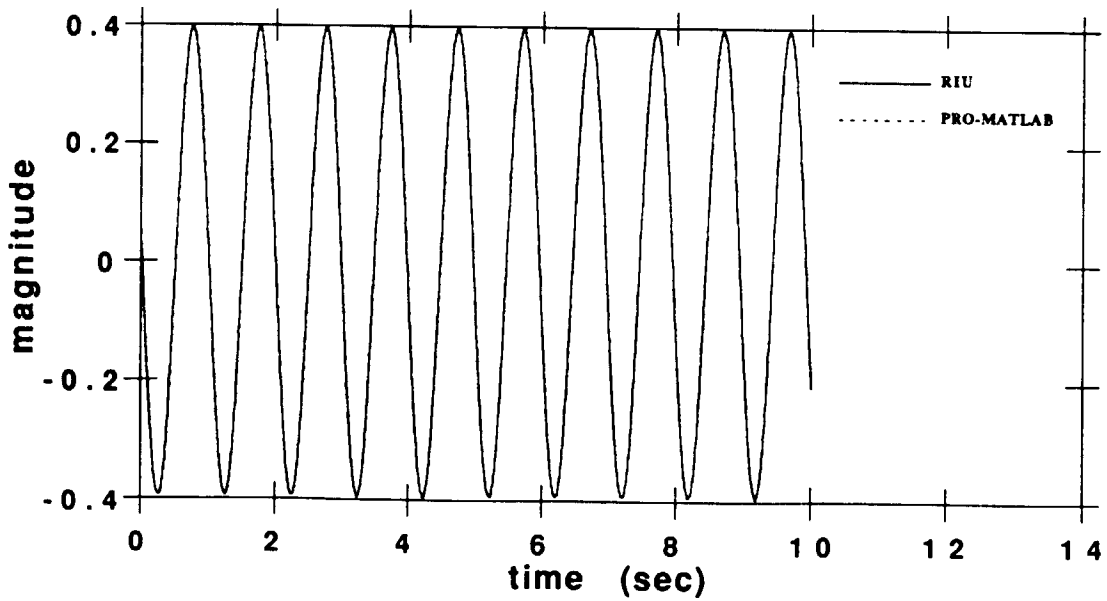


Figure 25a. Overlay plot of 8.0 Hz sine wave test, showing the raw and RIU digital filter #3 output time histories.

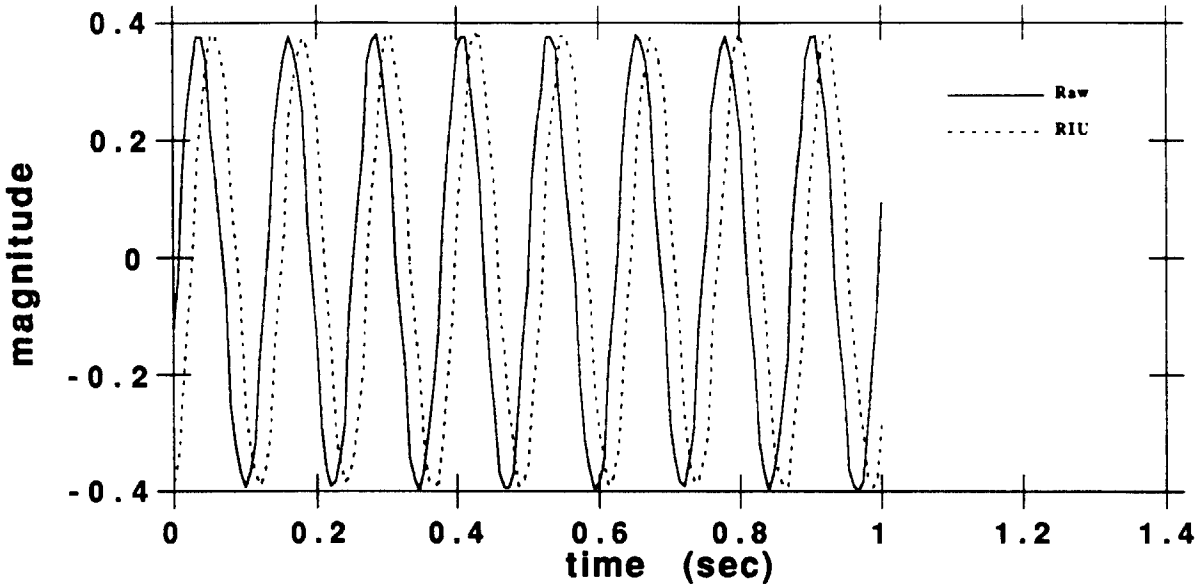


Figure 25b. Overlay plot comparing the measured output with a PRO-MATLAB simulation of RIU filter #3, for an 8.0 Hz sine wave input.

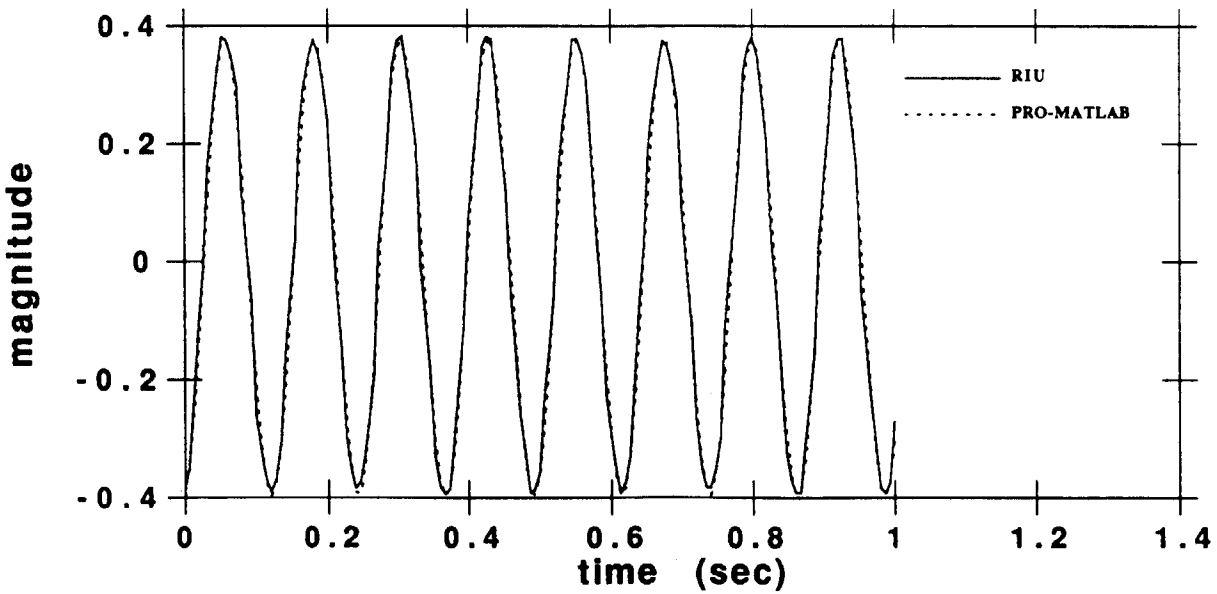
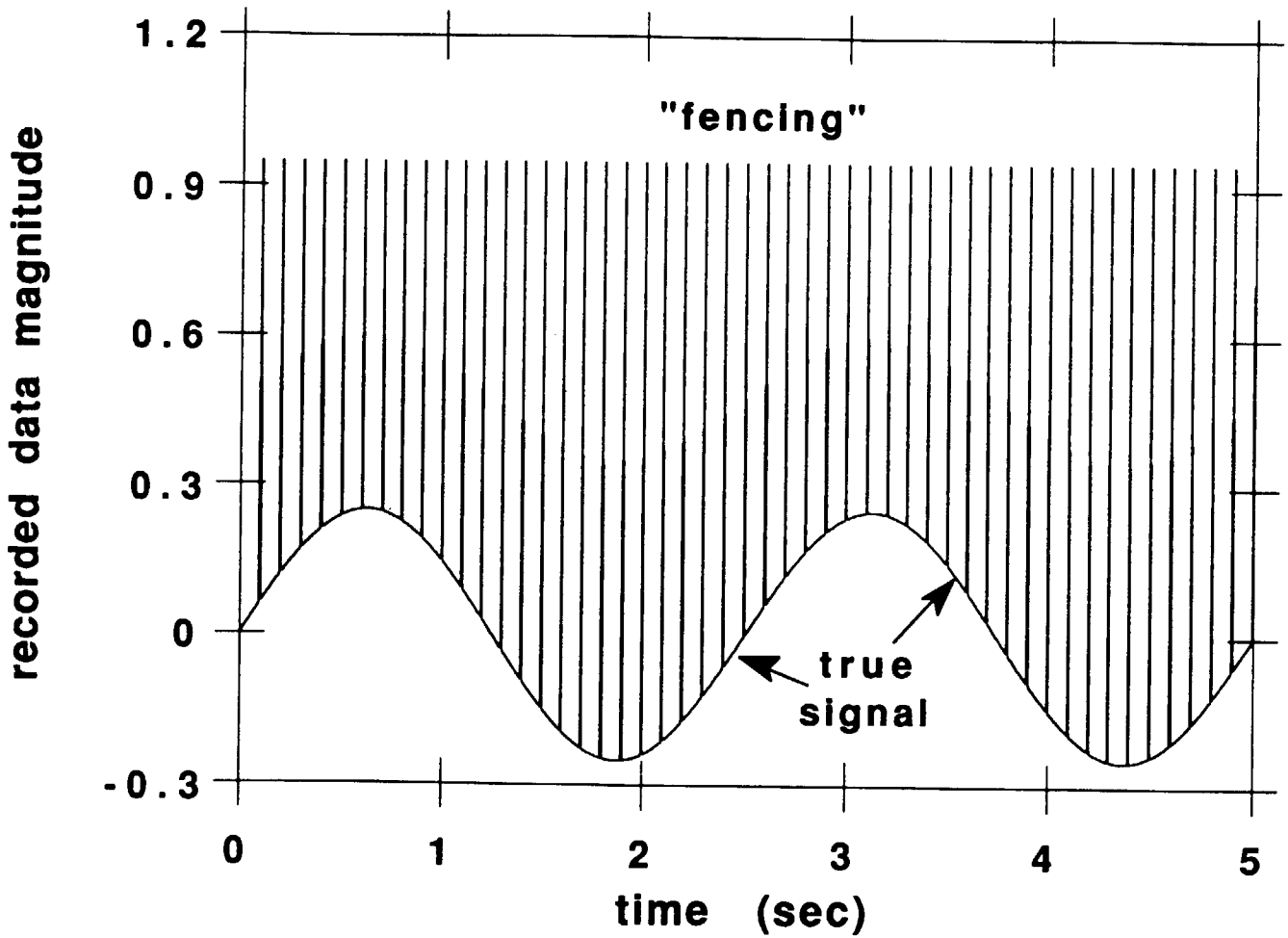


Figure 26. Sample GSET recorded time history plot illustrating the "fencing" problem.



APPENDIX A - CCS Hardware Acceptance Test General Log

```
:\GENERAL.LOG
04/12/91 03:25:45 PM

SYSTEM INITIALIZATION
04/12/91 03:25:45 PM
PC-1553 POWERUP STATUS
PASSED
PIOC POWERUP STATUS
RT REPORTED NO POWERUP ERRORS
HRMC POWERUP STATUS
RT REPORTED NO POWERUP ERRORS

ERROR LOG FILE SELECTION
04/12/91 03:26:37 PM
C:\ERROR.LOG

BATCH FILE SELECTION
04/12/91 03:35:26 PM
A:\JUMPADDR.BCH
PASSED

GSE INTERNAL PIOC JUMP TO ADDRESS FUNCTION
04/12/91 03:35:32 PM
0
0
80
PASSED

GSE INTERNAL HRMC JUMP TO ADDRESS FUNCTION
04/12/91 03:35:57 PM
0
0
80
PASSED

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS SELECT HSPC CHANNEL FUNCTION
04/12/91 04:16:49 PM
1

SET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:16:49 PM
EDS

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:17:32 PM
34.2
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER RELAY ENABLE FUNCTION
04/12/91 04:17:53 PM
STEP COMPLETE
EDS CPU 5 POWERUP STATUS
COULD NOT READ POWERUP STATUS OF RT
FAILED
EDS CPU 4 POWERUP STATUS
COULD NOT READ POWERUP STATUS OF RT
FAILED

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS CLEAR HSPC CHANNEL FUNCTION
```

```
04/12/91 04:19:01 PM
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:21:07 PM
23.2
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER RELAY ENABLE FUNCTION
04/12/91 04:21:28 PM
STEP COMPLETE
EDS CPU 5 POWERUP STATUS
RT REPORTED NO POWERUP ERRORS
PASSED
EDS CPU 4 POWERUP STATUS
RT REPORTED NO POWERUP ERRORS
PASSED

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS HSPC STATUS FUNCTION
04/12/91 04:22:08 PM
LOCAL CURRENT
  2.15 A
LOCAL VOLTAGE
 26.10 V
UUT INPUT VOLTAGE
 23.40 V
UUT CURRENT MONITOR
  2.14 A
UUT VOLTAGE MONITOR
 19.90 V
UUT
  5.30 V
UUT TEMPERATURE MONITOR
   299 K
VOLT REFERENCE
  9.99 V
BATTERY BACKUP DISABLED
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:23:13 PM
34.0
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS HSPC STATUS FUNCTION
04/12/91 04:23:28 PM
LOCAL CURRENT
  1.49 A
LOCAL VOLTAGE
 36.40 V
UUT INPUT VOLTAGE
 34.30 V
UUT CURRENT MONITOR
  1.45 A
UUT VOLTAGE MONITOR
 32.70 V
UUT
  5.33 V
```

```
UUT TEMPERATURE MONITOR
   300 K
VOLT REFERENCE
  9.99 V
BATTERY BACKUP DISABLED
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:05 PM
19.9
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:34 PM
38.0
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:57 PM
39.0
4.0
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:25:24 PM
28.2
4.0
STEP COMPLETE

BATCH FILE SELECTION
04/12/91 04:27:20 PM
A:\PWRTEST.BCH
PASSED

UUT POWER SUPPLY EDS POWER DROP OUT TEST
04/12/91 04:27:25 PM
1.0
PASSED

UUT POWER SUPPLY EDS PFI DURATION TEST
04/12/91 04:27:29 PM
PASSED

UUT POWER SUPPLY EDS PFI THRESHOLD TEST
04/12/91 04:27:38 PM
PASSED

UUT POWER SUPPLY EDS BATTERY BACKUP TEST
04/12/91 04:28:06 PM
PASSED

BATCH FILE SELECTION
04/12/91 04:37:44 PM
A:\EDSJUMP.BCH
PASSED

UUT INTERNAL EDS JUMP TO ADDRESS FUNCTION
04/12/91 04:37:51 PM
```

```
0
0
80
PASSED

BATCH FILE SELECTION
04/12/91 04:46:04 PM
A:\IFUAUTO.BCH
PASSED

UUT INTERNAL EDS SELECT CPU FUNCTION
04/12/91 04:46:08 PM
EDS CPU 5
STEP COMPLETE

UUT INTERNAL EDS CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:46:09 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS CPU TO CPU COMMUNICATION TEST
04/12/91 04:46:17 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS EDAC TEST
04/12/91 04:46:20 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:46:22 PM
PASSED

UUT INTERNAL EDS OVERLAY MEMORY TEST
04/12/91 04:46:24 PM
PASSED

UUT INTERNAL EDS NON-OVERLAY MEMORY TEST
04/12/91 04:46:32 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MICROCODE RAM MEMORY TEST
04/12/91 04:48:00 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR DATA RAM MEMORY TEST
04/12/91 04:48:08 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MATRIX MULTIPLY THROUGHPUT TEST
04/12/91 04:48:13 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:48:21 PM
4
6
8
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:48:27 PM
```

```
4
6
8
PASSED

UUT INTERNAL EDS SELECT CPU FUNCTION
04/12/91 04:48:30 PM
EDS CPU 4
STEP COMPLETE

UUT INTERNAL EDS CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:48:32 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS CPU TO CPU COMMUNICATION TEST
04/12/91 04:48:39 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS EDAC TEST
04/12/91 04:48:42 PM
PASSED

UUT INTERNAL EDS CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:48:44 PM
PASSED

UUT INTERNAL EDS OVERLAY MEMORY TEST
04/12/91 04:48:46 PM
PASSED

UUT INTERNAL EDS NON-OVERLAY MEMORY TEST
04/12/91 04:48:54 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MICROCODE RAM MEMORY TEST
04/12/91 04:50:24 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR DATA RAM MEMORY TEST
04/12/91 04:50:31 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MATRIX MULTIPLY THROUGHPUT TEST
04/12/91 04:50:35 PM
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:50:43 PM
4
6
8
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:50:49 PM
4
6
8
PASSED
```

```
UUT I/O FUNCTIONAL EDS EXTERNAL INTERRUPTS TEST
04/12/91 04:50:53 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B INTERNAL SELF TEST
04/12/91 04:50:55 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B ON-BOARD RAM TEST
04/12/91 04:50:57 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS MONITOR MODE TEST
04/12/91 04:51:01 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS CONTROLLER MODE TEST
04/12/91 04:51:06 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
04/12/91 04:51:10 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:51:12 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:51:14 PM

RESET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:51:36 PM
STEP COMPLETE

UUT I/O FUNCTIONAL EDS SELECT CPU FUNCTION
04/12/91 04:51:38 PM
EDS CPU 5
STEP COMPLETE

UUT I/O FUNCTIONAL EDS EXTERNAL INTERRUPTS TEST
04/12/91 04:51:39 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B INTERNAL SELF TEST
04/12/91 04:51:41 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B ON-BOARD RAM TEST
04/12/91 04:51:43 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS MONITOR MODE TEST
04/12/91 04:51:46 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS CONTROLLER MODE TEST
04/12/91 04:51:52 PM
PASSED
```

```
UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
04/12/91 04:51:57 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:51:59 PM
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:52:01 PM

RESET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:52:30 PM
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS SWITCH CONFIGURATION FUNCTION
04/12/91 04:52:35 PM
STEP COMPLETE

UUT INTERNAL MDIS 1 CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:52:39 PM
PASSED

UUT INTERNAL MDIS 1 CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:52:47 PM
PASSED

UUT INTERNAL MDIS 1 CPU FUNCTIONS EDAC TEST
04/12/91 04:52:49 PM
PASSED

UUT INTERNAL MDIS 1 OVERLAY MEMORY TEST
04/12/91 04:52:51 PM
PASSED

UUT INTERNAL MDIS 1 NON-OVERLAY MEMORY TEST
04/12/91 04:52:59 PM
PASSED

UUT INTERNAL MDIS 1 PROM TEST
04/12/91 04:53:59 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B INTERNAL SELF TEST
04/12/91 04:54:07 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B ON-BOARD RAM TEST
04/12/91 04:54:09 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B BUS MONITOR MODE TEST
04/12/91 04:54:12 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B BUS CONTROLLER MODE TEST
04/12/91 04:54:16 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
```

```
04/12/91 04:54:20 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:54:22 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:54:24 PM

RESET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:54:46 PM
STEP COMPLETE

UUT I/O FUNCTIONAL MDIS 1 EXTERNAL INTERRUPTS TEST
04/12/91 04:54:48 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 1
04/12/91 04:54:51 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 2
04/12/91 04:54:53 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 3
04/12/91 04:54:56 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 4
04/12/91 04:54:58 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 OUTPUT TEST
04/12/91 04:55:00 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 1
04/12/91 04:55:02 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 2
04/12/91 04:55:04 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 3
04/12/91 04:55:06 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 4
04/12/91 04:55:08 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 OUTPUT TEST
04/12/91 04:55:10 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC ON-BOARD RAM TEST
04/12/91 04:55:13 PM
```

```
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CALIBRATE TEST
04/12/91 04:55:14 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC RANGE TEST
04/12/91 04:55:16 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CONVERSION RATE TEST
04/12/91 04:55:20 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CHANNEL TEST
04/12/91 04:55:22 PM

UUT I/O FUNCTIONAL MDIS 1 SIO NORMAL MESSAGE IN TEST
04/12/91 04:59:12 PM
PASSED

BATCH FILE SELECTION
04/12/91 05:00:07 PM
A:\MDISSIO.BCH
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO ON-BOARD RAM TEST
04/12/91 05:00:11 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO NORMAL MESSAGE IN TEST
04/12/91 05:00:13 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO NORMAL MESSAGE OUT TEST
04/12/91 05:00:16 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO PARITY ERROR MESSAGE TEST
04/12/91 05:00:19 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO CHANNEL ERROR MESSAGE TEST
04/12/91 05:00:21 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO SYNC ERROR MESSAGE TEST
04/12/91 05:00:23 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO MISSING TRANSITION MESSAGE TEST
04/12/91 05:00:25 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 SIO EXTRA TRANSITION MESSAGE TEST
04/12/91 05:00:27 PM
PASSED

UUT I/O FUNCTIONAL MDIS 1 HRM CONFIGURATION RAM TEST
04/12/91 05:01:01 PM
```

APPENDIX B - CCS Hardware Acceptance Test Error Log

```
:\ERROR.LOG
04/12/91 03:26:37 PM


SYSTEM INITIALIZATION
04/12/91 03:26:37 PM
INITIALIZING PC-1553B CARD
PC-1553B CARD IS INITIALIZED
PIOC POWERUP STATUS
PASSED
HRMC POWERUP STATUS
PASSED
GENERAL LOG ENABLED

BATCH FILE SELECTION
04/12/91 03:35:26 PM
PASSED

GSE INTERNAL PIOC JUMP TO ADDRESS FUNCTION
04/12/91 03:35:32 PM
JUMP TO ADDRESS PERFORMED BY RT
PASSED
PERFORM AS IS COMMAND PERFORMED BY RT
PASSED

GSE INTERNAL HRMC JUMP TO ADDRESS FUNCTION
04/12/91 03:35:57 PM
JUMP TO ADDRESS PERFORMED BY RT
PASSED
PERFORM AS IS COMMAND PERFORMED BY RT
PASSED

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS SELECT HSPC CHANNEL FUNCTION
04/12/91 04:16:49 PM
HSPC CHANNEL SELECT FUNCTION PERFORMED BY RT
STEP COMPLETE

SET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:16:49 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:17:32 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER RELAY ENABLE FUNCTION
04/12/91 04:17:53 PM
POWER RELAY ENABLED FUNCTION PERFORMED BY RT
STEP COMPLETE
EDS CPU 5 POWERUP STATUS
TIMEOUT OCCURRED WAITING ON RT 1553 CARD RESPONSE
EDS CPU 4 POWERUP STATUS
TIMEOUT OCCURRED WAITING ON RT 1553 CARD RESPONSE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS CLEAR HSPC CHANNEL FUNCTION
04/12/91 04:19:01 PM
HSPC CHANNEL CLEAR FUNCTION PERFORMED BY RT
STEP COMPLETE
```

```
GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:21:07 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER RELAY ENABLE FUNCTION
04/12/91 04:21:28 PM
POWER RELAY ENABLED FUNCTION PERFORMED BY RT
STEP COMPLETE
EDS CPU 5 POWERUP STATUS
PASSED
EDS CPU 4 POWERUP STATUS
PASSED

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS HSPC STATUS FUNCTION
04/12/91 04:22:08 PM
HSPC STATUS FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:23:13 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS HSPC STATUS FUNCTION
04/12/91 04:23:28 PM
HSPC STATUS FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:05 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:34 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:24:57 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS POWER SUPPLY OUTPUT FUNCTION
04/12/91 04:25:24 PM
POWER SUPPLY OUTPUT FUNCTION PERFORMED BY RT
STEP COMPLETE

BATCH FILE SELECTION
04/12/91 04:27:20 PM
PASSED

UUT POWER SUPPLY EDS POWER DROP OUT TEST
04/12/91 04:27:25 PM
POWER SUPPLY DROPOUT TEST INIT PERFORMED BY RT
PASSED
POWER SUPPLY DROPOUT FUNCTION PERFORMED BY RT
PASSED
```

```
POWER SUPPLY DROPOUT TEST CHECK PERFORMED BY RT
PASSED

UUT POWER SUPPLY EDS PFI DURATION TEST
04/12/91 04:27:29 PM
BATTERY BACKUP ON FUNCTION PERFORMED BY RT
PASSED
PFI DURATION TEST INIT PERFORMED BY RT
PASSED
POWER RELAY DISABLED FUNCTION PERFORMED BY RT
PASSED
POWER RELAY ENABLED FUNCTION PERFORMED BY RT
PASSED
PFI DURATION TEST CHECK PERFORMED BY RT
PASSED
BATTERY BACKUP OFF FUNCTION PERFORMED BY RT
PASSED

UUT POWER SUPPLY EDS PFI THRESHOLD TEST
04/12/91 04:27:38 PM
PFI THRESHOLD INIT PERFORMED BY RT
PASSED
POWER RELAY DISABLED FUNCTION PERFORMED BY RT
PASSED
POWER RELAY ENABLED FUNCTION PERFORMED BY RT
PASSED
PASSED

UUT POWER SUPPLY EDS BATTERY BACKUP TEST
04/12/91 04:28:06 PM
BATTERY BACKUP ON FUNCTION PERFORMED BY RT
PASSED
BATTERY BACKUP TEST INIT PERFORMED BY RT
PASSED
POWER RELAY DISABLED FUNCTION PERFORMED BY RT
PASSED
POWER RELAY ENABLED FUNCTION PERFORMED BY RT
PASSED
BATTERY BACKUP TEST CHECK PERFORMED BY RT
PASSED
BATTERY BACKUP OFF FUNCTION PERFORMED BY RT
PASSED

BATCH FILE SELECTION
04/12/91 04:37:44 PM
PASSED

UUT INTERNAL EDS JUMP TO ADDRESS FUNCTION
04/12/91 04:37:51 PM
JUMP TO ADDRESS PERFORMED BY EDS CPU 4
PASSED
JUMP TO ADDRESS PERFORMED BY EDS CPU 5
PASSED
PERFORM AS IS COMMAND PERFORMED BY RT
PASSED
PERFORM AS IS COMMAND PERFORMED BY RT
PASSED

BATCH FILE SELECTION
04/12/91 04:46:04 PM
```

```
PASSED

UUT INTERNAL EDS SELECT CPU FUNCTION
04/12/91 04:46:08 PM
EDS CPU 5 SELECTED

UUT INTERNAL EDS CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:46:09 PM
WATCHDOG TIMER TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS CPU TO CPU COMMUNICATION TEST
04/12/91 04:46:17 PM
CPU TO CPU COMMUNCATION TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS EDAC TEST
04/12/91 04:46:20 PM
EDAC TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:46:22 PM
MEMORY WRITE PROTECT TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS OVERLAY MEMORY TEST
04/12/91 04:46:24 PM
OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS NON-OVERLAY MEMORY TEST
04/12/91 04:46:32 PM
NON-OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MICROCODE RAM MEMORY TEST
04/12/91 04:48:00 PM
MICROCODE RAM MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR DATA RAM MEMORY TEST
04/12/91 04:48:08 PM
DATA RAM MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MATRIX MULTIPLY THROUGHPUT TEST
04/12/91 04:48:13 PM
MATRIX MULTIPLY THROUGHPUT TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:48:21 PM
FIXED POINT VARIABLE MATRIX TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:48:27 PM
FLOATING POINT VARIABLE MATRIX TEST PERFORMED BY RT
PASSED
```

```
UUT INTERNAL EDS SELECT CPU FUNCTION
04/12/91 04:48:30 PM
EDS CPU 4 SELECTED

UUT INTERNAL EDS CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:48:32 PM
WATCHDOG TIMER TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS CPU TO CPU COMMUNICATION TEST
04/12/91 04:48:39 PM
CPU TO CPU COMMUNCATION TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS EDAC TEST
04/12/91 04:48:42 PM
EDAC TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:48:44 PM
MEMORY WRITE PROTECT TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS OVERLAY MEMORY TEST
04/12/91 04:48:46 PM
OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS NON-OVERLAY MEMORY TEST
04/12/91 04:48:54 PM
NON-OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MICROCODE RAM MEMORY TEST
04/12/91 04:50:24 PM
MICROCODE RAM MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR DATA RAM MEMORY TEST
04/12/91 04:50:31 PM
DATA RAM MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR MATRIX MULTIPLY THROUGHPUT TEST
04/12/91 04:50:35 PM
MATRIX MULTIPLY THROUGHPUT TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:50:43 PM
FIXED POINT VARIABLE MATRIX TEST PERFORMED BY RT
PASSED

UUT INTERNAL EDS ARRAY PROCESSOR FIXED POINT VARIABLE MATRIX MULTIPLY TEST
04/12/91 04:50:49 PM
FLOATING POINT VARIABLE MATRIX TEST PERFORMED BY RT
PASSED
```

```
UUT I/O FUNCTIONAL EDS EXTERNAL INTERRUPTS TEST
04/12/91 04:50:53 PM
EXTERNAL INTERRUPTS INIT PERFORMED BY RT
PASSED
INTERRUPT RT PERFORMED BY PIOC
PASSED
EXTERNAL INTERRUPTS TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL EDS 1553B INTERNAL SELF TEST
04/12/91 04:50:55 PM
1553B INTERNAL SELF TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL EDS 1553B ON-BOARD RAM TEST
04/12/91 04:50:57 PM
1553B ON-BOARD RAM TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS MONITOR MODE TEST
04/12/91 04:51:01 PM
MONITOR MODE TEST PERFORMED BY PIOC
PASSED
EVALUATE MONITOR MODE PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL EDS 1553B BUS CONTROLLER MODE TEST
04/12/91 04:51:06 PM
BUS CONTROLLER TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
04/12/91 04:51:10 PM
1553B RT TO RT TEST PERFORMED
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:51:12 PM
BUS CONTROLLER TO REMOTE TERMINAL BROADCAST
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:51:14 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
```

```
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
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TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
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TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
```

PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
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 TERMINAL ADDRESS INIT PERFORMED BY RT
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 TERMINAL ADDRESS TEST PERFORMED BY RT
 PASSED

 RESET UUT TERMINAL ADDRESS FUNCTION
 04/12/91 04:51:36 PM
 SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
 STEP COMPLETE
 TERMINAL ADDRESS INIT PERFORMED BY RT
 STEP COMPLETE

 UUT I/O FUNCTIONAL EDS SELECT CPU FUNCTION
 04/12/91 04:51:38 PM
 EDS CPU 5 SELECTED

 UUT I/O FUNCTIONAL EDS EXTERNAL INTERRUPTS TEST
 04/12/91 04:51:39 PM
 EXTERNAL INTERRUPTS INIT PERFORMED BY RT
 PASSED
 INTERRUPT RT PERFORMED BY PIOC
 PASSED
 EXTERNAL INTERRUPTS TEST PERFORMED BY RT
 PASSED

 UUT I/O FUNCTIONAL EDS 1553B INTERNAL SELF TEST
 04/12/91 04:51:41 PM
 1553B INTERNAL SELF TEST PERFORMED BY RT
 PASSED

 UUT I/O FUNCTIONAL EDS 1553B ON-BOARD RAM TEST
 04/12/91 04:51:43 PM
 1553B ON-BOARD RAM TEST PERFORMED BY RT
 PASSED

 UUT I/O FUNCTIONAL EDS 1553B BUS MONITOR MODE TEST
 04/12/91 04:51:46 PM
 MONITOR MODE TEST PERFORMED BY PIOC
 PASSED
 EVALUATE MONITOR MODE PERFORMED BY RT
 PASSED

 UUT I/O FUNCTIONAL EDS 1553B BUS CONTROLLER MODE TEST
 04/12/91 04:51:52 PM
 BUS CONTROLLER TEST PERFORMED BY RT
 PASSED

 UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
 04/12/91 04:51:57 PM
 1553B RT TO RT TEST PERFORMED
 PASSED
```

UUT I/O FUNCTIONAL EDS 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:51:59 PM
BUS CONTROLLER TO REMOTE TERMINAL BROADCAST
PASSED

UUT I/O FUNCTIONAL EDS 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:52:01 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
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SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
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TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED

RESET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:52:30 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
STEP COMPLETE
TERMINAL ADDRESS INIT PERFORMED BY RT
STEP COMPLETE

GSE I/O FUNCTIONAL PIOC HEALTH AND STATUS SWITCH CONFIGURATION FUNCTION
04/12/91 04:52:35 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
STEP COMPLETE
TERMINAL ADDRESS INIT PERFORMED BY RT
STEP COMPLETE
PERFORM AS IS COMMAND PERFORMED BY RT
STEP COMPLETE

UUT INTERNAL MDIS 1 CPU FUNCTIONS WATCHDOG TIMER TEST
04/12/91 04:52:39 PM
WATCHDOG TIMER TEST PERFORMED BY RT
PASSED

```
UUT INTERNAL MDIS 1 CPU FUNCTIONS MEMORY WRITE PROTECT TEST
04/12/91 04:52:47 PM
MEMORY WRITE PROTECT TEST PERFORMED BY RT
PASSED

UUT INTERNAL MDIS 1 CPU FUNCTIONS EDAC TEST
04/12/91 04:52:49 PM
EDAC TEST PERFORMED BY RT
PASSED

UUT INTERNAL MDIS 1 OVERLAY MEMORY TEST
04/12/91 04:52:51 PM
OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL MDIS 1 NON-OVERLAY MEMORY TEST
04/12/91 04:52:59 PM
NON-OVERLAY MEMORY TEST PERFORMED BY RT
PASSED

UUT INTERNAL MDIS 1 PROM TEST
04/12/91 04:53:59 PM
PROM TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B INTERNAL SELF TEST
04/12/91 04:54:07 PM
1553B INTERNAL SELF TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B ON-BOARD RAM TEST
04/12/91 04:54:09 PM
1553B ON-BOARD RAM TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B BUS MONITOR MODE TEST
04/12/91 04:54:12 PM
MONITOR MODE TEST PERFORMED BY PIOC
PASSED
EVALUATE MONITOR MODE PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B BUS CONTROLLER MODE TEST
04/12/91 04:54:16 PM
BUS CONTROLLER TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE RECEIVE RT TO RT TRANSFER TEST
04/12/91 04:54:20 PM
1553B RT TO RT TEST PERFORMED
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE RECEIVE BROADCAST COMMAND TEST
04/12/91 04:54:22 PM
BUS CONTROLLER TO REMOTE TERMINAL BROADCAST
PASSED

UUT I/O FUNCTIONAL MDIS 1 1553B RT MODE TERMINAL ADDRESS TEST
04/12/91 04:54:24 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
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PASSED
TERMINAL ADDRESS INIT PERFORMED BY RT
PASSED
TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
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TERMINAL ADDRESS INIT PERFORMED BY RT
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TERMINAL ADDRESS TEST PERFORMED BY RT
PASSED

RESET UUT TERMINAL ADDRESS FUNCTION
04/12/91 04:54:46 PM
SET UUT TERMINAL ADDRESS PERFORMED BY PIOC
STEP COMPLETE
TERMINAL ADDRESS INIT PERFORMED BY RT
STEP COMPLETE

UUT I/O FUNCTIONAL MDIS 1 EXTERNAL INTERRUPTS TEST
04/12/91 04:54:48 PM
EXTERNAL INTERRUPTS INIT PERFORMED BY RT
PASSED
INTERRUPT RT PERFORMED BY PIOC
PASSED
EXTERNAL INTERRUPTS TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 1
04/12/91 04:54:51 PM
INPUTS 1 LOW TEST 1 PERFORMED BY PIOC
PASSED
INPUTS 1 LOW PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 2
04/12/91 04:54:53 PM
INPUTS 1 HIGH TEST 1 PERFORMED BY PIOC
PASSED
INPUTS 1 HIGH PERFORMED BY RT
PASSED

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UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 3
04/12/91 04:54:56 PM
INPUTS 1 HIGH TEST 2 PERFORMED BY PIOC
PASSED
INPUTS 1 HIGH PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 INPUT TEST 4
04/12/91 04:54:58 PM
INPUTS 1 HIGH TEST 3 PERFORMED BY PIOC
PASSED
INPUTS 1 HIGH PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 1 OUTPUT TEST
04/12/91 04:55:00 PM
PATTERN 1 OUT PERFORMED BY RT
PASSED
PATTERN 1 TEST PERFORMED BY PIOC
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 1
04/12/91 04:55:02 PM
INPUTS 2 LOW TEST 1 PERFORMED BY PIOC
PASSED
INPUTS 2 LOW PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 2
04/12/91 04:55:04 PM
INPUTS 2 HIGH TEST 1 PERFORMED BY PIOC
PASSED
INPUTS 2 HIGH PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 3
04/12/91 04:55:06 PM
INPUTS 2 HIGH PERFORMED BY RT
PASSED
INPUTS 2 HIGH PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 INPUT TEST 4
04/12/91 04:55:08 PM
INPUTS 2 HIGH TEST 3 PERFORMED BY PIOC
PASSED
INPUTS 2 HIGH PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 BIO 2 OUTPUT TEST
04/12/91 04:55:10 PM
PATTERN 2 OUT PERFORMED BY RT
PASSED
PATTERN 2 TEST PERFORMED BY PIOC
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC ON-BOARD RAM TEST
04/12/91 04:55:13 PM
ON-BOARD RAM TEST PERFORMED BY RT
PASSED
```

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CALIBRATE TEST
04/12/91 04:55:14 PM
CALIBRATE TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC RANGE TEST
04/12/91 04:55:16 PM
RANGE TEST 1 PERFORMED BY PIOC
PASSED
RANGE TEST 1 PERFORMED BY RT
PASSED
RANGE TEST 2 PERFORMED BY PIOC
PASSED
RANGE TEST 2 PERFORMED BY RT
PASSED
RANGE TEST 3 PERFORMED BY PIOC
PASSED
RANGE TEST 3 PERFORMED BY RT
PASSED
RANGE TEST 4 PERFORMED BY PIOC
PASSED
RANGE TEST 4 PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CONVERSION RATE TEST
04/12/91 04:55:20 PM
CONVERSION RATE TEST PERFORMED BY RT
PASSED

UUT I/O FUNCTIONAL MDIS 1 AMUX/ADC CHANNEL TEST
04/12/91 04:55:22 PM
OUTPUT VOLTAGE LEVEL TEST PERFORMED BY RT
PASSED
AMUX CHANNEL TEST PERFORMED BY RT
PASSED
OUTPUT VOLTAGE LEVEL TEST PERFORMED BY RT
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AMUX CHANNEL TEST PERFORMED BY RT
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APPENDIX C - CCS Computations Speed Test

APPENDIX C - CCS Computation Speed Test

A set of 5 "dummy" control experiments were executed on the CCS to determine the achievable sampling rates for state feedback controllers of varying sizes. For these tests, the CCS/RIU was connected to the CEM, however, the computed actuator commands were not transmitted to the test article since the "dummy" control law matrices were not taken from real controllers, but were arbitrarily defined. Each of these test runs were the same, with the exceptions being the controller size and the sampling rate. Each of the controllers used the 8 accelerometer signals to compute 8 thruster commands. The tests were of relatively short duration (10 seconds); the reason being that finding the achievable sampling rate for the 5 controllers was done by trial and error, thus, in order to speed up the process, the time length per test was deliberately trimmed back.

Table C1 contains the achieved sampling rates for the 5 tests, and their corresponding controller sizes; these values are also plotted in Figure C1.

Table C1. Achievable sampling rates on the CCS.

Test #	Controller states	Sampling rate (Hz)
1	16	255
2	30	250
3	50	229
4	70	210
5	100	175

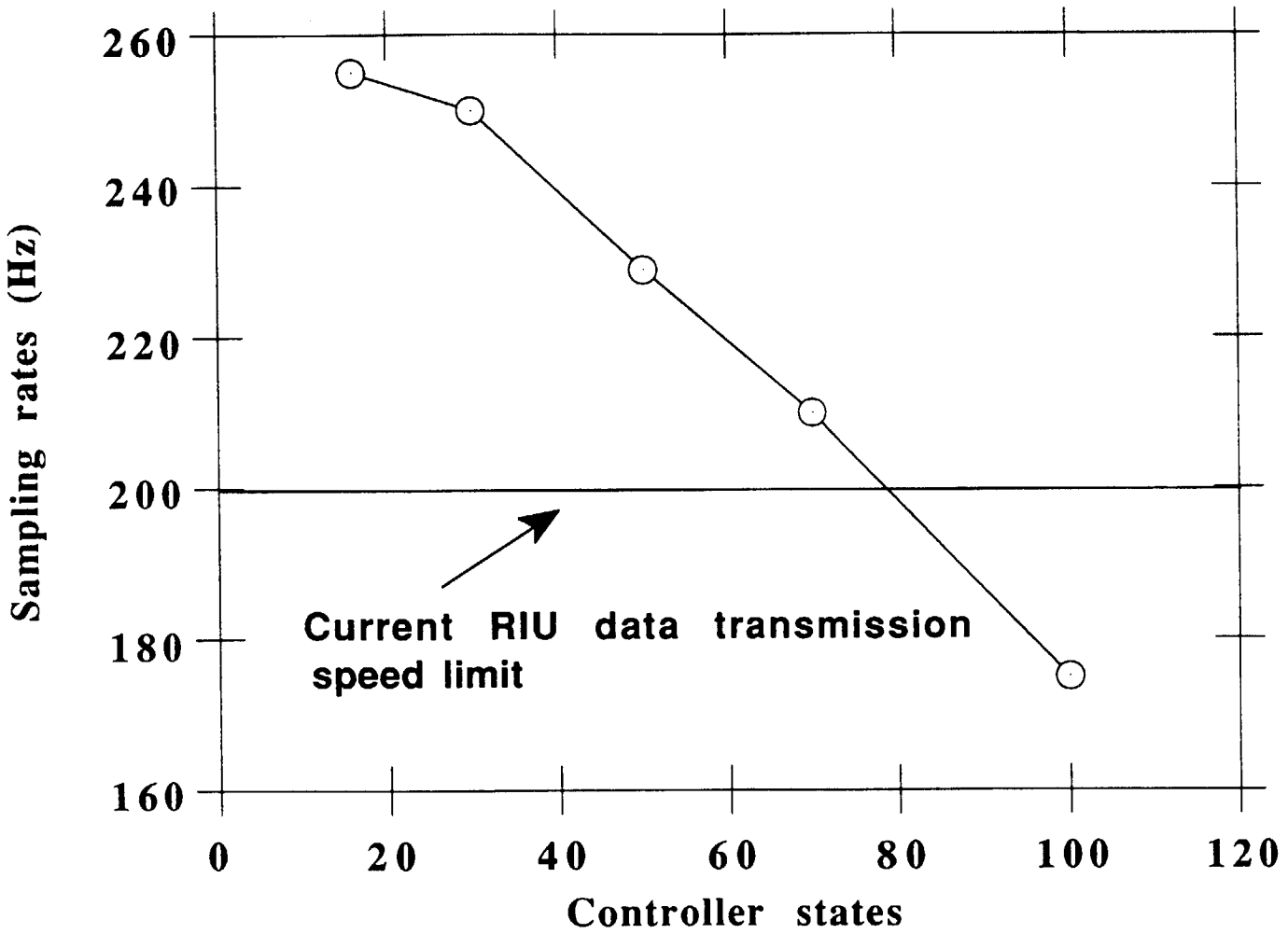
Several important points should be made here. First, the above values really represent the fastest that the CCS, particularly the EDS, can process and compute a control law of a given size. The above sampling rates, are the rates at which the CCS requests data updates from the RIU; the current RIU, however, can only transmit updated I/O data to and from the CCS at a rate of 200 Hz. Thus, the controllers which were executed above this figure were not using fresh sensor data in every CCS sample period. For this reason, the maximum practical CCS sampling rate, for controllers with 70 states or less, is 200 Hz with the present system.

The second factor to be considered, regarding system speed, is the number of sensors and actuators selected for the experiment, and just as importantly, how they are to be used. In the above "dummy" tests, signals from each of the 8 accelerometers were used by the controllers to compute the eight thruster commands, in what would be considered "typical" active control experiments. The current CCS/RIU, however, allows more freedom in how sensors and actuators can be used in experiments. For example, the RIU can digitally process a signal from a single

sensor with multiple filters; each filter's output is considered as a distinct signal, to be transmitted to the CCS. This, in effect, multiplies the amount of data which is received by the CCS. In addition, not every sensor signal has to be used in the controller in the CCS. As for the actuators, their computed controller commands may be augmented by pre-computed disturbance command values. The use of these options will slow down the overall speed of the system.

The final point concerns the recording of test data in real time. The GSET records the test data (i.e., sensor signals, actuator commands and their time syncs) off of the 1553B bus and onto its hard disk. The particular 1553B interface card in the GSET is an old design with known limitations in the speeds at which it can correctly interpret the data. It has been observed throughout the CCS/RIU development and test phases that sampling at the higher rates increases the probability that data recording errors will occur in the GSET. For example, in the speeds tests involving the 16 state decoupled controller, executed at 250+Hz, test runs with 6 and 9 data recording errors, respectively, over a 10 second test period, have been noted. This is compared to the occurrences, on the average, of only 1 or 2 data recording errors over a 30 second test period, for the same controller executed at 200 Hz or less. It should be emphasized that these data recording errors do not imply that the sensor signals used in the control law and the resulting computed computed actuator commands are in error, and thus corrupting the experiment. The only impact which these errors have is in recording the data.

Figure C1. Plot of the achievable CCS sampling rates versus the number of states in the controller.



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13. ABSTRACT *(Maximum 200 words)*

This work reports on the validation tests conducted on the Control/Structures Interaction (CSI) Computer System (CCS)/Remote Interface Unit (RIU), which consists of a commercially available, LaRC programmed, space flight qualified computer and a flight like data acquisition and filtering computer, developed at LaRC. The tests were performed in the Space Structures Research Laboratory (SSRL) and included open loop excitation, closed loop control, safing, RIU digital filtering and RIU stand alone testing with the CSI Evolutionary MOdel (CEM) Phase-0 testbed. The test results indicated that the CCS/RIU sytem is comparable to ground based systems in performing real-time control-structure experiments.

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