

FRIDEN ELECTRONIC CALCULATORS

EC-130 SERVICE MANUAL

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A. INTRODUCTION

This article is written as a primary training device and presupposes a thorough understanding of the detailed logic of the EC-130 Calculator. It is intended that the student, using only this article and the associated block diagram, will be able to grasp both the logic and the circuitry of this machine by drawing upon his background of training and experience on the EC-130 Calculator.

Because this is not a new machine but a redesign of the existing EC-130, many basic circuits are identical or nearly identical to existing circuits in the EC-130. These areas will be passed over lightly or not touched upon at all. This will limit the subject to the differences in logic and circuitry between the Three Counter EC-130 and Four Counter EC-130. This limitation has two advantages. First, it reduces the size of the volume to a small package of vital information and, second, it avoids the discouragement which normally accompanies the thought of plowing through a massive volume of already familiar information to find the desired information.

B. THE ENTRY ENCODER

The Entry Encoder is a scale of eight binary counter which has only parallel inputs and parallel outputs. It consists of three flip-flops, and replaces the Change Sign, Shift Down, Store, Recall, Repeat, and Add or Sub flip-flops. The Entry Encoder is used in the Change Sign, Clear Entry, Store, Recall, Repeat, Add, and Subtract functions, and the appropriate keyboard switches are used to set the Entry Encoder flip-flops. The keyboard is the same as the one used in the Four Counter machine so there are necessarily some changes in the keyboard interface to permit one switch to set the proper binary code into the Entry Encoder. The enclosed Encoder Truth Table (Figure 5-1) shows which Encoder flip-flops are set by each of the seven keyboard switches listed. The Encoder flip-flops are reset after each function

**ENTRY ENCODER
TRUTH TABLE**

FLIP-FLOP	1	2	4
RECALL	1	0	0
CHG SIGN	0	1	0
REPEAT	1	1	0
CLEAR ENTRY	0	0	1
ADD SUB	1	0	1
STORE	0	1	1

Figure 5-1

so it is not necessary to reset any flip-flops with a keyboard switch. It is necessary only to set the appropriate flip-flops; however, because each flip-flop can be set by more than one switch, the switch outputs are applied to the flip-flops through diode OR gates. For example, the EEN2 FF can be set by the Change Sign switch, the Repeat switch, and the Store switch. These switch outputs are applied to an OR gate, and the output of the OR gate is integrated to provide the DC enable signal for the AC AND gate which sets the EEN2 FF.

Note, also the connection between the Add switch and the Subtract switch. This connection exists for the same reason as on the Four Counter machine. The Subtract switch must enable the Sign Control FF to be reset and the Add switch must not, but both switches must enable the EEN1 FF and the EEN4 FF to be set. Hence, a diode is connected to isolate the two switches in one direction and connect them in the other direction. The Clear Entry switch is not used as an input to the OR gate which sets the EEN4 FF because the output of the Clear Entry switch must be used to reset the Overflow FF as well as to set the EEN4 FF; whereas it is not desired to have the outputs of the Add, Subtract, or Store switches enable the resetting of the Overflow FF.

The Encoder is reset at the end of each function by ERF3 (the same signal which resets the function flip-flops in the Four Counter machine).

C. THE TIMING CHAIN

There are a few changes in the timing chain, but all are relatively simple. The emitter followers have been removed from the set outputs of the D, E, F, and G flip-flops because there is insufficient loading of these signals to warrant the additional drive. The P flip-flop has been eliminated and R1 will not be intensified.

The clock flip-flop has been eliminated, and the output of I-169 is used as the clock signal and triggers the A flip-flop. Since the clock frequency must stay at about 333KC, the master oscillator frequency is cut in half by using .0056 μ f and .0033 μ f capacitors in the tank circuit in place of the 1500 pf and the 820 pf capacitors. The emitter follower and the inverter in the oscillator circuit have also been changed to provide the risetime and falltime necessary for the clock signal. The new oscillator circuit is shown in Figure 5-2.

An extremely important point to remember is that the A, B, and G flip-flops are still preset so that the sync pulse ALWAYS comes off the delay line in B3 R3 C0 time. This is true irregardless of the position of data in the delay line with re-

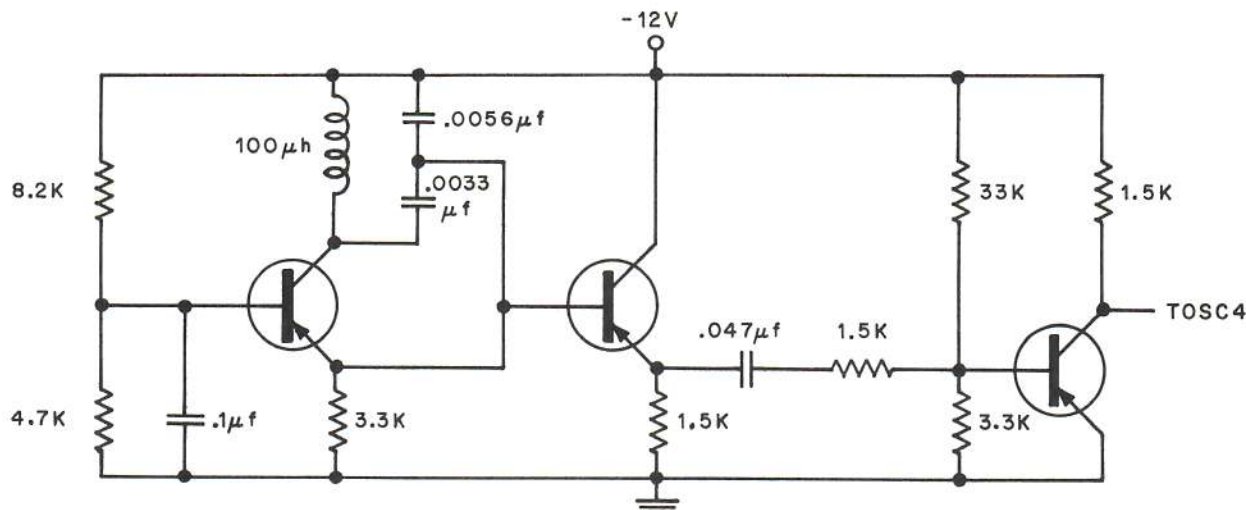


Figure 5-2

spect to the sync pulse. (This is also true in the Four Counter machine but this point bears re-emphasizing.) Much will be made of this later.

Two other changes involve the decoded timing signals. Since TC04 is needed as well as TC03, TC03 is now an input to an inverter (I-301) to generate TC04. Also, C15 is no longer developed as a separate signal. So the OR gate that develops TCX5 (I-229) has four timing signal inputs which define C15 time. The same signals are also used at two other OR gates to define C15 time. All in all, the timing chain has not been changed much.

D. THE PHASE COUNTER

Only one very small change has been made in the Phase Counter. Since M1AD3 is no longer developed, MSU3 is used to inhibit stepping the counter to PS6 from PS5 in divide. This will also inhibit stepping from PS4 to PS5 so an AC AND gate is used to set the PC1 FF in PS4 of divide. AC AND gate 1171 is enabled by MSU3 and HOME1 is the trigger. So, when the Phase Counter is in PS4 of Divide A-1171 enables HOME1 to step the counter to PS5, but does not enable it to be stepped to PS6 until MSU3 is lost. This poses an interesting question. Is MSU3 detrimental to the operation of the counter in subtract? No, it is not, because MSU3 is not developed until PS7 of subtract, and although MSU3 inhibits stepping the counter to PSZ, PS73 and HOME1 reset the CF FF and the Phase Counter is pulled to PSZ by the override reset.

PSZ3 is no longer decoded because it is no longer needed.

E. DATA FLOW

1. NORMAL DATA FLOW

In this machine, data flow in machine idle is serial from the delay line to the A Counter, parallel from the A Counter to the C Counter, and serial from the C Counter to the delay line. Hence, "normal" data flow uses only two counters instead of three as in the Four Counter machine. The B Counter has been eliminated in this machine.

2. SHIFT LEFT

Elements 121 and 122 actually enable SAD9 to be generated, and elements 128 and 129 actually enable SDC9 to be generated. To enable SAD9, one of the inputs to OR gate 121 must be logic 1 (0 volts). To enable SDC9, one of the inputs to OR gate 128 must be logic 1. The inputs to these two OR gates come from Inverters I-094, I-101, I-096, and I-105. I-105 will not be discussed because the logic used to complement R1 is the same in both machines. To enable SAD9 in Recall or Repeat, the output of I-094 must be logic 1, so the input to I-094 must be logic 0 (negative). The output of AND gate 093 will be negative when any input is negative. To enable SDC9 in Recall or Repeat, the output of I-096 must be logic 1, so the input to I-096 must be logic 0. The output of AND gate 093 will be negative when any input is negative. The development of SAD9 and SDC9 to shift left, shift up, and shift down is controlled by I-101. To enable SAD9 and SDC9, the output of I-101 must be logic 1, so the input must be logic 0 (negative). This will occur when any input to AND gate 100 is negative.

In further description of the logic to enable SAD9 or SDC9 to be developed, the signal will be considered developed when an input to AND gates A-093, A-100, or A-092 has been proved to be negative.

a. **DIGIT ENTRY.** Shift left is done the same as in the Four Counter machine. For example, in a digit entry, OR gate 060 and Inverter 061 develop MEIL3 which develops M1L4. M1L4 is an input to OR gate 097 to develop SAD9 and SDC9 at the end of R1 time.

b. **DECIMAL ALIGN.** Align shift R1 left is developed the same way as entry shift R1 left except that OR gate 053 and inverter 054 develop MAIL3 which develops M1L4.

c. **ENTRY AND ALIGNSHIFT LEFT OVERFLOW.** If an overflow occurs in entry or align shift R1 left, the overflow is determined by AC AND gate 1224 at the input of the Overflow flip-flop. CDZ4 is the DC input, and ECD2 is the AC input. If there is a digit other than zero in R1 C14, and another digit is entered into R1, then the digit that was in R1 C14 is shifted into D at B15 R1 C14 time in PS7 and no more SAD9 pulses are generated. So the digit stays in the D Counter and is there when HOME1 resets the Common Digit flip-flop. ECD2 transitions positive and sets the Overflow flip-flop. If there is an overflow in align shift R1 left in PS1, it is necessary to terminate the function at the end of PS1. If the function were allowed to continue with an overflowed number, errors could develop. If there is an overflow in PS1 of a function AC AND gate 1103 resets the Common Function FF at the end of PS1. If the overflow FF sets in PS1, AOFL1 is positive and enables A 1103. When the Phase Counter steps off of PS1 to PS2 or PS6, the output of OR gate 029 goes positive and resets the Common Function FF, thus terminating the function.

The overflow which results from align shift R1 left, or shift R2 left in Multiply or Divide is sensed by OR gate 108. Four timing signals at the input of OR gate 108 define C15 time. TFG1 is a convenient signal which transitions to 0 volts in C15 time, and EDPS2 assures that all the multiplier or dividend has been operated upon before RSL03 can be developed. PS73 and PS12 define PS1 or PS3 or PS5. The output of this gate is used to develop RSL03 in C15 time of PS1 in an align shift R1 left, in C15 time of PS3 in a multiply problem, and in C15 time of PS5 in a divide problem if R2 is being shifted left. MSU3 is applied to OR gate 108 to assure that RSL03 won't be developed in PS5 of divide unless R2 is being shifted left. Thus, as long as the machine is subtracting in PS5 of Divide, the gate is inhibited, but when a carry overflow stops the subtract

cycle and shift R2 left begins, MSU3 permits RSL03 to be developed.

Although RSL03 will be developed every PS1, every PS3, and every PS5, it will not interfere with the machine operation in the wrong function.

For example:

Every time the machine goes into PS1, either nothing is done, or MA1L3 (align shift R1 left) is developed. If MA1L3 is developed, the DPS FF must be set, so RSL03 is generated. If the DPS FF is already set when the machine goes into PS1, and MA1L3 is not developed, RSL03 is still generated, but has no effect because the machine does nothing if MA1L3 is not developed.

Every time the machine goes into PS3, either nothing is done (as in the case of a divide problem) and no harm is done by generating RSL03, or R2 is shifted left (as in the case of a multiply problem) and RSL03 will be generated if the DPS FF is set.

Every time the machine goes into PS5 in a multiply problem, either nothing is done, or a count of 1 is added to R2. In either case, it doesn't matter that RSL03 may be developed. Every time the machine goes into PS5 in a divide problem, either RMD is subtracted from R1, and a count of 1 is added to R2, or RMD is added to R1 and R2 is shifted left. If the machine is subtracting in PS5 of Divide, MSU4 inhibits RSL03 to avoid any interaction. If the machine is adding RMD to R1 and shifting R2 left, RSL03 will be developed if the DPS FF is set.

d. **MULTIPLY SHIFT R2 LEFT.** OR gate 048 generates the signal to shift R2 left in a multiply problem, so naturally one input to OR gate 048 is EMU2. Three other inputs, PC12, PC22, and PC41, define PS3. The two timing signals TFE2 and TFF1 define R2 time, and TCX5 limits the columns involved in the shift R2 left to C2 through C14. The only time the output of OR gate 048 goes negative (logic 0) is in PS3 of Multiply, and only during the R2 times between C2 and C14. The output of OR gate 048 is applied to AND gate 100 and inverter 101 to enable the generation of SAD9 and SDC9.

e. **DIVIDE SHIFT R2 LEFT.** OR gate 039 is used to generate SAD9 and SDC9 to shift R2 left in Divide. EDV2 is, of course, one input to OR gate 039. Another input is ACOF2. The Carry Overflow flip-flop is set in Divide at the end of the subtract cycle because there is an overdraft. Per the Three Counter machine Divide Flow Chart in Figure 5-3, the next thing to be done is shift R2 left and add RMD to R1. OR gate 039 takes care of shifting

DIVIDE FLOW CHART (3 COUNTER EC-130)

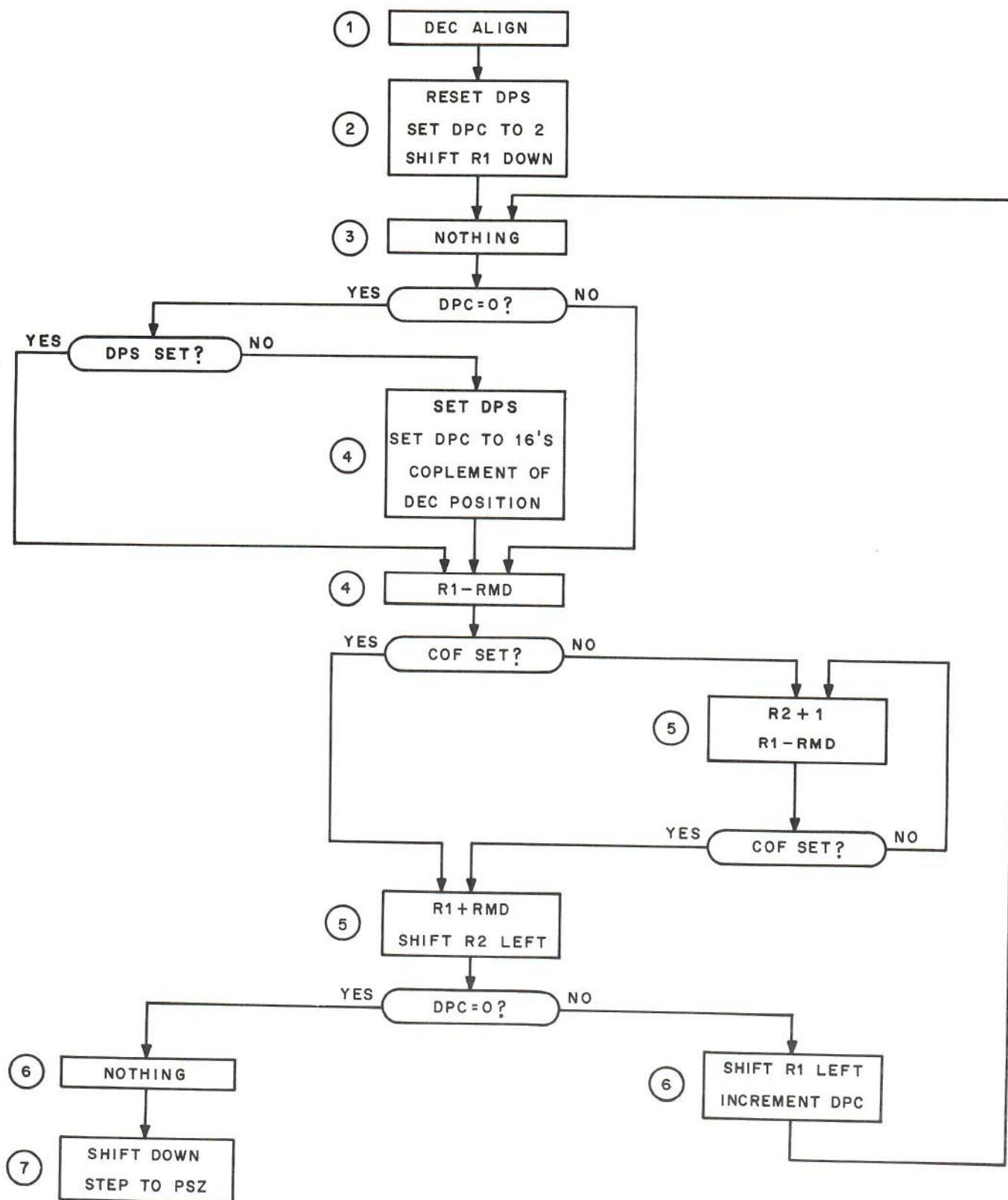


Figure 5-3

R2 left in PS5. TFF1 and TFE2 define R2 time, and TCX5 defines C2 through C15 times.

3. SHIFT UP

Shift up in the Three Counter machine is much the same as in the Four Counter machine. With normal (idle) data flow from the A Counter to the C Counter, to shift up, the data must be shifted from the A Counter to the D Counter, and from the D Counter to the C Counter. Timing is the same in this machine as in the earlier model EC-130. There are three ways to utilize the shift up feature; Repeat, Recall, and the first entry of a digit entry.

a. REPEAT FUNCTION. The Entry Encoder code for Repeat is a binary three. This is reflected in OR gate 090, which is used to generate SAD9; and OR gate 091, which is used to generate SDC9. Both these gates have EEN12 and EEN22 as inputs. (Actually, these two signals alone define a code of three or a code of seven, but since the code seven isn't used, it isn't necessary to have EEN41 on the gates.) The only other input on OR gate 090 is PS64, so SAD9 will be generated every R time in PS6. PS64 is also an input to OR gate 091. But, OR gate 091 also has three other inputs. TC03 assures that SDC9 will not be generated in C0 time (which would create sync pulse problems), TFG1 inhibits SDC9 during RS and RMD times, and TR13 inhibits SDC9 during R1 time. Thus, data is preserved in RS, RMD, and R1 times, and R2, R3, and R4 data is shifted up. This logic is nearly identical to that in the earlier machine.

b. RECALL FUNCTION. Recall is gated by an Entry Encoder code of one. So the two OR gates

used to develop SAD9 and SDC9 in recall will have EEN12, EEN21, and EEN41 as inputs. OR gate 089 (used to develop SAD9) has two other inputs; PS64 defines PS6, and TR03 inhibits the development of SAD9 in RMD time. OR gate 088 also has two other inputs. PS64, as in OR gate 089, and TC03, which inhibits SDC9 to preserve the sync pulse in B3 R3 C0 time. This logic is nearly identical to the Recall logic in the Four Counter EC-130.

c. SHIFT UP IN THE DIGIT ENTRY OPERATION. Shift up in a digit entry is gated by OR gate 099. Since the Entry Encoder is not set in a digit entry, no Encoder signals are applied to OR gate 099. Thus, the logic for OR gate 099 is identical to that in the earlier EC-130.

4. SHIFT DOWN

Shift down in this machine is radically different from the method used in the Four Counter machine. A shift down in the normal sense of the word cannot be done because there is no counter which can be bypassed. Shift down in the new EC-130 is a rather more complex idea and a correct concept of timing becomes of paramount importance.

Figure 5-4a shows a portion of the data in a machine as organized on the delay line. Figure 5-4b shows the same data AFTER shifting down R1, R2, R3, and R4. Note that the data that was in R1, R2, R3, and R4 is now 48 μ s closer to the sync pulse than before the shift down. In fact, whether a digit is in RS, RMD, R1, R2, R3, or R4 depends solely upon its proximity to the sync pulse.

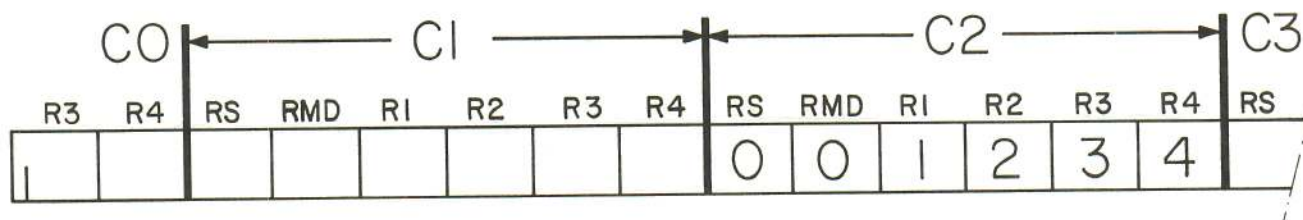


Figure 5-4a

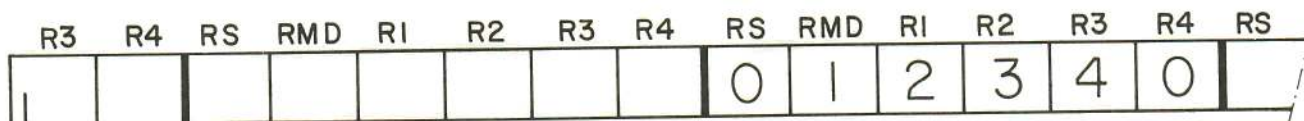


Figure 5-4b

Look at Figure 5-5a. If a single pulse is 480 μ s from the sync pulse, it MUST be in R1 C2 time. The act of shifting R1 down merely moves that pulse 48 μ s closer to the sync pulse. In Figure 5-5b, that pulse is only 432 μ s from the sync

pulse. Hence, it MUST be in RMD C2 time. It has been shifted down. Now a general (but important) statement can be made. TO SHIFT DATA DOWN, IT IS NECESSARY ONLY TO MOVE THAT DATA 48 μ s CLOSER TO THE SYNC PULSE.

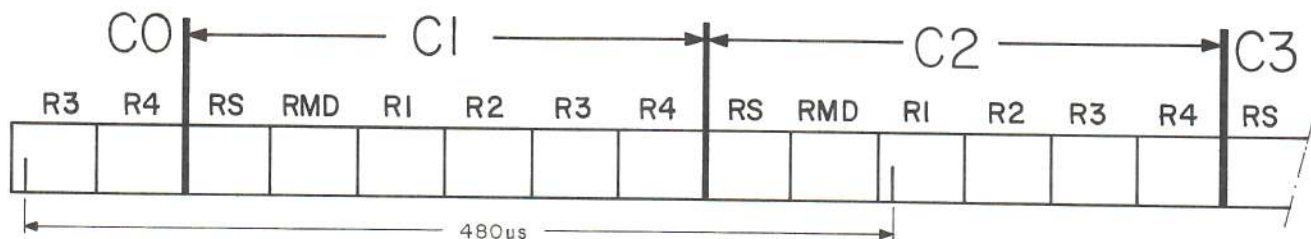


Figure 5-5a

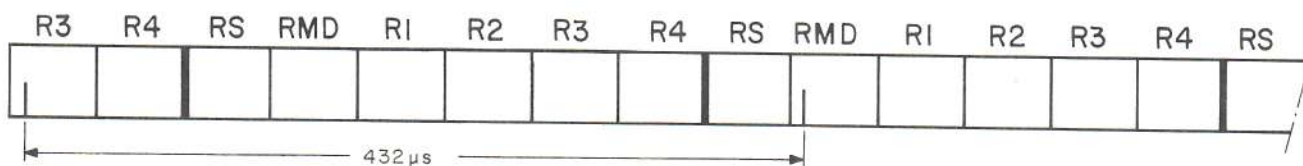


Figure 5-5b

Would the result be the same if the sync pulse were moved closer to the data? At first glance one would say, no! But, look closely at Figure 5-6a which shows the sync pulse in B3 R3 C0, a pulse in B3 R1 C2 (480 μ s from the sync pulse), and a pulse in B3 R2 C2 (528 μ s from the sync pulse). Now suppose the sync pulse is shifted up

to B3 R4 C0, as drawn in Figure 5-6b. This time the sync pulse is moved 48 μ s closer to the data instead of vice versa. It appears that there is no change in the position of the data, but now the first pulse (in B3 R1 C2) is only 432 μ s and the second is only 480 μ s from the sync pulse. When these three pulses count back onto the delay line

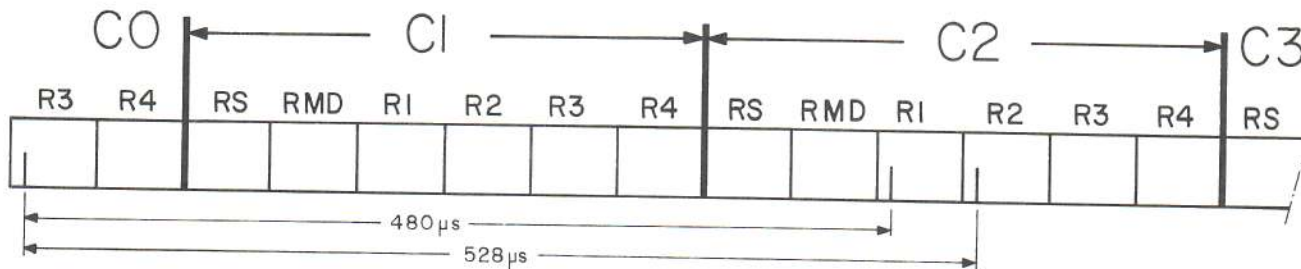


Figure 5-6a

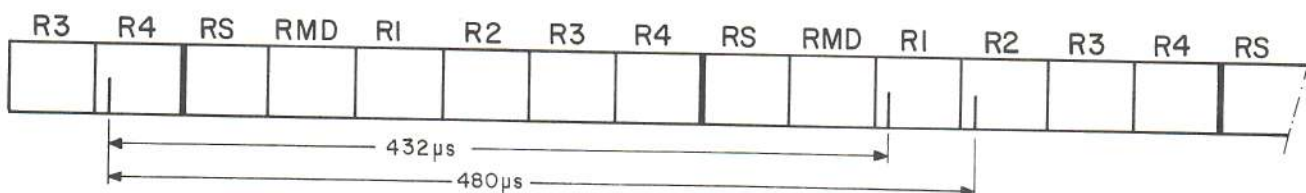


Figure 5-6b

they maintain this time relationship. When the sync pulse counts back off the delay line it is re-established in B3 R3 C0 (Figure 5-6c) time. So the nearest pulse, only 432 μ s later, MUST be in

RMD C2 time, and the second, 480 μ s from the sync pulse, MUST be in R1 C2 time. Clearly, shifting up the sync pulse has the same effect as shifting down data.

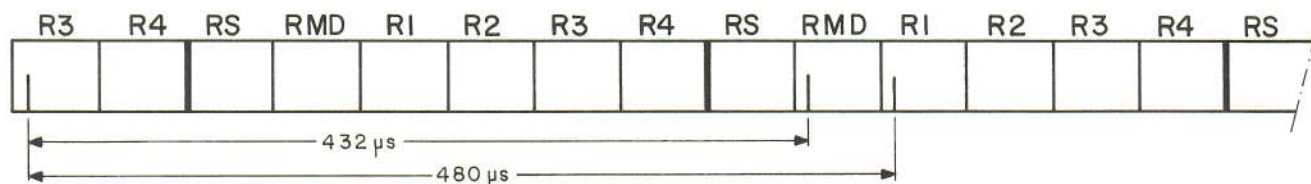


Figure 5-6c

The problem now is that shifting up the sync pulse shifts down ALL data including RS. Fortunately, it is a simple matter to correct this. If RS is shifted up to RMD in the same line pass that the sync pulse is shifted up, then in the next line pass when all data is resynchronized 48 μ s early, the original RS data will still be in RS time. For example, suppose there is data in C2 as shown in Figure 5-7a, and R1, R2, R3, and R4 are to be shifted down in a Clear Entry function. Shift down in Clear Entry is done in PS6, so in PS6 when the sync pulse counts off the delay line, it synchronizes the timing chain, thus establishing itself in B3 R3

C0 time, and establishing All data in their proper times. Then the sync pulse is shifted up (delayed 48 μ s) into R4 C0 time. Since the timing chain is already running, this has no effect on the data as it counts off the delay line. As this data comes off the delay line, all RS data is shifted up (delayed 48 μ s) into RMD time (see Figure 5-7b). When the sync pulse counts off the delay in the next line pass (PS7), it resynchronizes the timing chain so that all data is shifted down, and the RS data that was shifted up into RMD is once again in RS time. R1, R2, R3, and R4 data are shifted down as shown in Figure 5-7c.

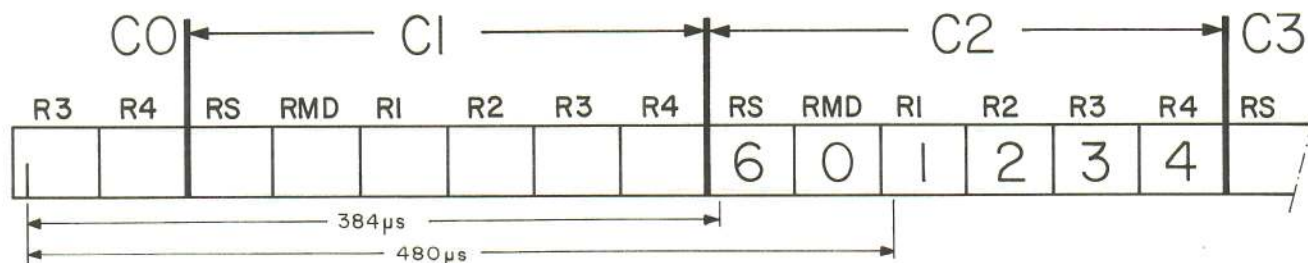


Figure 5-7a

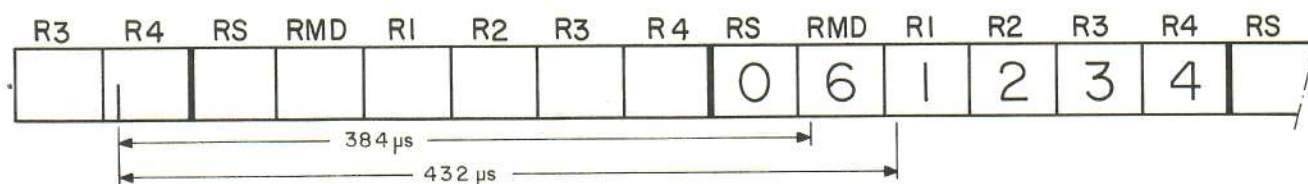


Figure 5-7b

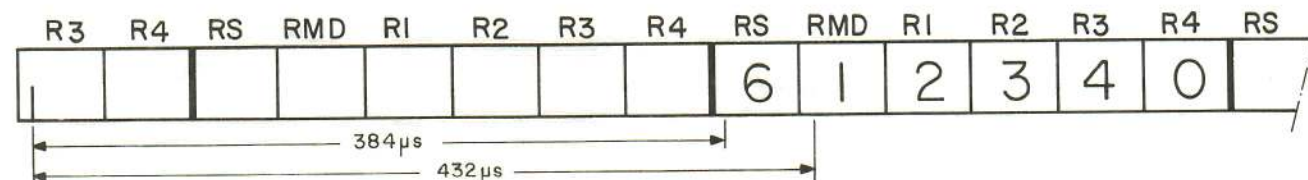


Figure 5-7c

a. SHIFT DOWN R1, R2, R3, R4 IN CLEAR ENTRY, ADD, SUBTRACT, MULTIPLY AND DIVIDE. This, then, is the basic theory of shift down. The operation just described occurs in PS6 of Clear Entry. But the same thing happens in PS6 of the Add, Subtract, and Store functions as well as in the Clear Entry function. The two OR gates that are used to shift up the sync pulse and RS are OR gate 310 and OR gate 304. OR gate 310 is used to generate SAD9 and SDC9 in C0 time to shift up the sync pulse in the Clear Entry, Add, Subtract, and Store functions. PS64 is one input to OR gate 310 and enables the sync pulse to be shifted up only in PS6. EEN42 is another input because the only time EEN4 FF is set is in any one of the above functions. The third input to OR gate 310 is TC04. Thus, OR gate 310 enables SAD9 and SDC9 to be developed in R3 C0 and R4 C0. OR gate 304 enables SAD9 and SDC9 to be developed in RS and RMD of all C times to restore RS to its original position with respect to the sync pulse. There are three inputs to OR gate 304: EEN42 gates for Add, Subtract, Store, or Clear Entry, and PS64 gates for PS6. TFG2 inhibits the OR gate during R1, R2, R3, and R4 times. So OR gate 304 enables SAD9 and SDC9 during RS and RMD times. This will put RS data in RMD time and leave RMD data in the D Counter. If this is left in the D Counter, it will be placed in the next RS time when the next SAD9 and SDC9 are developed. Hence, CRD9 must be developed to clear RMD out of the D Counter. OR gate 305 will enable CRD9 when its output is logic 0 (negative). Two inputs to O-305 are EEN42 and PS64, the same as on O-304. TR14 is the third input to O-305. This means that when O-304 is gating SAD9 and SDC9 to shift RS up, O-305 enables CRD9 to reset the RMD data out of the D Counter in the following R1 time.

The net effect of the operation of OR gates 310, 304, and 305 is that R1, R2, R3, and R4 are shifted down, and RS remains in RS in the Add, Subtract, Store, and Clear Entry functions.

b. SHIFT DOWN R1 IN MULTIPLY AND DIVIDE. To shift down R1, R2, R3, and R4 in PS7 of Multiply or Divide, OR gates 308, 302, and 303 are operated. OR gate 308 enables the sync pulse to be shifted up only in PS7 of Multiply or Divide. OR gate 302 is responsible for enabling SAD9 and SDC9 in RS and RMD of all column times to shift up RS in PS7 of Multiply or Divide. (TFG2 is negative during RS and RMD times). As before, the RMD data must be cleared out of the D Counter each column time, and OR gate 303 enabled CRD9 to be generated at the end of each R1 time in PS7 of Multiply or Divide.

To shift down R1 and clear R1 to zero in PS2 of Multiply or Divide, it is necessary to shift up

the sync pulse, then shift up RS, R2, R3, and R4 causing that data to remain in synchronization to keep it where it was. This puts R1 in RMD. Two OR gates are used to accomplish this. OR gate 306 enables SAD9 and SDC9 in each R time of PS2 except R1 time. (Remember that the only time the machine steps to PS2 is in Multiply or Divide, and we ALWAYS want to shift R1 down to RMD in PS2.) This means that all R times except R1 time are shifted up with the sync pulse. This puts all R times except R1 in their original positions with respect to the sync pulse. R1 is 48 μ s closer to the sync pulse, which is effectively a shift down of R1, however, the method described has a drawback. SAD9 and SDC9 are generated for each R time except R1. At the end of RS time, SAD9 and SDC9 are generated, and RS data goes to the D Counter. Whatever was in the D Counter goes to RS time in the C Counter. At the end of RMD time SAD9 and SDC9 are again generated; RMD data goes to the D Counter, and RS data goes to RMD time in the C Counter. SAD9 and SDC9 are inhibited in R1 time so the RMD data stays in the D Counter. At the end of R2 time SAD9 and SDC9 are again generated; R2 data is shifted into the D Counter, and the contents of the D Counter (RMD data) is shifted into R2 time. This means that in the next line pass when the results of shifting up the sync pulse are seen, R1 will have been shifted down to RMD as expected, but RMD will have been shifted up into R1. This is grossly wrong! R1 must be cleared out so that the multiplier or dividend in R2 can be shifted into R1, digit by digit. If RMD is shifted into R1, it will appear to the machine that the RMD data is the most significant part of the multiplier or dividend. Clearly, RMD must not be allowed to reach R1 time. The easiest way to stop it is to reset the D Counter to zero when RMD data is present in the D Counter. Then when SAD9 and SDC9 are generated at the end of R2 time, zeros will be shifted into R2. The RMD data is shifted into the D Counter at B15 RMD time and the next SDC9 will occur at B15 R2 time. Between these two times, the D Counter must be reset to zero. The obvious time to do this is B15 R1 time. OR gate 050 enables CRD9 in each R1 time in PS2. The three Phase Counter signals define PS2, and TR14 defines R1 time. No other signals are necessary because the only time the machine is in PS2 is in Multiply or Divide.

c. STORE FUNCTION. Shift down in Store is a little different because R1 data must be advanced twice. This means that the sync pulse must be shifted up twice in addition to shifting up other R times to keep them in the right position with respect to the sync pulse. OR gates 310, 304, and 312 are used to accomplish this.

You are already familiar with the operation of OR gates 310 and 304. They are used to shift down

R1, R2, R3, and R4 in Add, Subtract, Clear Entry, and Store. These two gates put R1 data in RMD time, R2 data in R1 time, R3 data in R2 time, and R4 data in R3 time. R4 is left empty. This takes one line pass and is done in PS6. The only thing remaining to be done is to put the data now in RMD into RS, but it is equally important NOT to further shift down all the other R times. Since shifting the sync pulse up is the same as shifting ALL data down, in addition to shifting up the sync pulse, we must shift up all R times except RMD. OR gate 312 performs this operation in PS7 of Store. EEN42 and EEN22 define the Store function, PS74 gates for PS7, and TR03 inhibits the output during RMD time. Hence, OR gate 312 enables SAD9 and SDC9 for the sync pulse, RS, R1, R2, R3, and R4.

In conclusion, shift down is not difficult to understand as long as the student thoroughly understands basic data organization.

F. ADD FUNCTION

To begin the Add function the Entry Encoder must first be set to a binary code of five. This is the code for both the Add and Subtract functions and corresponds to setting the Add or Subtract FF in the Four Counter machine.

1. ENTRY ENCODER LOGIC

When the Add switch is closed, 0 volts is applied to OR gates 322 and 324. This 0 volts enables AC AND gates 1663 and 1681 to set EEN4 FF and EEN1 FF, respectively. EKBD3 is the AC input to all the gates which set the Entry Encoder flip-flops, so after about 6 ms the Entry Encoder is set to a binary code of five.

When the Phase Counter steps to PS1, OR gate 053 will develop MAIL3 until R1 is decimal aligned, then the Phase Counter will jump to PS6.

2. SIGN CONTROL LOGIC

In PS6, two things are done:

(a) The Sign Control FF checks the signs of R1 and R2 to determine if the ultimate operation will be an addition or subtraction. The Sign Control FF is normally clamped in the set condition during machine idle by ERF3 applied to ASC1 as an override set. If the flip-flop is still set at the beginning of PS7, the machine will add; if it is in the reset condition at the beginning of PS7, the machine will subtract. OR gate 007 samples the signs of R1 and R2, and to do this it must have several inputs. EEN12 and EEN42 gate for an Add or Subtract function. TC14 and PS64 limit the sampling to C1 time of PS6. TFF1 further limits the

sampling to R1 and R2 times, and XRDL4 provides the actual sign information from the delay line. If all these conditions are met, and there is a minus sign in R1 or in R2, the output of OR gate 007 will go negative (logic 0) for about 1 μ s. This negative transition is inverted by I-008 and will reset the Sign Control FF. If the Sign Control FF remains reset, the machine will subtract. But if there are minus signs in both R1 and R2, there will be two transitions at the output of OR gate 007; the first will reset the flip-flop, and the second will set it again, and the machine will add. If both the signs of R1 and R2 are positive, there will be no transitions to reset the flip-flop and the machine will add. It will be assumed that the Sign Control FF is in the set condition at the end of PS6.

(b) The second thing which occurs in PS6 is the shift down of R1, R2, R3, and R4. Recall that this is accomplished by shifting the sync pulse up, which is the same as shifting everything down. Then RS is shifted up to put the RS data back in RS time. Since both are done in the same line pass, it appears (and indeed is true) that the sync pulse is shifted up to B3 R4 C0, and that each RS data is shifted up into RMD time. But when the sync pulse counts off the delay line in PS7, it is re-established in B3 R3 C0 time (48 μ s earlier than it was in PS6 after the shift up), and thus ALL data is re-established 48 μ s earlier in PS7. This amounts to a shift down of R1, R2, R3, and R4. OR gate 310 enables SAD 9 and SDC9 when its output is negative. Its output will be negative in C0 time of PS6 in Add or Subtract. OR gate 304 enables SAD9 and SDC9 in each RS and RMD time of PS6 in Add or Subtract. (Additional shift down information can be obtained under Topic E4).

3. DEVELOPMENT OF MAD4

In PS7 the actual addition is done. Once again assuming that the Sign Control FF was in the set condition at the end of PS6, ASC2 is negative and ASC1 is positive. Because ASC1 is positive at the input of OR gate 023, MSU4 cannot be generated, but ASC2 is negative and is an input to OR gate 021. When the output of OR gate 021 goes negative MAD4 will be generated. The other three inputs to OR gate 021 define PS7 and the Add or Subtract functions. In either an Add or Subtract function, the Entry Encoder is set to a binary code of five, hence the use of EEN12 and EEN42. So the only time the output of OR gate 021 will be negative is in PS7 of an Add or Subtract function when the Sign Control FF is set. ASC2 assures that the function is Add instead of Subtract. When the output of O-021 goes negative, it causes MAD4 to be developed by I-020.

4. OVERFLOW

If the addition yields an overflow, the overflow is sensed by the setting of the Carry Overflow FF. ACOF1 is the AC input to AC AND gate 1221 on the Overflow FF. The DC input to 1221 is MA1S3. Anytime the Carry Overflow FF sets in an Add function, the Overflow FF will be set by AC AND gate 1221. (Note: OR gate 311, which generates MA1S3 in a Divide, cannot cause MA1S3 to be generated before the Carry Overflow FF is set (ACOF2 negative). This means that ACOF1 has already transitioned positive BEFORE MA1S3 can go positive. Hence, in a Divide, the trigger occurs before the DC enable, and AC AND gate 1221 cannot set the Overflow FF.)

G. SUBTRACT FUNCTION

The basic Subtract function is the same as in the earlier EC-130, however, there are some changes, mainly caused by using the Entry Encoder.

1. ENTRY ENCODER LOGIC

The Entry Encoder is set exactly the same way as in Add. When the Subtract switch is closed, the diode connecting it to the Add switch becomes forward biased to permit EEN4 FF and EEN1 FF to be set by EKBD3. The Subtract switch output is also used as a DC enable to AC AND gate 1143 (Sign Control FF). When EKBD3 transitions positive, A-1143 will reset the Sign Control FF. If the Sign Control FF stays reset, the machine will subtract. Whether the Sign Control FF stays reset will depend upon the result of checking the signs of R1 and R2 in PS6.

When the Phase Counter steps to PS1, an align shift R1 left will be generated if necessary by OR gate 053. After the alignment is completed, the Phase Counter jumps to PS6.

2. SIGN CONTROL AND SHIFT DOWN LOGIC

In PS6 two things will be accomplished. The Sign Control FF checks the signs of R1 and R2 to determine whether the ultimate operation will be an addition or a subtraction. Recall that the Subtract switch reset the Sign Control FF at the beginning of the function. If the Sign Control FF is in the reset condition at the end of PS6, a subtract operation will be performed; if it is in the set condition at the end of PS6, the machine will add.

There are six inputs to OR gate 007 to gate for the signs of R1 and R2. EEN12 and EEN42 define the Add or Subtract functions. PS64 limits the sampling to PS6 time and TC14 further limits the sampling to column one. TFF1 is negative only during R1 and R2, so the only time the output of

O-007 can possibly go negative (logic 0) is during R1 or R2 of C1 time in PS6 or an Add or Subtract function. If there is a pulse in R1 C1 time it means that the sign of R1 is negative. If the sign of R1 is negative, XRDL4 will transition negative in R1 C1 time and the output of O-007 will go negative. This is inverted by I-008 whose output is applied to the T input of the Sign Control FF. Since the flip-flop is already reset, the output of the inverter will set the flip-flop. If the Sign Control FF stays set, the machine will add. If, however, there is a minus sign in R2 as well as in R1, the output of I-008 will transition positive twice, resetting the flip-flop with the second pulse, and the machine will subtract.

R1, R2, R3, and R4 are shifted down. The machine does this by shifting up the sync pulse and RS. The sync pulse is shifted up by gating to enable SAD9 and SDC9 during each R time of C0 time. OR gate 310 accomplishes this. EEN42 gates for the Add, Subtract, Clear Entry, or Store functions. TCO4 enables the OR gate in all R times of C0 time, and PSG4 limits the operation of the gate to PS6 time. So the output of the gate is negative in R3 or R4 of C0 time in PS6 of Subtract. When the output of O-310 is negative, SAD9 and SDC9 are enabled and this results in the shift up of the sync pulse.

OR gate 304 is used to enable SAD9 and SDC9 in RS and RMD to shift up RS. EEN42 and PS64 gate for PS6 of an Add, Subtract, Clear Entry, or Store function. TFG2 is negative during RS and RMD times. So the output of O-304 will be negative to enable SAD9 and SDC9 in each RS and RMD times. At the end of RS time RS is shifted to the D Counter. At the end of RMD time, RMD is shifted to the D Counter, and RS is shifted into RMD time at the C Counter. This leaves RMD in the D Counter. If the RMD data is in the D Counter at the end of the next RS time, this data will be shifted into RS time. To avoid this, the D Counter is reset each R1 time. This is done by OR gate 305. EEN42 gates for Add, Subtract, Clear Entry, or Store. PS64 and TR14 gate for each R1 time in PS6, and the output of O-305 will go negative for 48 μ s at this time. Any negative input to AND gate 309 will cause CRD9 to be developed by elements 144 and 145.

So, OR gates 310, 304, and 305 are operated to shift down R1, R2, R3, and R4 in PS6 of a Subtract problem. (For additional shift down information, see Topic E4.)

3. THE DEVELOPMENT OF MSU4

The actual subtract operation is done in PS7. Again it must be assumed that the Sign Control FF is in the reset condition. If it is, then ASC2 is

positive to inhibit the generation of MAD4. ASC1 is negative. This signal is one of three inputs to OR gate 023 and enables O-023. PS74 gates for PS7, and ACOF1 must always be negative at the beginning of PS7. (The reason ACOF1 is there is because in this machine if it is necessary to complement R1, the complement is done in PS7 instead of in PSZ as in the Four Counter EC-130. Since MSU3 must be inhibited if the complement is being taken, ACOF1 is used to inhibit gate 023 at this time.) Thus, the output of OR gate 023 goes negative for one line pass. This makes the output of AND gate 046 negative and the output of I-070 positive. This signal is MSU3. MSU3 is the input of I-073 and MSU4 is an input to OR gate 071. The output of this gate is inverted and used to inhibit CRA9, and to enable C1D9. MSU4 is also applied to O-146 with TCX5, TRO4, and TB154 to develop SDA9 each RMD time to place the complement of RMD into the A Counter for addition with R1. The rest of the basic subtract logic is identical to that of the earlier EC-130 and will not be covered.

MSU3 is positive at the end of subtract and inhibits the Phase Counter from being stepped to PSZ. But, PS73 and HOME1 are anded at AND gate 1104 to reset the Common Function FF. When ECF1 goes negative ECFD4 goes positive and clamps the Phase Counter to PSZ with the override resets. ECFD4 also generates ERF3 to reset the Entry Encoder FF's and set the Sign Control FF.

4. COMPLEMENT

If the Carry Overflow FF is set at the end of the subtract operation, it is indicative of the necessity to complement R1 and change the sign of R1. Then ACOF1 will be positive at the input to OR gate 016 (which develops ECFD4) and inhibits the generation of ECFD4. ECFD4 stays negative even though the Common Function FF is reset, and thus the Phase Counter is not clamped to PSZ. It stays at PS7, and R1 will be complemented in PS7. There is also one other effect of ECFD4 staying negative. The Sign Control FF stays reset. Normally, if the Sign Control FF is reset in PS7, OR gate 023 will generate MSU3. However, ACOF1 is now positive and inhibits the gate. So the purpose of having ACOF1 as an input to OR gate 023 is to inhibit the subtract operation during the complementing of R1. Of course, after the complement of R1 is completed, HOME1 resets the Carry Overflow FF and ECFD4 (elements 016 and 017) goes positive. This results in clamping the Phase Counter to PSZ, and setting the Sign Control FF with the override set input.

H. CHANGE SIGN OF R1

The logic used in changing the sign of R1 in this

machine agrees with the logic used in the Four Counter machine. The idea is to add a count of one to R1 C1 time. If R1 C1 contains a zero (no minus sign) then the addition of a count of one puts a one (minus sign) in R1 C1. If there is already a count of one (minus sign) in R1, the addition of a count of one puts a two in R1. This count of two is promptly cleared to zero (no minus sign). The count of one is added to R1 C1 time by generating ASA13 to set the A1 FF at the end of RMD C1 time. There are five ways of generating ASA13, and two of them are used to change the sign of R1. These two are described as follows:

1. SUBTRACT FUNCTION

OR gate 081 (located on the logic print between the Phase Counter and the Carry FF) will cause I-111 to generate ASA13 when the output of O-081 goes negative. The first condition is that the Sign Control FF must be reset (which defines a subtract function). This is gated by ASC1. The second condition is that the Carry Overflow FF must be set (showing the necessity of complementing R1 and changing the sign of R1). This is gated by ACOF2. TRO4 and TC14 define RMD C1 time and the output of O-081 will go negative for 48 μ s and cause ASA13 to go positive for 48 μ s. When ASA13 is positive, A1 FF is enabled to be set by CRA9.

Then the contents of R1 C1 can count in on top of the count of one already in the A Counter. If there was nothing in R1 C1 then the new count will be a one (minus sign). Thus, nothing else needs to be done. But if the sign of R1 was already minus with a count of one in R1 C1, then the addition of a count of one will put a two in R1 C1. This is an invalid code for sign information and this "two" must be cleared out to zero (the valid code to show that the sign of R1 is positive). AC AND gate 1297 at the input to the A1 FF detects any invalid code in C1 time. If the A2 FF sets any time in C1 time, it is indicative of an invalid code for the sign information. TC13 is the DC input to A-1297 and limits the operation of the gate to the time that sign information is counting into the A Counter. CA21 is the trigger input to A-1297. If the A2 FF sets, CA21 goes positive and resets the A1 FF. (Recall that in the Four Counter machine this was done in the B Counter, and both the B1 FF and the B2 FF were reset.) In this machine, however, the A2 FF stays set. At the end of R1 C1 time this illegal counter code is shifted to the C Counter. Because the C1 FF and the C5 FF are reset, CCZ3 is positive indicating that the C Counter is zero, and C1C9 is inhibited. Hence, the C2 FF stays set. Complications are avoided by leaving the reset gates on the C2 FF, so that the C2 FF is reset by the succeeding A to C shift of D to C shift if the incoming data is not supposed to have the C2 FF set. If the incoming data is

supposed to have the C2 FF set there is no problem. It is already set.

2. CHANGE SIGN FUNCTION

The other way ASA13 can be used to change the sign of R1 is by operating OR gate 077. When the output of OR gate 077 goes negative, the sign of R1 will be changed as described in Topic H1. OR gate 077 is used in conjunction with the Change Sign Key. When the Change Sign switch is closed, EEN2 FF is enabled to be set by EKBD3. EEN1 FF and EEN4 FF remain reset. In PS1 the data in R1 is decimal aligned if necessary (see Topic E3 for align shift R1 left information). After the decimal alignment, the Phase Counter jumps to PS6. In PS6 the actual change sign operation takes place. OR gate 077 is gated by EEN11, EEN22, and EEN41 for the Change Sign function only. PS64 limits the operation of the gate to PS6. TR14 and TC14 define R1 C1 time so the output of O-077 will go negative only during R1 C1 time in PS6 of a Change Sign function. When the output of this gate goes negative, the sign of R1 is changed as described in Topic G2. In PS7, nothing is done and the machine terminates the function at the end of PS7.

3. MULTIPLY OR DIVIDE FUNCTION

Changing the sign of R1 in Multiply and Divide is explained in the description of those functions.

J. MULTIPLY FUNCTION

The Multiply logic is essentially the same in this machine as in the earlier EC-130. The changes are minor and are a product of a more efficient use of parts.

1. MULTIPLY FLOW CHART

The Multiply Flow Chart is shown in Figure 5-8. (See Foldout Page 23.) This Flow Chart should be compared with the Multiply Flow Chart of the Four Counter EC-130. While there are differences, the operation is done in the same order in both machines. Because of the similarity of operation, learning the Multiply function of the Three Counter machine will present no special problems. The Multiply function is explained by Phase Counter step in the following explanation.

2. DECIMAL ALIGN (PS1)

As in the Four Counter machine, PS1 is devoted exclusively to the decimal alignment of the contents of R1. MAIL3 is developed by elements 053 and 054, and MAIL3 in turn causes MIL4 to be developed. MIL4 is one of four inputs to OR gate 097. TCX5 and TR14 gate for all R1 times from

C2 through C14 (C15 in Divide). Since RSL03 is developed only in C15 time, and O-097 is inhibited in C15 time in a Multiply function, it has no logic function as an input to O-097 in Multiply. So when the output of O-097 goes low, it causes SAD9 and SDC9 to be generated every R1 time in columns C2 through C14 to shift R1 left.

3. CHANGE SIGN OF R1 (PS2)

In PS2 of a Multiply problem the same things must be done that are done in PS2 in the earlier EC-130. First, the sign of R1 is added to the sign of R2. OR gate 051 and inverter 052 are used to generate AIRX3 which inhibits the generation of CRA9 when AIRX3 is logic 1. (The logic used to develop AIRX3 is identical to the logic in the Four Counter machine and will not be further discussed). AIRX3 also is used to reset the DPS FF and to set a count of 4 into the Decimal Point Counter.

4. SHIFT DOWN R1 TO RMD

The other thing done in PS2 is the shift down of R1. To shift down R1, it is necessary to shift up the sync pulse, and all data except R1. In addition, because it is necessary to clear R1 out to zero, CRD9 must be generated each R1 time to reset the RMD data out of the D Counter. If this is not done, RMD data will end up in R1 time. OR gate 306 causes SAD9 and SDC9 to be generated each R time except R1 time in PS2 including R3 C0 time for the sync pulse. This results in the sync pulse and all data except R1 data being shifted down. OR gate 307 is used to clear the RMD data out of the D Counter. The output of O-307 goes negative each R1 time in PS2 and causes CRD9 to be generated each time it goes negative. Developing CRD9 in R1 time clears out the RMD data before it can be shifted into R2 time. (For more detailed information on Shifting Down R1, see Topic E4.)

An overflow in the Multiply function is detected in this machine in the same way as in the Four Counter machine. Once the Decimal Point Counter has been counted to zero, and the DPS FF has been set, RSL03 is developed each PS3 time. If there is any data remaining in the D Counter when RSL03 is developed, CRD9 will clear the D Counter to zero, and the Overflow flip-flop will be set. The function will not be interrupted so the decimal alignment is allowed to continue to its ultimate conclusion. RSL03 is developed by OR gate 108 and Inverter 109. The four timing signal inputs to O-108 limit the operation to R1, R2, R3, and R4 of C15 time. EDPS2 assures that the DPS FF is set, and MSU3 inhibits the gate during a Subtract function. PS73 and PS12 gate for PS1, PS3, or PS5. When the output of I-109 goes posi-

tive, the output of I-143 goes negative to enable CRD9 to be developed. When the output of I-109 goes positive and there is data in the D Counter, AC AND gate 1222 causes the Overflow flip-flop to be set. (For additional Shift Left Overflow information, see Topic E2.)

5. SHIFT R2 LEFT (PS3)

In PS3 of Multiply, the same thing is done in this machine that is done in the Four Counter machine. R2 must be shifted left. Shift R2 left is controlled by OR gate 048 which causes SAD9 and SDC9 to be developed when its output goes negative. PC41, PC22, and PC12 at the input of O-048 define PS3. EMU2 limits the operation of the gate to the Multiply function, and TCX5 inhibits the gate in C0, C1, and C15 times. TFE2 and TFF1 define R2 time, so the output will go negative each R2 time, C2 through C14 in PS3 of a Multiply function.

6. ADD IN MULTIPLY FUNCTION (PS4)

An overflow in a Multiply is detected in PS3 in the same manner used in the Four Counter machine. If there is a digit other than zero in the D Counter when RSL03 is developed, the D Counter will be reset to zero by CRD9, and the Overflow FF will be set by AC AND gate 1222. (For additional shift left overflow information, see Topic E2c.)

Everything that is done in PS4 and PS5 of Multiply in the Four Counter machine is done in PS4 in the Three Counter machine. The first operation occurs at the beginning of PS4. If the Decimal Point Counter is zero, and the Decimal Point Storage FF is reset, the DPS FF will be set by AC AND gate 1133. The enable input to A-1133 is DSZ3. The AC trigger input comes from OR gate O11. The two inputs to O-011 are EMD4 and PC41. EMD4 and PC41 are both negative in PS3 of Multiply, so the output of O-011 is negative. PC41 goes positive at the beginning of PS4 so the output of O-011 goes positive. This positive transition will set the DPS FF if DSZ3 is also positive. When the DPS FF sets, EDPS1 transitions positive. EDPS1 is used to set the Decimal Point Counter to a count of three plus the decimal position.

The add cycles are also done in PS4. To add in a multiply problem, it is necessary to generate MAD4. When the output of OR gate 041 goes negative, MAIM3 goes positive which causes MAD4 to go negative. To get the output of O-041 negative it is necessary to have all inputs negative. EMU2 is always negative in a multiply problem. PC42 and PC22 define PS4 or PS5 (although it will be seen shortly that the entire add cycle is done in

PS4). CDZ3 is negative as long as there is a digit other than zero in the D Counter. When the output of O-041 goes negative, MAD4 is caused to go negative and enables OR gate 074 to develop AIRA3. (For more detailed information on addition see Topic F.)

7. INCREMENT D COUNTER

At the end of each addition in C15 time OR gate 134 causes the D Counter to be incremented. TFH2, TFJ2, TFK2, and TFL2 define C15 time. TR14 defines R1 time, and MAD4 and EMU2 define an addition in a Multiply function. Hence, OR gate 134 will cause the D Counter to be incremented once for each add cycle. The logic for O-134 is the same as in the earlier machine.

8. CARRY OVERFLOW AND CARRY

If there is a carry overflow, or a carry overflow and a carry, R2 is incremented by OR gates 079 and 078 respectively, exactly as in the earlier machine. It should be noted that OR gate 043 inhibits the generation of MAD4 if there is a carry overflow condition. This precludes any possible interaction between an add cycle and a carry overflow condition.

9. STEP TO PS5

The machine will stay in PS4 until the D Counter is incremented to zero. To keep the machine in PS4, MAIM3 is an input to OR gate 024. This inhibits incrementing the Phase Counter until MAIM3 goes negative, and this will not happen until CDZ3 goes positive. Thus, the Phase Counter is locked in PS4 until the D Counter reaches zero.

Normally, nothing is done in PS5. However, if the last add cycle in PS4 yields a carry overflow the count of one will be added to R2 in PS5 instead of PS4.

10. SHIFT R1 LEFT (PS6)

In PS6, R1 must be shifted left if the Decimal Point Counter does not equal zero. OR gate 062 will have a negative output if the Decimal Point Counter is not zero in PS6 of a Multiply or a Divide. When its output is negative, M1L4 is caused to be negative and enables OR gate 097 to develop SAD9 and SDC9 each R1 time of C2 through C14. (For additional shift left information, see Topic E2) M1L4 is also an input to OR gate 059 (input to the Decimal Point Counter). In PS6 when R1 is being shifted left, all inputs to O-059 are negative, and the output is negative. When HOME1 goes positive, the output goes positive and increments the Decimal Point Counter.

Also, in PS6 MMDL3 is positive and is an input to AC AND gate 1154 (at the PC4 FF). HOME1 is the trigger input to A-1154; thus, the same HOME1 that increments the Decimal Point Counter and the Phase Counter also resets PC4 FF. This is the PS6 to PS3 jump. Note that if R1 is shifted left in PS6, the PS6 to PS3 jump MUST be done. But, if the Decimal Point Counter is already zero at the beginning of PS6, then MMDL3 and MIL4 are not developed (DSZ3 is positive at the input to 062). Thus, nothing is done in PS6, and at the end of PS6 the machine goes into PS7 instead of PS3 (MMDL3 is negative at A-1154 and inhibits resetting PC4 FF).

11. SHIFT DOWN IN PS7

In PS7 R1, R2, R3, and R4 must be shifted down. This means that the sync pulse and RS must be shifted up, and that RMD must be cleared out of the D Counter at R1 time. OR gate 308 causes SAD9 and SDC9 to be generated to shift up the sync pulse in C0 time of PS7 in a Multiply or Divide. OR gate 302 causes SAD9 and SDC9 to be developed during each RS and RMD time of PS7 in a Multiply or Divide. OR gate 303 causes CRD9 to be generated each R1 time of PS7 in a Multiply or Divide. (For more detailed information on shift down in PS7 of Multiply, see Topic E4). At the end of PS7, HOME1 steps the Phase Counter to zero, A-1104 causes the Common Function FF to be reset, and the machine comes out of the Multiply function.

12. CONCLUSION AND SUMMARY

In general, the Multiply functions of both types of EC-130 are the same. Specific operations are done in the same order. This can be verified by a comparison of the two Multiply Flow Charts. The only difference of any significance is that the add cycles are done in PS4 instead of in PS5. In the earlier machine, PS4 was a "dead time" in which nothing was done for 5 milliseconds. Now the "dead time" is in PS5. Of course some of the logic used to accomplish these similar operations is somewhat different, but if anything, the logic is simpler and easier to understand than in the earlier machine. Furthermore, some of the logic is unchanged at all thereby putting the machine in a light of familiarity.

K. DIVIDE FUNCTION

Division in the new model EC-130 is much the same as division in the earlier Model EC-130. The same operations must be done and in the same sequence.

1. DIVIDE FLOW CHART

Figure 5-9 (see Foldout Page 25) shows the Divide Flow Chart which is very similar to the Divide Flow Chart of the Four Counter machine. Note that PS1 and PS2 are identical in both machines. However, in PS3 there is a difference. In the later Model EC-130 there is no subtraction done in Step 3. Instead the first subtract is done in PS4, and each subsequent subtraction is done in PS5. Note that the operation is the same in both machines; only the phase step may be different. PS6 and PS7 are also the same in both machines. In the Division function the Entry Encoder is not used because there is a Divide FF which is controlled by the divide switch. The function begins when the Divide FF and the Common Function FF are set.

2. DECIMAL ALIGN (PS1)

The following description of the Divide function will be by Phase Counter step.

In PS1 of Divide, as in PS1 of all functions, only align shift R1 left is accomplished. In order to align it is necessary to develop MAIL3 and MIL4. The development of these two signals is controlled by OR gate 053. The signals PC41, PC21, and PC12 define PS1. ECF2 is negative because the Common Function FF is set. DSZ3 will be negative if R1 must be shifted left for alignment. If all five inputs to OR gate 053 are negative, the output will be negative. This causes MAIL3 to be positive, and causes MIL4 to be negative. MIL4 is one of four inputs to OR gate 097. The output of O-097 will be negative each R1 time C2 through C14 times. A negative at the output of O-097 causes SAD9 and SDC9 to be generated (for additional, more complete information on align shift R1 left see Topic E2).

3. CHANGE SIGN OF R1 (PS2)

In PS2 of the divide problem the same things must be done that are done in PS2 in the earlier EC-130. First, the sign of R1 is added to the sign of R2. OR gate 051 and inverter 052 are used to generate AIRX3 which inhibits the generation of CRA9 when AIRX3 is logic 1. AIRX3 is also used to reset the DPS FF and to set a count of four into the Decimal Point Counter.

4. SHIFT DOWN R1 to RMD

In addition, R1 is shifted down in PS2. To shift down R1, it is necessary to shift up the sync pulse, and all data except R1. Also, because it is necessary to clear R1 out to zero, CRD9 must be generated each R1 time to reset the RMD data out

of the D Counter. If this is not done, RMD data will end up in R1 time. OR gate 306 causes SAD9 and SDC9 to be generated each R time except R1 in PS2 including R3 C0 time for the sync pulse. This results in the sync pulse and all data except R1 data being shifted up. OR gate 050 is used to clear the RMD data out of the D Counter. The output of O-050 goes negative each R1 time in PS2, and causes CRD9 to be generated each time it goes negative. Developing CRD9 in R1 time clears out the RMD data before it can be shifted into R2 time. (For more detailed information on shifting down R1 in Divide, see Topic E4.)

(NOTE: No operation is done in PS3 of Divide.)

5. SUBTRACT IN DIVIDE FUNCTION (PS4)

Everything that is done in PS3 and PS4 of Divide in the Four Counter machine is done in PS4 in the Three Counter machine. The first operation occurs at the beginning of PS4. If the Decimal Point Counter is zero, and the Decimal Point Storage FF is reset, the DPS FF will be set by AC AND gate 1133. The enable input to A-1133 is DSZ3. The AC trigger input comes from OR gate 011. The two inputs to O-011 are EMD4 and PC41. EMD4 and PC41 are both negative in PS3 of Divide so the output of O-011 is negative. PC41 goes positive at the beginning of PS4 so the output of O-011 goes positive. The positive transition will set the DPS FF if DSZ3 is also positive. When the DPS FF sets, EDPS1 transitions positive. EDPS1 is used to set the Decimal Point Counter to a count of three plus the number of the decimal position.

The first subtract cycle is also done in PS4. This subtract cycle corresponds to the subtract cycle in PS3 of the Four Counter of the EC-130. To do a subtract cycle in Division it is necessary to generate MSU3 and MSU4. OR gate 045 has four inputs. PC42 and PC21 define PS4 or PS5. EDV2 is negative in a Divide function, and ACOF1 will be negative as long as there is no overdraft. The output of O-045 will be negative when all inputs are negative and will cause MSU3 to be positive and MSU4 to be negative. MSU3 is applied as an input to OR gate 142 to enable CRD9 to be developed. Since in the subtract cycle RMD data is counted into the D Counter serially, it is necessary to reset the D Counter at the end of each RMD time. MSU4 is applied to OR gate 071 with TCX5 and TRO4. These three signals will cause the output of O-071 to be negative each RMD time C2 through C14. When the output of O-071 is negative, CRA9 will be inhibited. MSU4 is also applied as an input to OR gate 146 with TCX5, TRO4, and TB154. SDA9 will be developed when all four of these signals are negative. The logic of the remainder of the subtract cycle is identical to that in the Four Counter ma-

chine with one exception. If the subtract cycle yields an overdraft, it will be necessary to reset the D5 FF at the beginning of HOME1. In the earlier machine this was enabled by CED55, but in this machine it will be enabled by the signal MSU3.

6. STEP TO PS5

It is impossible to have more than one subtract cycle in PS4 of Divide because the Phase Counter is not inhibited from stepping to PS5. MSU3 is one input to OR gate 024 (the input to the Phase Counter). While it is true that MSU3 is positive during the subtract cycle and inhibits HOME1 from incrementing the Phase Counter, MSU3 is also applied as a DC input to AC AND gate 1171. The AC input to this gate is HOME1. When the output of A-1171 transitions positive it will set PC1 FF. This steps the Phase Counter from PS4 to PS5. However, it is now impossible to further increment the Phase Counter until MSU3 goes negative. Hence, the first subtract cycle is done in PS4 while all subsequent subtract cycles must be done in PS5.

7. INCREMENT R2 (PS5)

In PS5 the remainder of the subtract cycles are done, and for each subtract cycle completed, R2 will be incremented by one. This corresponds to the subtract cycles and the generation of the answer in PS4 of Divide in the Four Counter machine. If the subtract cycle in PS4 did not yield an overdraft, MSU3 will continue to be developed by OR gate 045 until there is an overdraft and ACOF1 goes positive to inhibit the generation of MSU3. ACOF1 is also an input to OR gate 080. This OR gate is used to generate ASA13 to increment R2 in Divide. If there was an overdraft in PS4 the Carry Overflow FF would have been set at the end of PS4, ACOF1 would be positive, and it would have inhibited incrementing R2 as well as inhibiting the generation of MSU3. However, if the subtract cycle in PS4 did not yield an overdraft, a successful subtraction was completed. Hence, each successive subtract cycle in PS5 will cause R2 to be incremented by one, whether or not the subtract cycle yields an overdraft. OR gate 080 will have a negative output in PS5 of Divide if the Carry Overflow FF is not set. PC42, PC21, and PC12 gate for PS5. TC24 gates for the least significant digit column, and TR14 gates R1 time. OR gate 080 gates for R1 time instead of R2 time because the count of one will be set into the A Counter at the end of R1 time by the CRA9 signal.

The final subtract of the subtract cycle yields an overdraft. Since the Carry FF is set in C15 time, and CRD9 is developed each R time, a 9 will be set into the D Counter with ACRY1 and CRD9. This 9 must be cleared to zero, so MSU3 and HOME1 are used as inputs to AC AND gate

1308 to reset the D5 FF. MSU3 takes the place of CED55 in the Four Counter machine.

8. RESTORE OVERDRAFT (Add in Divide)

When the final subtract cycle yields an overdraft, the Carry Overflow FF is set by HOME1. Since ACOF1 is an input to OR gate 045, MSU3 will go negative at the beginning of HOME time. But MSU3 does not go negative until after HOME1 has gone positive. Therefore, the Phase Counter cannot be incremented to PS6 by this HOME time, and the machine will stay in PS5 for one more line pass. The machine uses this additional line pass in PS5 to clear out the overdraft by adding RMD to R1 and to shift R2 left. RMD is added to R1, and R2 is shifted left in the same line pass. To add RMD to R1 it is necessary to generate MAD4. This is done with OR gate 039. OR gate 039 has two inputs. EDV2 is negative in any divide problem and ACOF2 is negative when the final subtraction yields an overdraft. When the output of OR gate 039 is negative MAD4 will be generated.

Also, when RMD is added to R1 in PS5, the Carry FF is again set in C15 time. If the DPS FF is set, RSL03 (OR gate 108) will be developed to enable CRD9 to be generated. When CRD9 is generated and the Carry FF is set, a 9 is put into the D Counter as before. But in this line pass, the machine is adding and shifting R2 left. A nine in the D Counter in C15 time would be shifted into R1 in PS6 to possibly give an incorrect answer. In the Four Counter EC-130, this nine was cleared out of the D Counter by having RSL05 develop CED55 to enable HOME1 to reset the D5 FF. In the new version of the machine, RSL03 resets the Carry FF so that the D Counter will be reset to zero by CRD9 in C15 time. (For additional, more detailed information about Addition see Topic F.)

9. SHIFT R2 LEFT (PS5)

To shift R2 left in PS5 of Divide it is necessary to generate SAD9 and SDC9. These two signals are caused to be generated in PS5 of Divide by OR gate 311. OR gate 311 has six inputs. EDV2 is negative in Divide, ACOF2 is negative in an overdraft condition, and DSZ3 is negative as long as the Decimal Point Counter is not zero. (If the Decimal Point Counter is zero the problem is completed and it will be unnecessary to shift R2 left any further.) TCX5 defines all C times from C2 through C15. TFE2 and TFF1 defines R2 time. Therefore, the output of OR gate 311 will be negative each R2 time, C2 through C15 time of PS5 in Divide. (For more detailed information on shifting R2 left in Divide, see Topic E2.) Please note that R2 is shifted left and RMD is added to R1 in the same line pass. There is no inter-action because the D Counter is not used in Addition.

10. OVERFLOW IN DIVIDE

An overflow in Divide is detected in PS5 in the same manner used in the Four Counter machine. If there is a digit other than zero in the D Counter when RSLO3 is developed, the D Counter will be reset to zero by CRD9, and the Overflow FF will be set by AC AND gate 1222. (For additional Shift Left Overflow information, see Topic E2.)

11. SHIFT R1 LEFT (PS6)

Machine operation in PS6 will be determined by the condition of the Decimal Point Counter. A count other than zero in the Decimal Point Counter indicates that the divide problem is not complete or decimal aligned in R2. Therefore, R1 must be shifted left, the Decimal Point Counter must be incremented, and a jump from PS6 to PS3 must be initiated. Shifting R1 left in PS6 of Divide is controlled by OR gate 062. OR gate 062 has three inputs; EMD4 is negative in Divide, PS64 is negative in PS6, and DSZ3 is negative if there is a count other than zero in the Decimal Point Counter. When the output of OR gate 062 goes negative M1L4 will be caused to go negative. M1L4 is one of four inputs to OR gate 097 which controls SAD9 and SDC9 to shift R1 left. (For more detailed information in shifting R1 left in Divide, see Topic E2.) M1L4 is also an input to OR gate 059. The output of OR gate 059 will increment the Decimal Point Counter when there is a transition from negative to positive. For this transition to occur, M1L4 must first be negative. Then the Decimal Point Counter can be incremented once at the end of each shift R1 left in Divide.

If, on the other hand, the Decimal Point Counter is already zero at the beginning of PS6, then nothing will be done in PS6 because the divide problem has been completed and is already decimal aligned in R2. In this case, shift R1 left is inhibited by the signal DSZ3 at the input to OR gate 062. This signal is positive, therefore, the output of the OR gate is positive. So MMDL3 must be negative and M1L4 must be positive. Because MMDL3 is negative AC AND gate 1154 is inhibited from resetting the PC4 FF at the end of PS6. Since the PC4 FF is not reset at the end of PS6, this means that the Phase Counter steps from PS6 to PS7, instead of jumping from PS6 to PS3.

12. SHIFT DOWN IN PS7

In PS7 of Divide, it is necessary to shift down R1, R2, R3, and R4. To do this in the Three Counter machine it is necessary, first, to shift up the sync pulse, then to shift up RS. It is also necessary to reset the D Counter to clear out the RMD data. If CRD9 is not developed, the RMD data

will appear in R4 time. This is not desirable! OR gate 308 controls the shifting up of the sync pulse in PS7 of Divide. The three signals at the input of OR gate 308 gate for Multiply or Divide, PS7, and C0 time. Therefore, SAD9 and SDC9 will be generated each R time of C0 time. This results in shifting the sync pulse from R3 C0 to R4 C0. OR gate 302 controls shifting up RS in Multiply or Divide. The three signals at the input to O-302 define Multiply or Divide, PS7, and RS or RMD. Therefore, the output of O-302 will be negative each RS time, and each RMD time in PS7 Divide which causes SAD9 and SDC9 to be generated at the end of each RS and each RMD times.

Since it is necessary to reset the D Counter, OR gate 303 is used to cause CRD9 to be generated. OR gate 303 has three inputs; EMD4 is negative in Divide, PS74 is negative in PS7, and TR14 is negative each R1 time. Therefore, the output of O-303 will be negative each R1 time of PS7 of Divide, and causes CRD9 to be generated. (For additional, more detailed information on Shift Down, see Topic E4.)

At the end of PS7, HOME1 steps the Phase Counter to zero. HOME1 also resets the Common Function FF through AC AND gate 1104. This results in all appropriate flip-flops being reset and terminates the Divide function.

13. CONCLUSION AND SUMMARY

In general, the method of division in the Three Counter machine is the same as the method of division in the Four Counter machine. The same operations must be done, and they must be done in the same order. The only really significant change is that in the Three Counter machine nothing is done in PS3; instead the first subtract is done in PS4. All subsequent subtractions are done in PS5 and each subtraction done in PS5 results in a count of one being added to R2. Note the similarity to the operation of the Four Counter machine. The first subtraction (in PS4) never results in a count of one being added to R2 to develop the answer. But each subsequent subtraction (in PS5) always results in a count of one being added to R2. All other operations are the same and are done in the same Phase Counter steps. Of course the logic used to generate each of these operations is somewhat different in the two machines, but on the whole the logic used in the Three Counter machine is simpler than that used in the Four Counter machine. This should result in easier, more efficient trouble shooting.

L. DECIMAL POINT COUNTER

A block diagram of the Decimal Point Counter

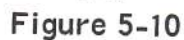
used in the Four Counter machine is shown in Figure 5-10. Its counterpart used in the Three Counter machine is shown in Figure 5-11. A brief comparison of these two block diagrams will reveal the strong similarity of the two. In Figure 5-10 the number one flip-flop can be set by AC AND gate 1212 or by AC AND gate 1211. A-1212 is gated by switch wafer M. A-1211 is gated by switch wafer H. However, in Figure 5-11 the number one flip-flop is set by AC AND gate 1211 only. Switch wafers M and H are inputs to OR gate 300 and the output of OR gate provides the DC input to A-1211. In the same fashion switch wafers L and G are inputs to OR gate 319 whose output is used to provide the DC input to A-1102 to set the number two flip-flop; switch wafers K and F are inputs to OR gate 320 and switch wafers J and E are inputs to OR gate 321 to provide the DC input to A-1181 to set the number eight flip-flop. In reality this does not change the logic of setting the Decimal Point Counter at all. It does enable the more efficient use of parts on hand to accomplish the same job. Note that there are no other changes in the Decimal Point Counter block diagrams.

M. DISPLAY

The method used to generate the complex deflection waveforms remains unchanged. However, some of the circuits used to generate the components of these complex waveforms are somewhat changed. These changes are described, circuit by circuit, as follows:

1. SEGMENT GENERATOR

The segment generator is no longer gated by the signals TCA2, TCB2, and TCC2. To take the place of these three signals, YBL5 is used. Because YBL5 is positive when it is desired to reset the segment generator, inverter 3001 is no longer needed. The new segment generator circuit is shown in Figure 5-12 with two inputs: YBL5 and YBDP3. When either of these two signals is logic one, inverter 3002 is off and has a negative (logic zero) output. This negative output keeps the segment generator reset transistor turned on to prevent the sawtooth waveform from being generated. YBDP3 is normally negative and enables YBL5 to control the segment generator. YBL5 is negative when it is desired to display a segment; hence, with both inputs to OR gate 3000 negative, inverter 3002 is turned on. With inverter 3002 turned on, the segment generator reset transistor is turned off, thus allowing a sawtooth to be developed. (An interesting result of using YBL5 is that no sawtooth waveform is generated unless that segment is actually intensified.)



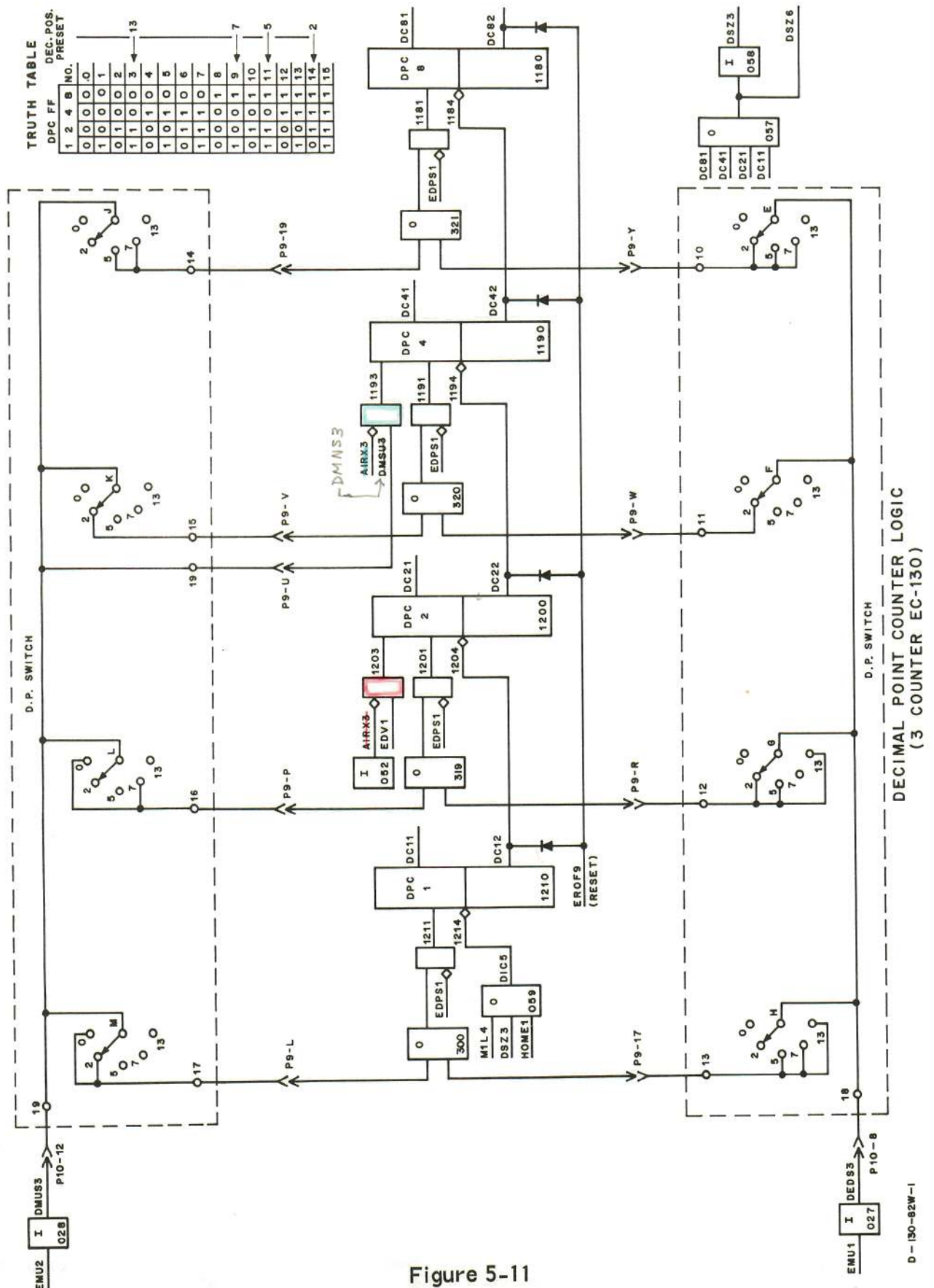


Figure 5-11

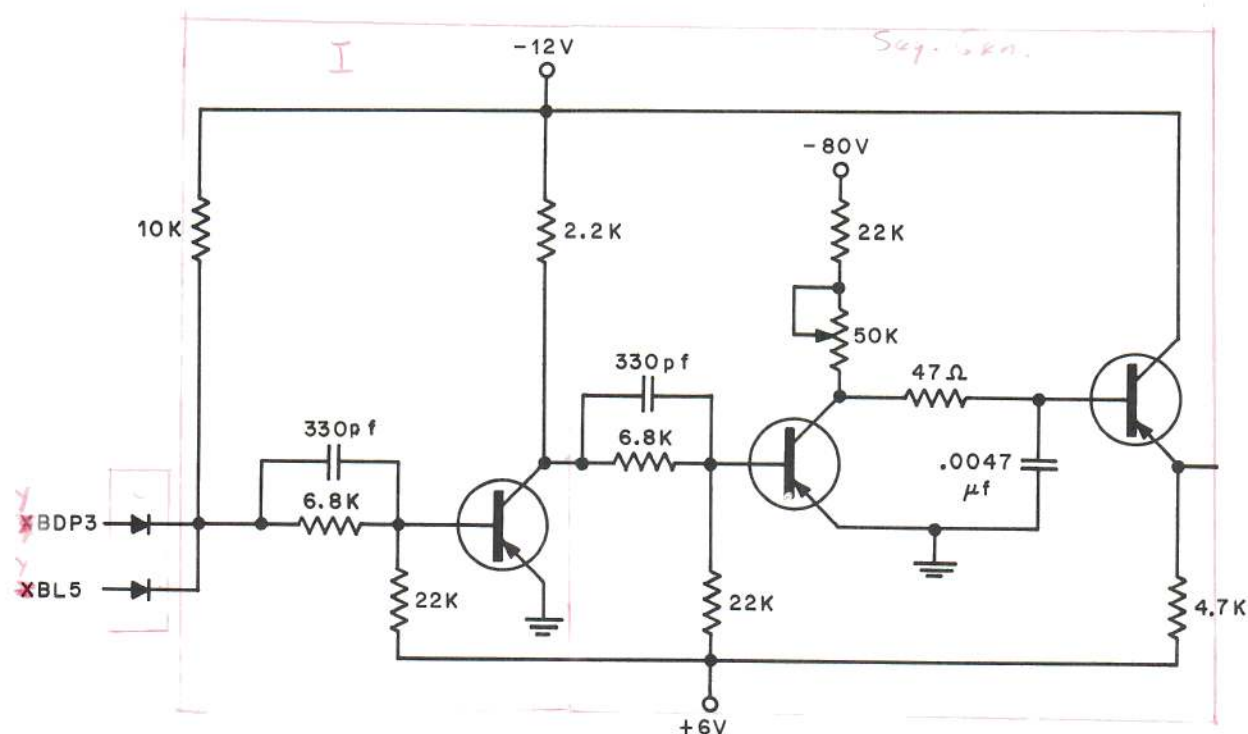


Figure 5-12

In addition to the logic change as described, there are two circuit changes. In the segment generator of the Four Counter machine there is a 47 ohm resistor connected between the .0047 μ f capacitor and ground. In the new EC-130 this 47 ohm resistor is connected between the .0047 μ f capacitor and the collector of the segment generator reset transistor. It serves the same purpose as before; that is, it limits collector current when the reset transistor is turned on. This protects the transistor from thermal damage. The second circuit change is that there is no longer a clamp diode connected from the .0047 μ f capacitor to -12 volts. Recall that it is necessary to clamp the capacitor to some maximum negative value. If this were not done, and the reset transistor failed for some reason to turn on, the capacitor would charge to -80 volts, exceeding the maximum collector voltage and base voltage rating of all the associated transistors. It is now realized, however, that the capacitor is clamped to a maximum of -12 volts even without the clamp diode. If the voltage on the capacitor exceeds -12.1 volts, the collector-base junction of the emitter follower is forward biased and clamps the capacitor to a maximum of about -12.1 volts.

2. SEGMENT SWITCHES

The Segment Switches have also been changed (see Figure 5-13). This circuit is simpler than the earlier version. The sawtooth waveform is applied

to a voltage divider comprised of two 4.64K 1% resistors in series. The other end of the voltage divider is connected to the appropriate Dot Generator. The collector of a transistor is connected between the two 4.64K resistors. When the transistor is turned off, current from the Segment Generator develops a sawtooth voltage waveform across the 500 ohm potentiometer (character width or height adjustment). But when the transistor is turned on, all this current is shorted to ground through the transistor, and no sawtooth voltage is developed across the 500 ohm potentiometer. Note that the base bias circuitry is the same as in the earlier EC-130, and that both the Vertical and Horizontal Segment switches are identical.

3. HORIZONTAL STAIRCASE GENERATOR

The Horizontal Staircase Generator is changed only slightly. (See Figure 5-14.) In the Four Counter machine, YYC1 and YCPR3 are inputs to OR gate 3006 to reset the staircase generator. But, in the new machine, YCPR3 is not generated, so TFG2 is used instead. The result is the same as before. YYC1 will go negative in C15 time, and TFG2 will go negative at the end of R4 C15 time. When both signals are negative, inverter 3007 is turned on to reset the generator.

Second, the clamp diode has been removed from the .47 μ f capacitor to -12 volts for the same

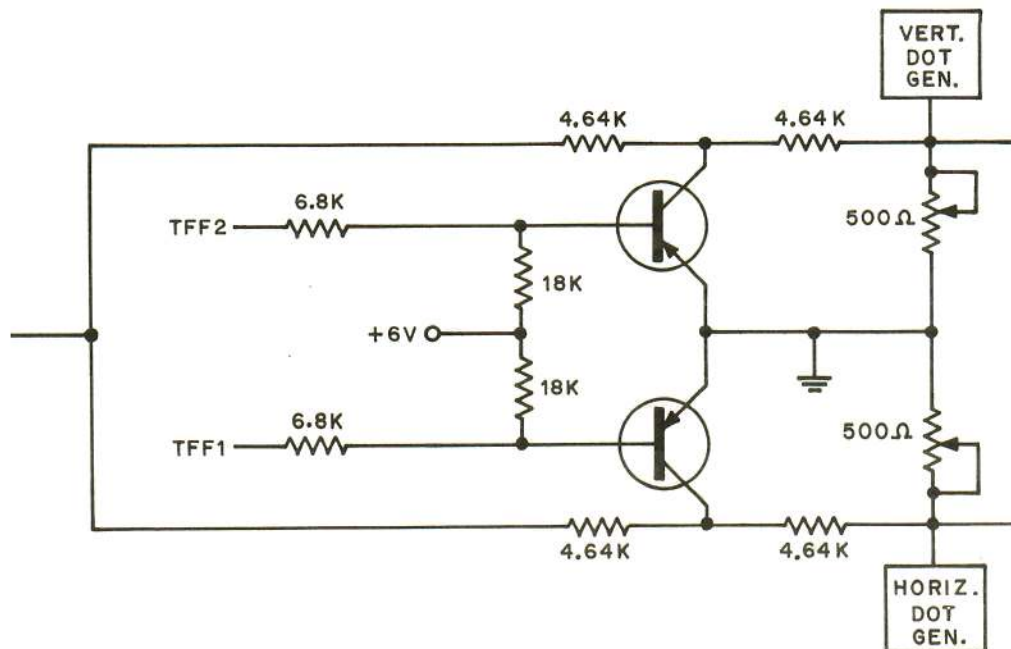


Figure 5-13

reason as listed in the Segment Generator description. The capacitor is clamped through the collector base junction of the first emitter follower. The Horizontal Staircase Generator circuit is shown in Figure 5-14.

The third change was made to reduce the possibility of a wavering display. The load resistor of OR gate 3004 is reduced to 12K and is returned to -8V. This necessitates a change in the size of the capacitor in the base of the step control transistor. It is now .0022 μ f.

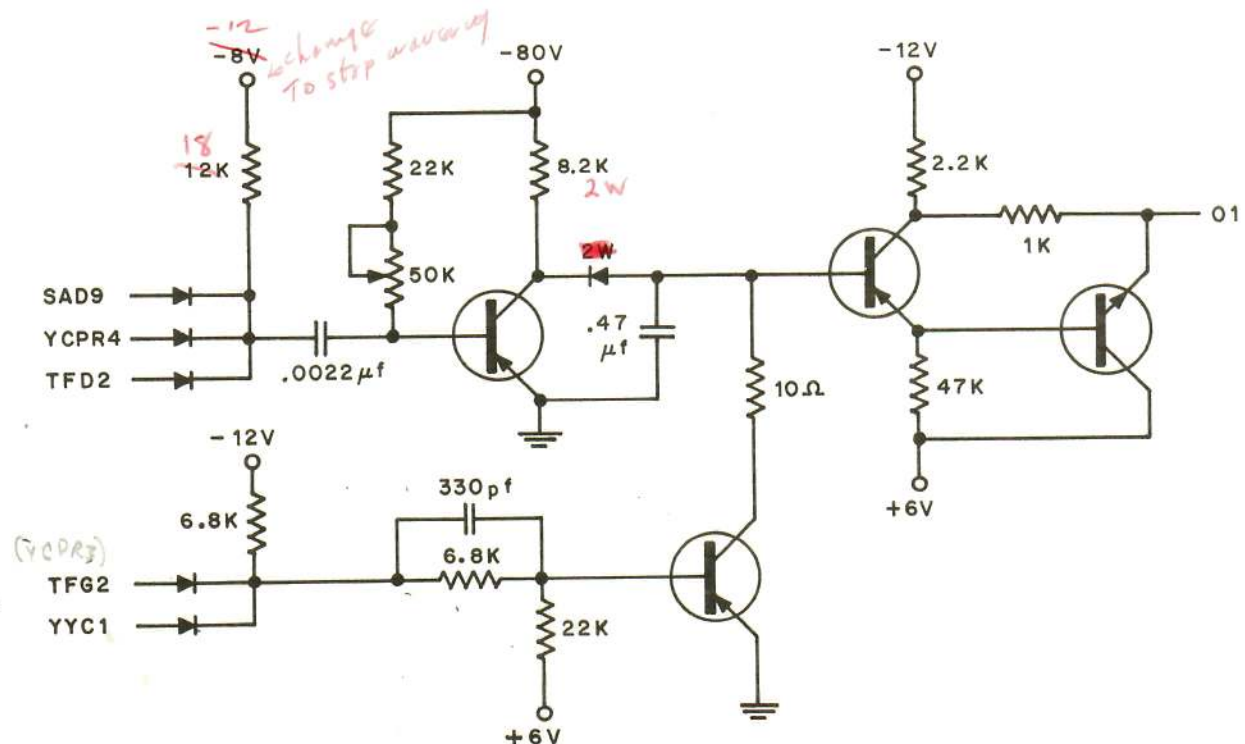


Figure 5-14

4. COMPARE AND INTENSIFICATION

The Compare logic involves only three small changes. First, PSZ3 is no longer an input to AND gate 225, so YCPR4 is developed even in a function or digit entry.

Second, YCPR3 is no longer developed. Hence, inverter 227 doesn't exist. Third, to generate SAD9 for display, OR gate 031 is used. O-031 has four inputs. PC41, PC21, and PC11 define PSZ so that the only time the output of O-031 can go negative is when there is a compare in PSZ. When the output does go negative SAD9 is caused to be developed.

In the blanking circuitry, PSZ3 is no longer an input to AND gate 250 because PSZ3 is no longer developed. Instead, ECFD4 is used to inhibit unblanking during a function or digit entry. OR gate 199 is used to inhibit unblanking during the last three microseconds of a segment. By applying the output of O-199 as an input to A-250, inverter 200 is no longer needed or used.

TC153 can no longer be used to enable the Display Control FF to be reset, because TC153 no longer exists, so TCX5 is used, and there is no change in timing.

MULTIPLY FLOW CHART (3 COUNTER EC-130)

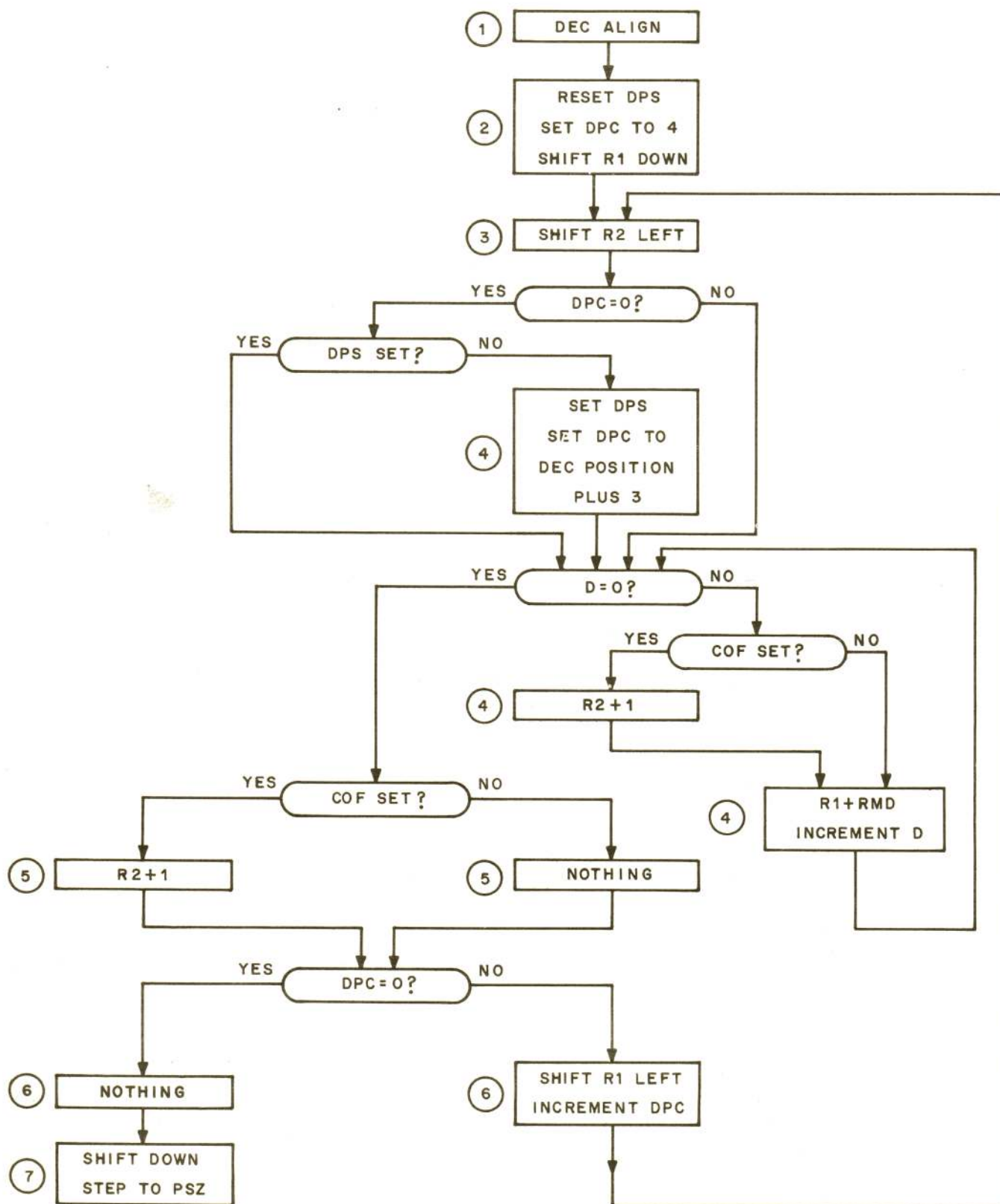


Figure 5-8

DIVIDE FLOW CHART (3 COUNTER EC-130)

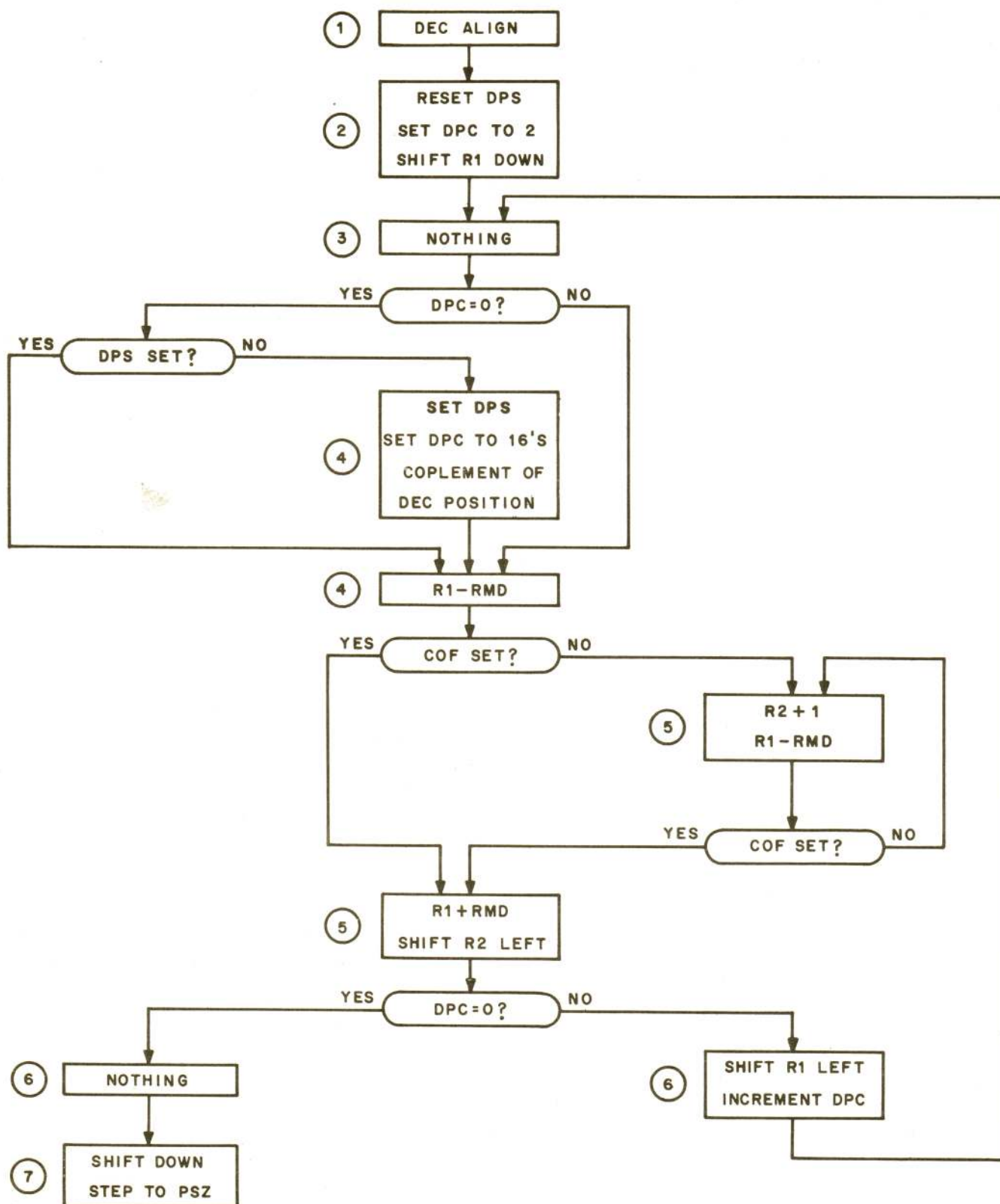


Figure 5-9