

**Casio 121-B
Calculator**

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Notes

- ◆ The symbol  denotes a physical connector pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- ◆ The symbol  denotes a connection between the two main printed circuit boards.
- ◆ The symbol  denotes V-24.
- ◆ Capacitance in microfarads unless otherwise indicated.
- ◆ These drawings based on unit with Serial No. ?.
- ◆ See www.cs.ubc.ca/~hilpert/eec for additional information.

Log

- ◆ 2006 Dec: Data collection by Mick Metselaar.
- ◆ 2007 Jan: Formatting and organisation by bhilpert.

Unresolved Issues & Questions

A few issues from the reverse engineering present questions. These are listed here:

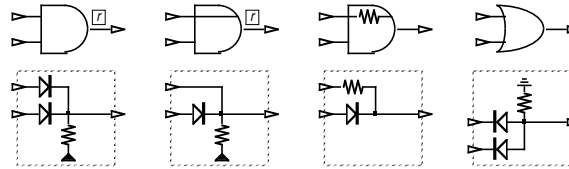
- No load resistor shown for flip-flop output 2-2V2-4 (Control - part 2).
- No load resistor shown for inverter output 2-2V3-9 (Control - part 2).
- No load resistor shown for OR output 2-1D1-7 (Arithmetic).
- No load resistor shown for OR output 2-U1-11 (Arithmetic).
- No load resistor shown for OR output 1-1D2-9 (Arithmetic).
- Two load resistors are shown for OR output 1-U1-3 (Control - part 1).
- Flip-flop output 2-2V2-5 is controlled by a wired-AND connection (Control - part 2).
- Flip-flop output 2-2V3-12 is controlled by a wired-AND connection (Control - part 2).

Logic Implementation

Most AND gates are constructed from discrete diodes and resistors. Most OR gates and more complex logic elements are contained in integrated circuits.

Gate symbols and signal names are presented in accordance with negative logic:
logic 0 = 0V, GND
logic 1 = V-24

The internal construction of discrete gates is shown in the following diagrams. A wire-AND or wire-OR construction is indicated by the input line traversing the width of the gate. In a few instances the load resistor for the gate is itself used as an input.



Outputs from ICs also generally require an external load resistor connected from the output to V-24. To reduce clutter load resistors are indicated in the schematic by a symbol in a box above the output:

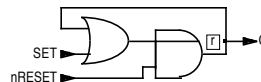
- | | |
|---|--|
|  = 100K discrete |  = discrete resistor, value undetermined |
|  = 220K discrete |  = modular package resistor |
|  = 56K discrete |  = no load resistor |
| |  = seemingly missing from source drawings |

In a few circumstances the discrete load resistor may be absent:

- When a gate drives only diode inputs (which are later followed by a load resistor), as opposed to driving the gate of a MOS transistor.
- The SSR0109 shift register, which appears to have internal resistors on the outputs.

S-R Flip-Flops

In several instances, S-R type flip-flops are constructed from simple gates, the following structure being the basic form:

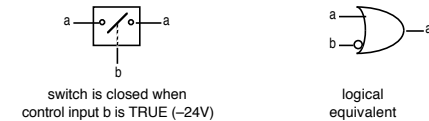


The OR gate will be within an IC and provides gain for the circuit. The AND gate is simply one diode for each nRESET input.

Notes on the Integrated Circuits

The integrated circuits are from an early family of MOS SSI / MSI technology produced by several Japanese manufacturers during the late 1960's to early 1970's. (Note these ICs are not CMOS and should not be confused with standard CMOS series ICs.)

- Outputs are open-collector, except SSR0109.
- Inferred for HD3103:
The 5 elements are not standard logic elements. They appear to be MOS transistors. They function as a bidirectional switch, or as a 2-input OR gate with one input inverted.



Care is taken in the logic design to ensure another "wire-ANDed" output does not feed back through the element to affect the state of the signal driving the non-inverted input. One location where this situation is somewhat ambiguous is the use of 2-1B5 between signals CXDA and CXEE on page Control 2.

- Inferred for flip-flops:
The flip-flops in this logic family appear to be Master/Slave D-type flip-flops with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while all outputs are changed synchronously by a single clock signal.
ØC = Capture Input (master section clock)
ØT = Toggle Input (slave section clock)
The state of the D input is captured when ØC is TRUE (-24V).
The Q output is set in accordance with the captured state when ØT goes TRUE.
- Inferred for HD3112:
This device is a full-blown Serial BCD Adder, performing serial addition, bit carry, tens carry, correction for digit sums greater than 9, negation, etc.

Gate Identification

Gates and logic elements are identified by a name taking the following form:

<board> - <type ID><enumeration>

where

- | | |
|---------------|---|
| <board> | = 1 (upper PCB) |
| | 2 (lower PCB) |
| <type ID> | = A (discrete AND gate) |
| | O (discrete OR gate) |
| | N (discrete NOT gate) |
| | other (within an IC, see 'IC Pinouts' page) |
| <enumeration> | = 1 to n |

When possible the names have been obtained from labelling on the PCB's, however if n≥50 the name has been created for this schematic.

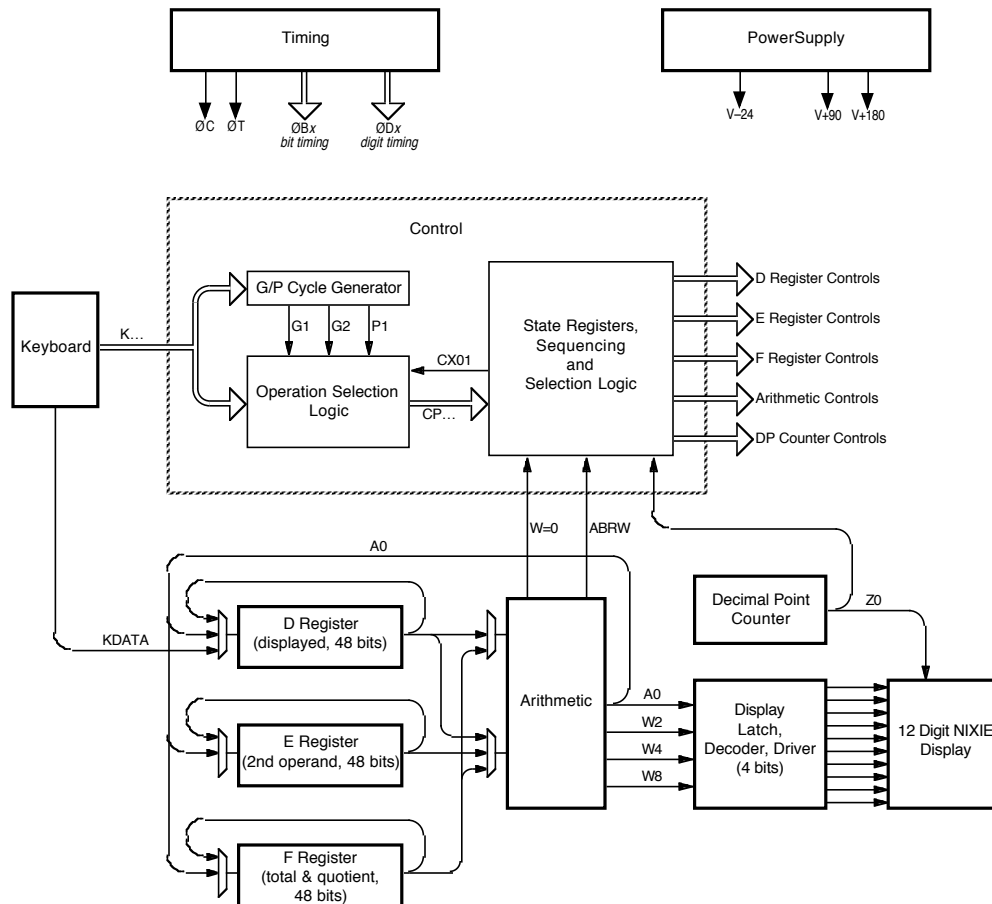
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Section: Notes

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Block Diagram



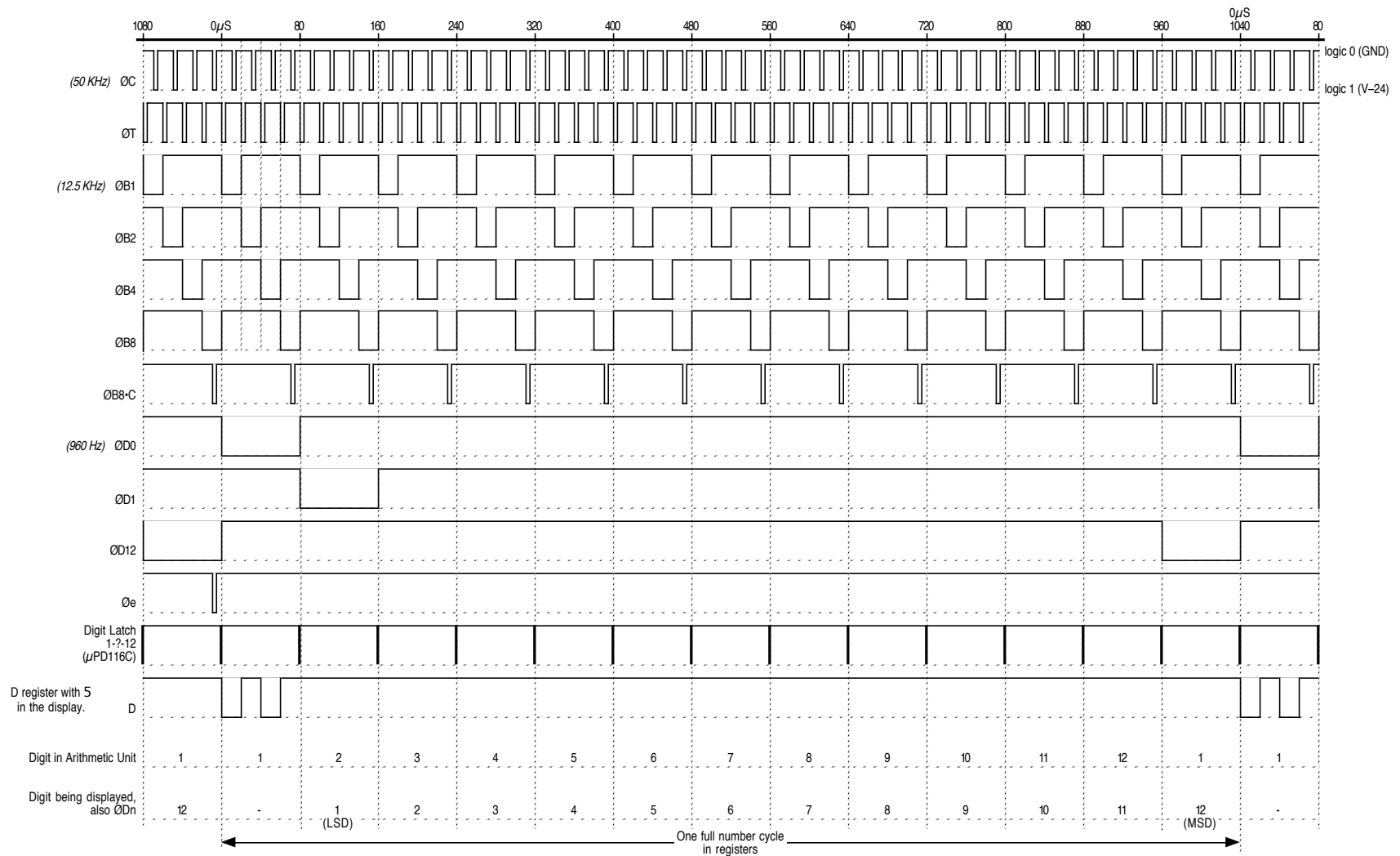
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Section: Block Diagram & Signals List
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Signals List

Some signal names are derived from labeling on the printed circuit boards. Others have been created for this schematic. A lowercase "n" at the beginning of a signal name indicates the logical NOT operation.

Section	Boards	Schematic	Description
Timing	Ø1 Ø2 J1 J4 ØK	Ø...	Uninterrupted repetitive signals.
		ØC	Master clock capture phase.
		ØT	Master clock update phase.
		ØBn	Bit periods.
	K1 K5 K12 KE	ØB1	Digit periods.
		ØB8	
		ØB8-C	
		ØDn	
	Øe	ØD0	End-of-number-cycle pulse
		ØD4	
		ØD11	
		ØD12	
Keyboard	=+ =- x ÷	K...	Signals derived directly from the keys.
		KADD	Function keys.
		KSUB	
		KMUL	
		KDIV	
		KDATA	Encoded numeral key bit stream.
Control	G1,2,3	KNML	Numeral key pressed.
		P	Counter for generating operation cycle. A single number cycle for executing most operations.
	X0	CP...	Operation selection signals.
		CPNN	Begin New Number flag.
		CPX0	Multiplication pending.
		CPD0	Division pending.
		CPEN	Enter Numeral.
		CP000	Enter 3 zeroes.
		CPAM	Negate.
		CPADD	
		CPN	
		CPMD	Recall total.
		CPF	
		CPCM	
	Qt PQ N0	CPQt	Quotient.
		CPPQ	Product or Quotient.
			Subtract from total flag.
	W0 MC	CX...	Other control signals.
		CXAS	Add during multiply, subtract during divide.
		CXSH	Shift register left during multiply and divide.
		CXIQ	Increment Quotient in F register.
		CXDD	D register receives from D register.
		CXDA	D register receives from Arithmetic.
		CXEE	E receives from E.
		CXEA	E receives from Arithmetic.
		CXFF	F receives from F.
		CXFA	F receives from Arithmetic.
D Register			12 digit register for the displayed number.
			12 digit register for the 2nd operand.
			12 digit register for total of multiplications and the quotient.
E Register			
F Register			
Arithmetic	A0 W2,4,8		Arithmetic sum.
			Digit numeral data on the way to the display latch.
			Numeral is zero.
DP Counter	Z0	W=0	Indication of Borrow during a subtraction.
		nABRW	
			Decimal point counter is at 0.

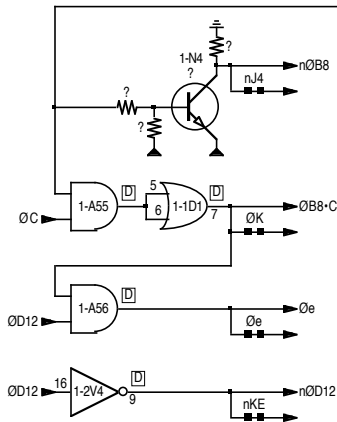
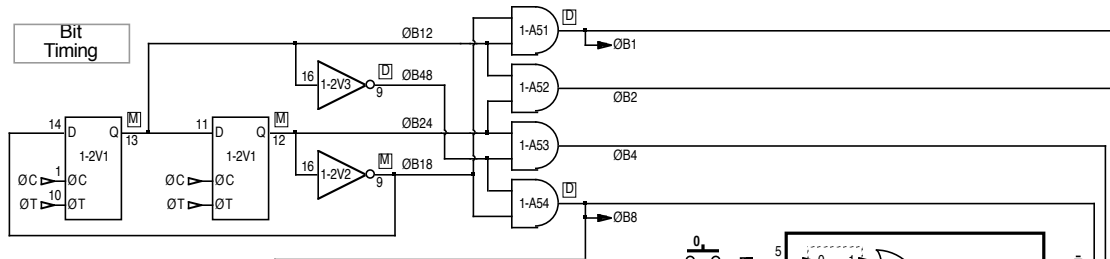
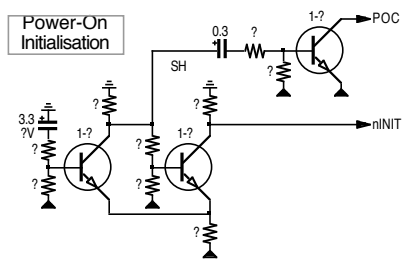
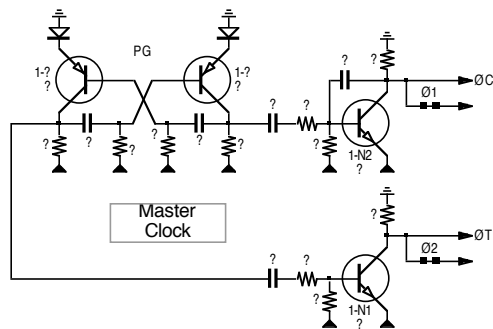


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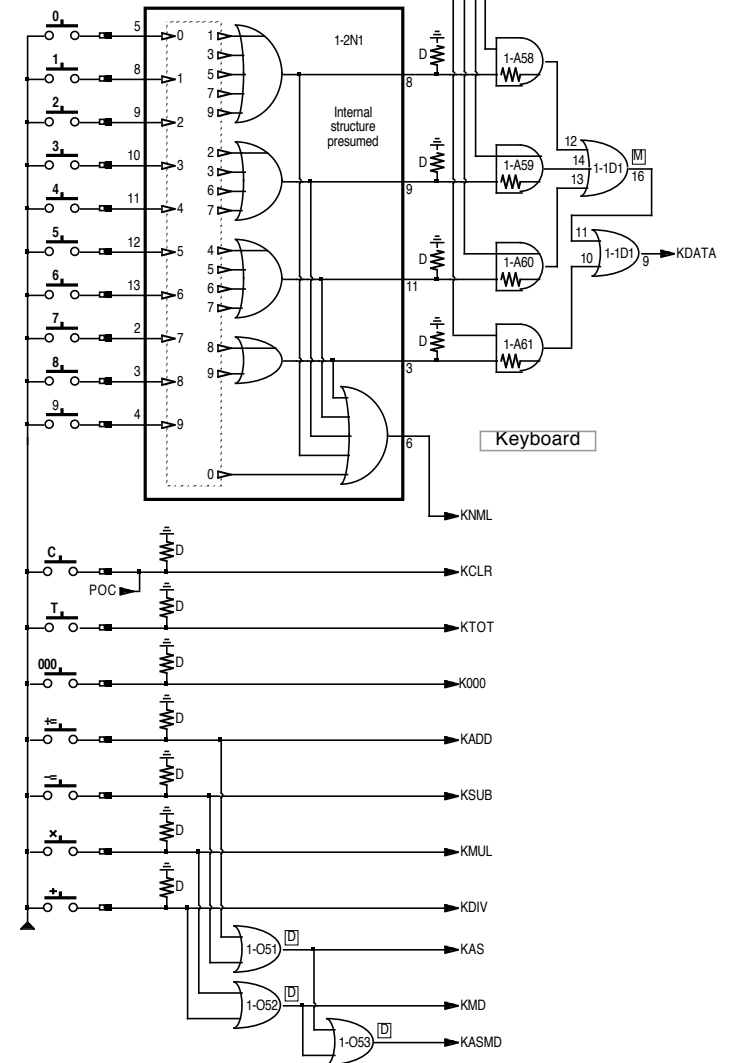
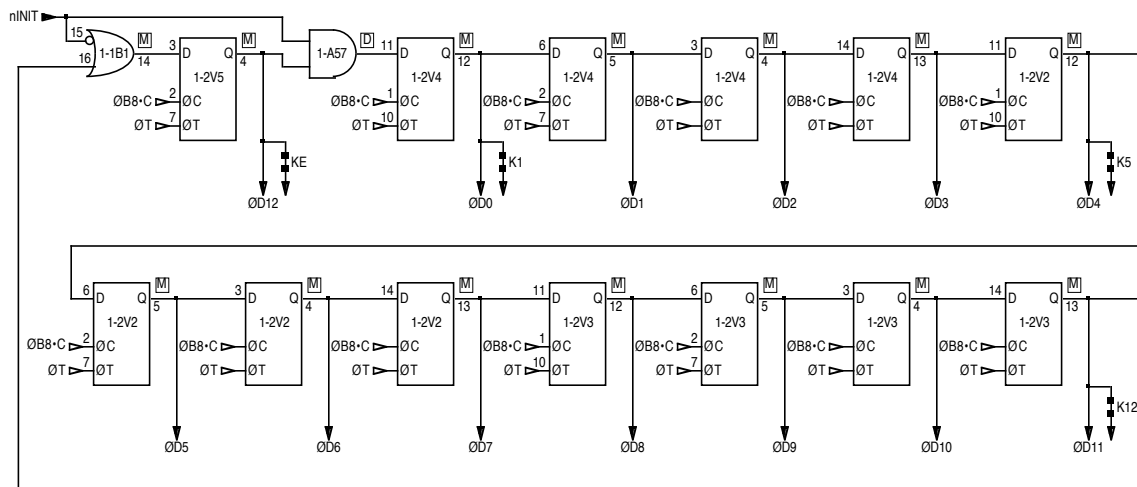
Section: Timing Diagram

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Digit Timing

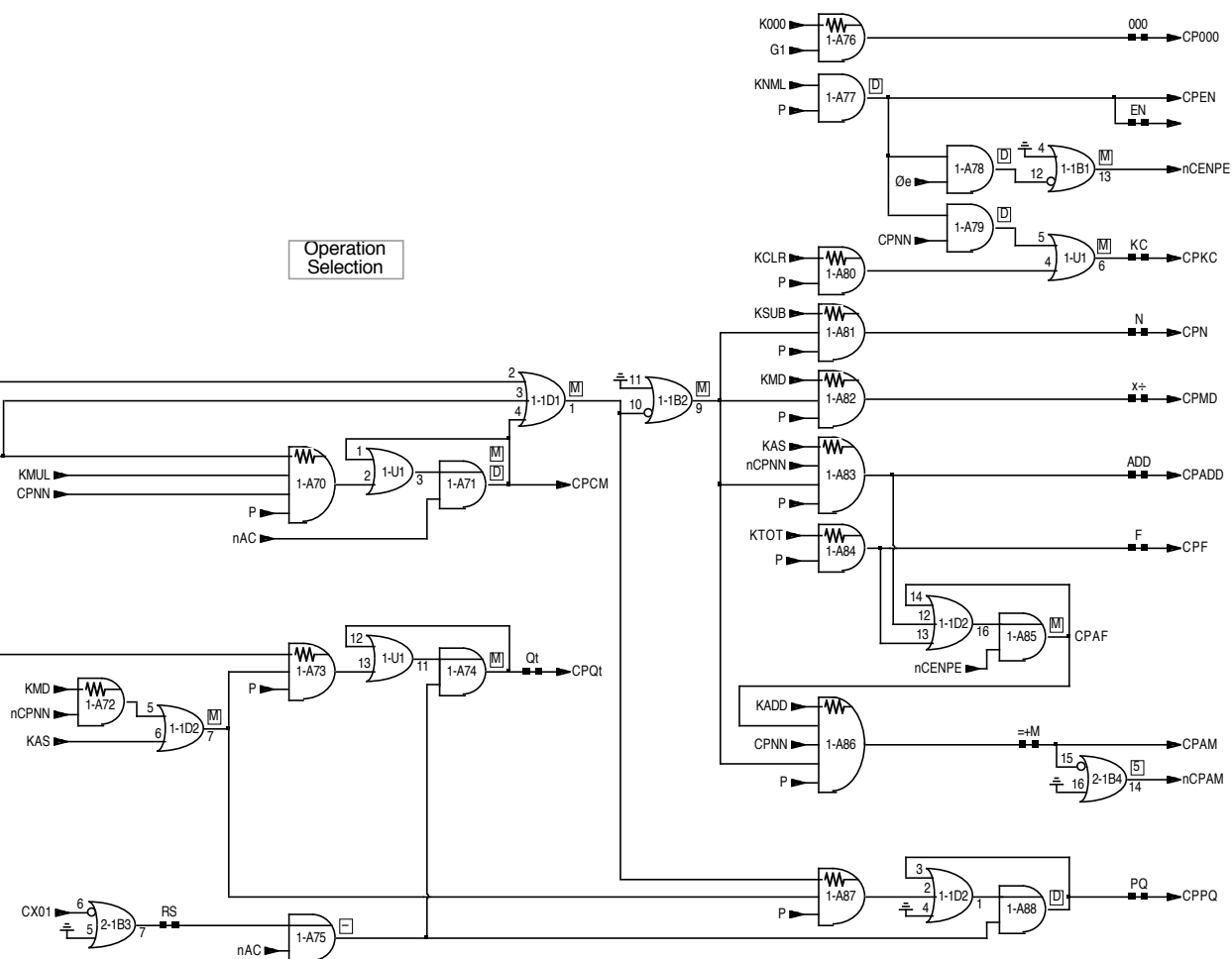
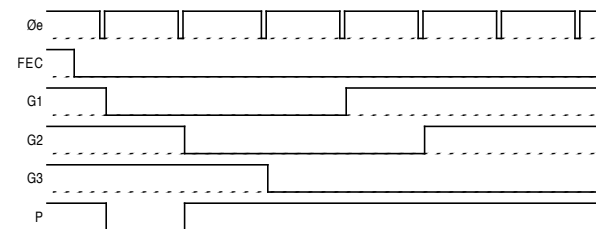


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Section: Timing & Keyboard

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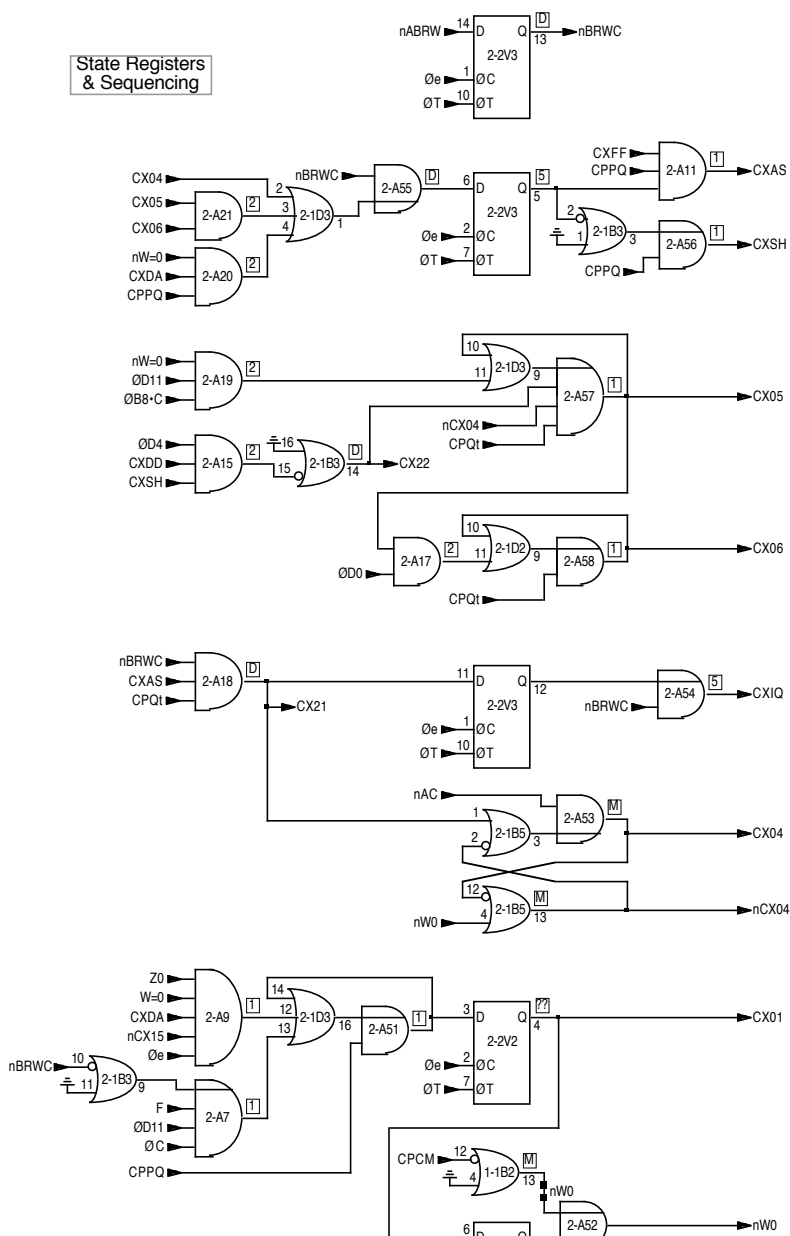
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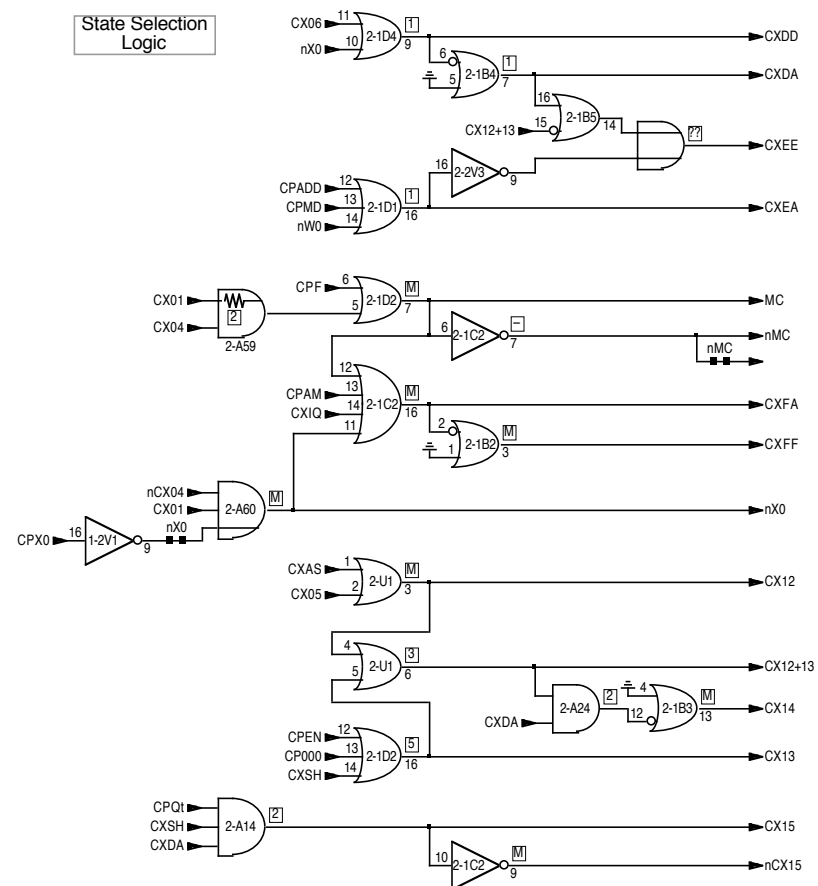
Section: Control - part 1
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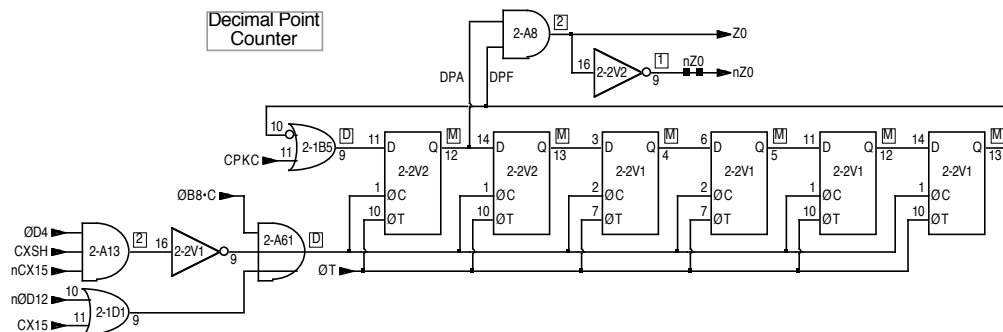
State Registers & Sequencing



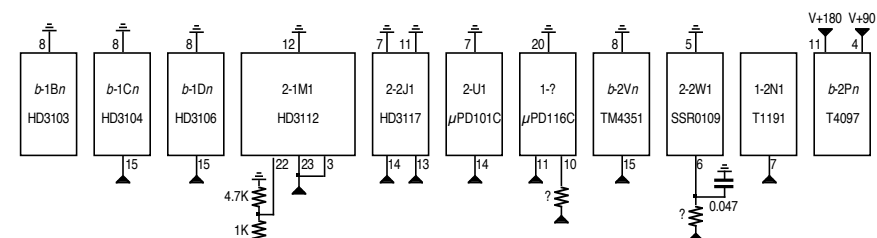
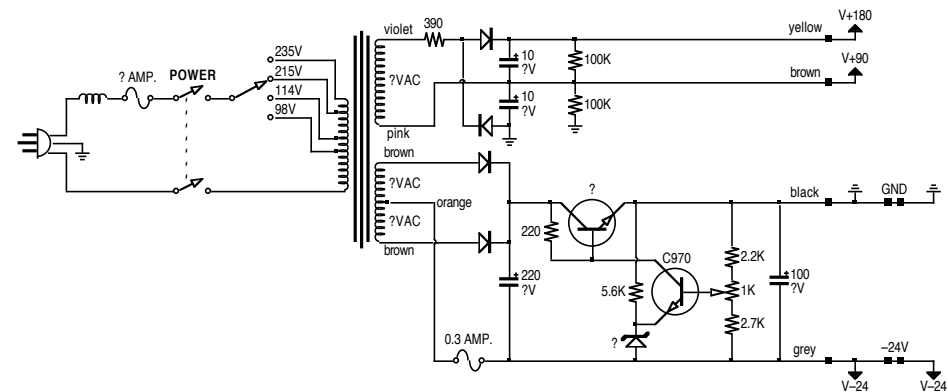
State Selection Logic



Decimal Point Counter

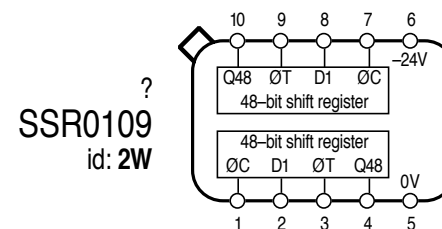
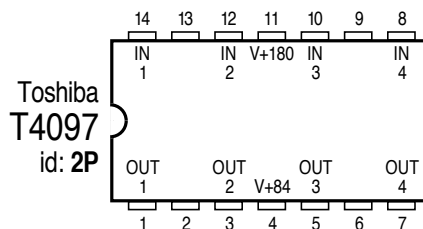
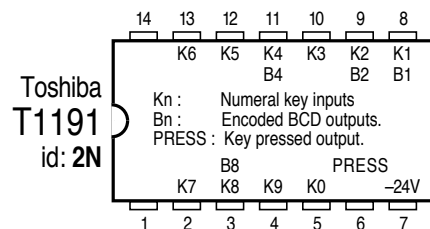
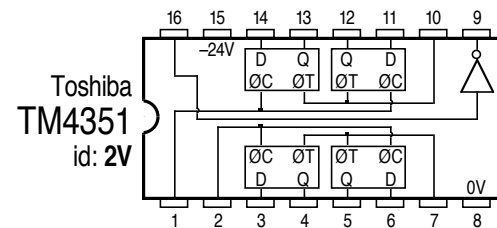
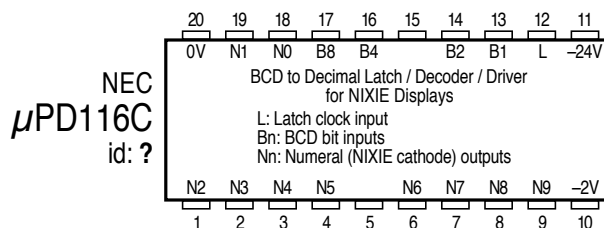
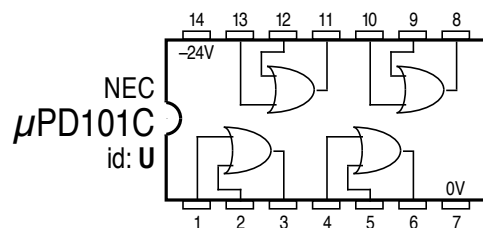
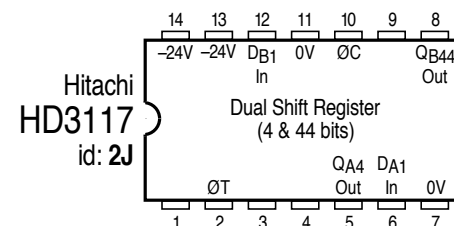
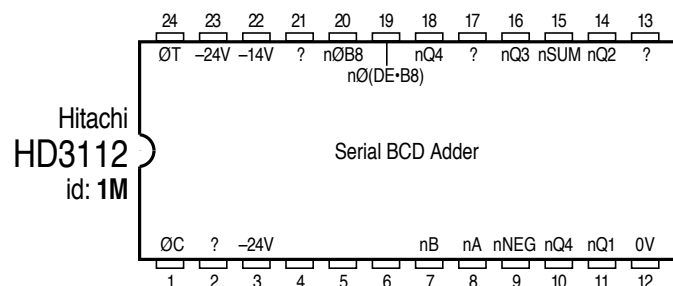
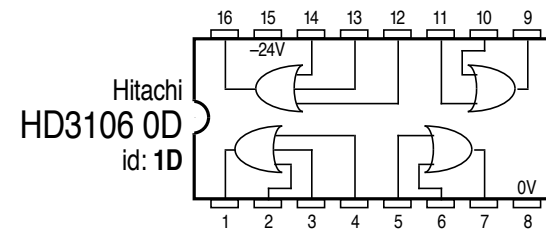
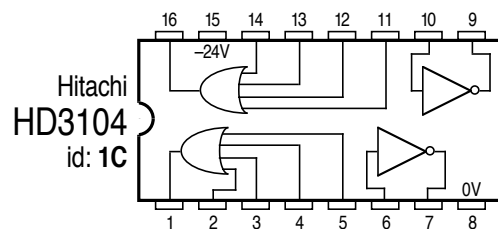
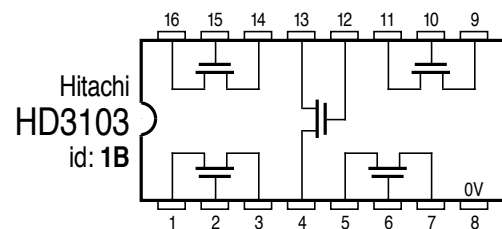


Section: Registers & Arithmetic
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IC	Type	IC	Type
1-U1	μ PD101C	2-U1	μ PD101C
1-?	μ PD116C	2-1B1	HD3103
1-1B1	HD3103	2-1B2	"
1-1B2	"	2-1B3	"
1-1D1	HD3106	2-1B4	"
1-1D2	"	2-1B5	"
1-2N1	T1191	2-1C1	HD3104
1-2P1	T4097	2-1C2	"
1-2P2	"	2-1D1	HD3106
1-2P3	"	2-1D2	"
1-2V1	TM4351	2-1D3	"
1-2V2	"	2-1D4	"
1-2V3	"	2-1M1	HD3112
1-2V4	"	2-2J1	HD3117
1-2V5	"	2-2V1	TM4351
		2-2V2	"
		2-2V3	"
		2-2W1	SSR0103

Section: Display & Power Supply
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◆ Logic 0 = 0V
Logic 1 = -24V

◆ Outputs are open-collector, closing to 0V (logic 0) and requiring external pull-down resistor to -24V (logic 1), except for SSR0109.

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Section: IC Pinouts
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