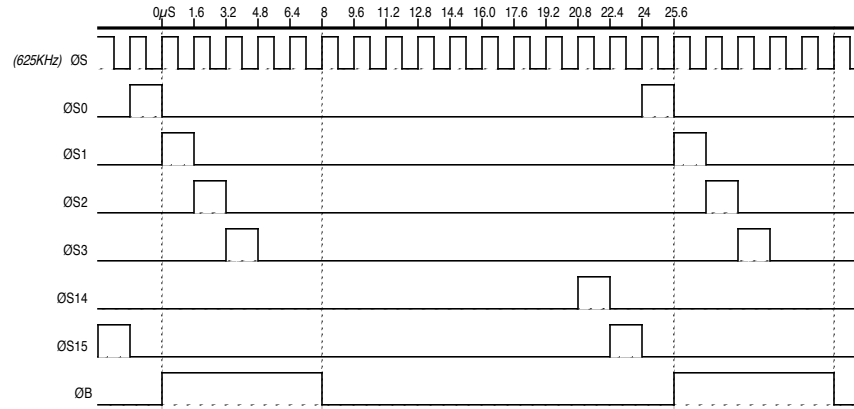
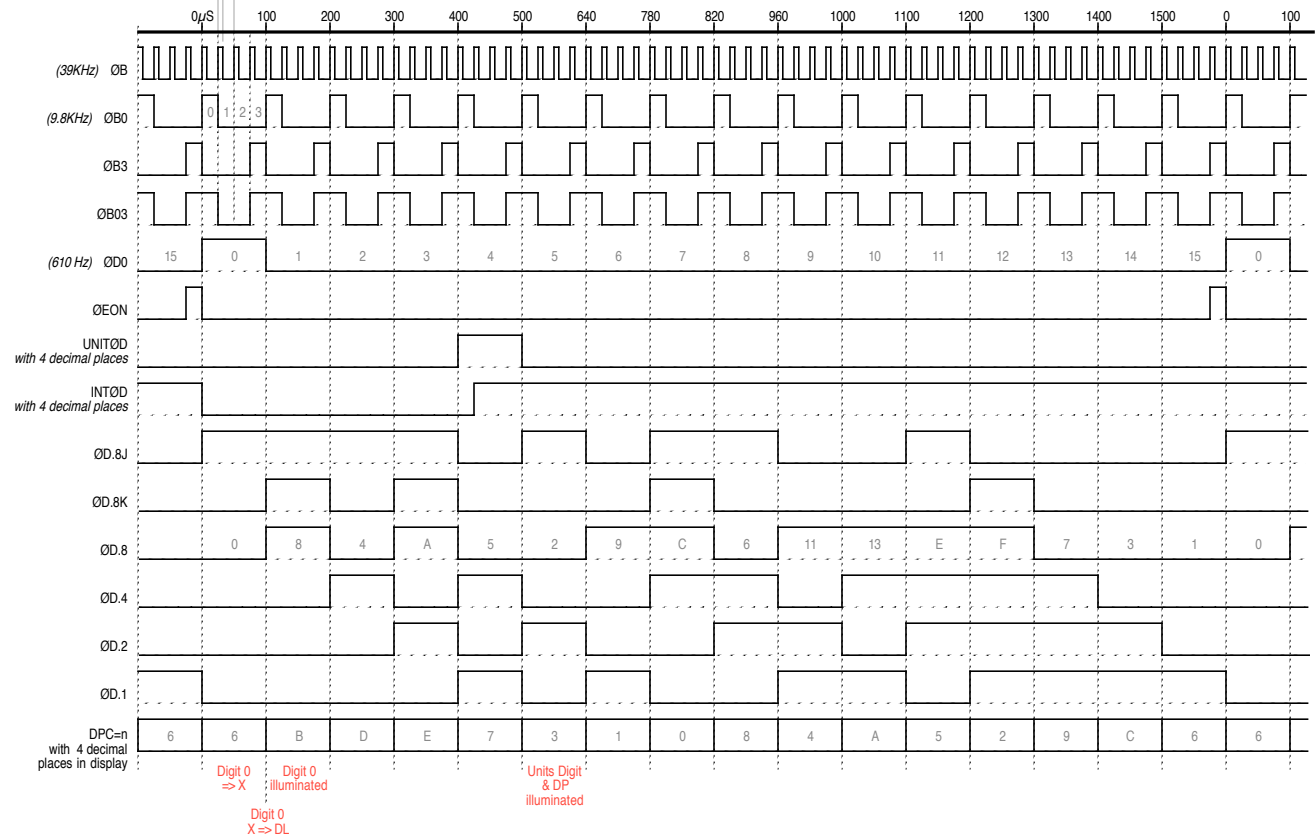


Channel Timing



Register-Bit, Digit & Number Timing



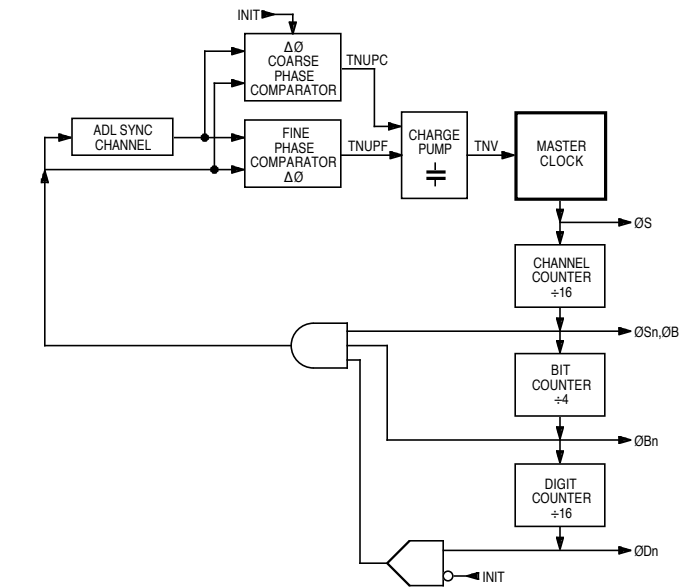
Sony SOBAX 2500 Calculator

Section: Timing Block Diagram & Graph

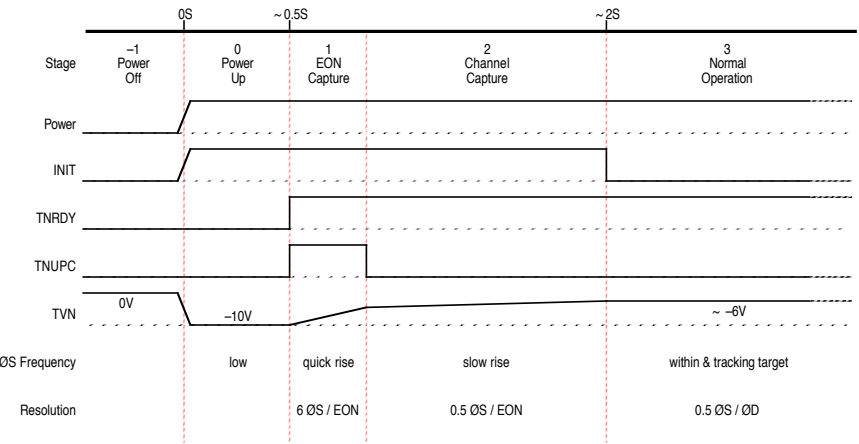
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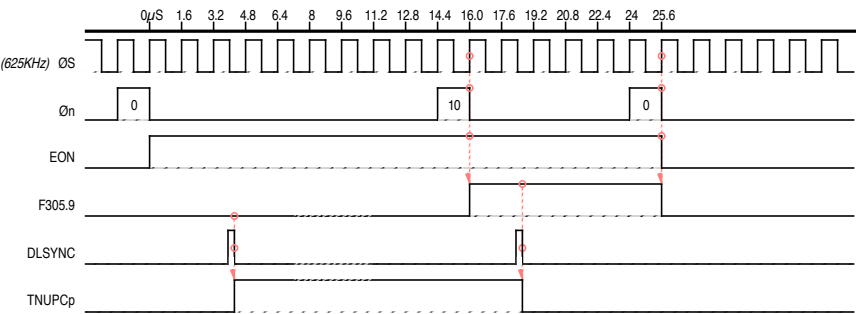
Timing Block Diagram



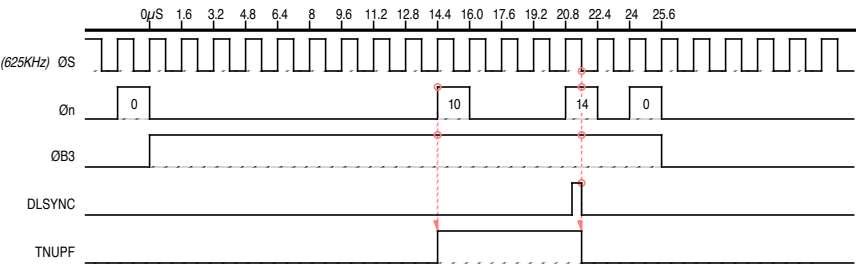
ADL Synchronisation Sequence



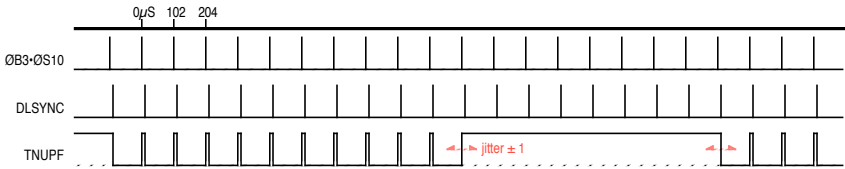
Coarse Phase Comparator Timing



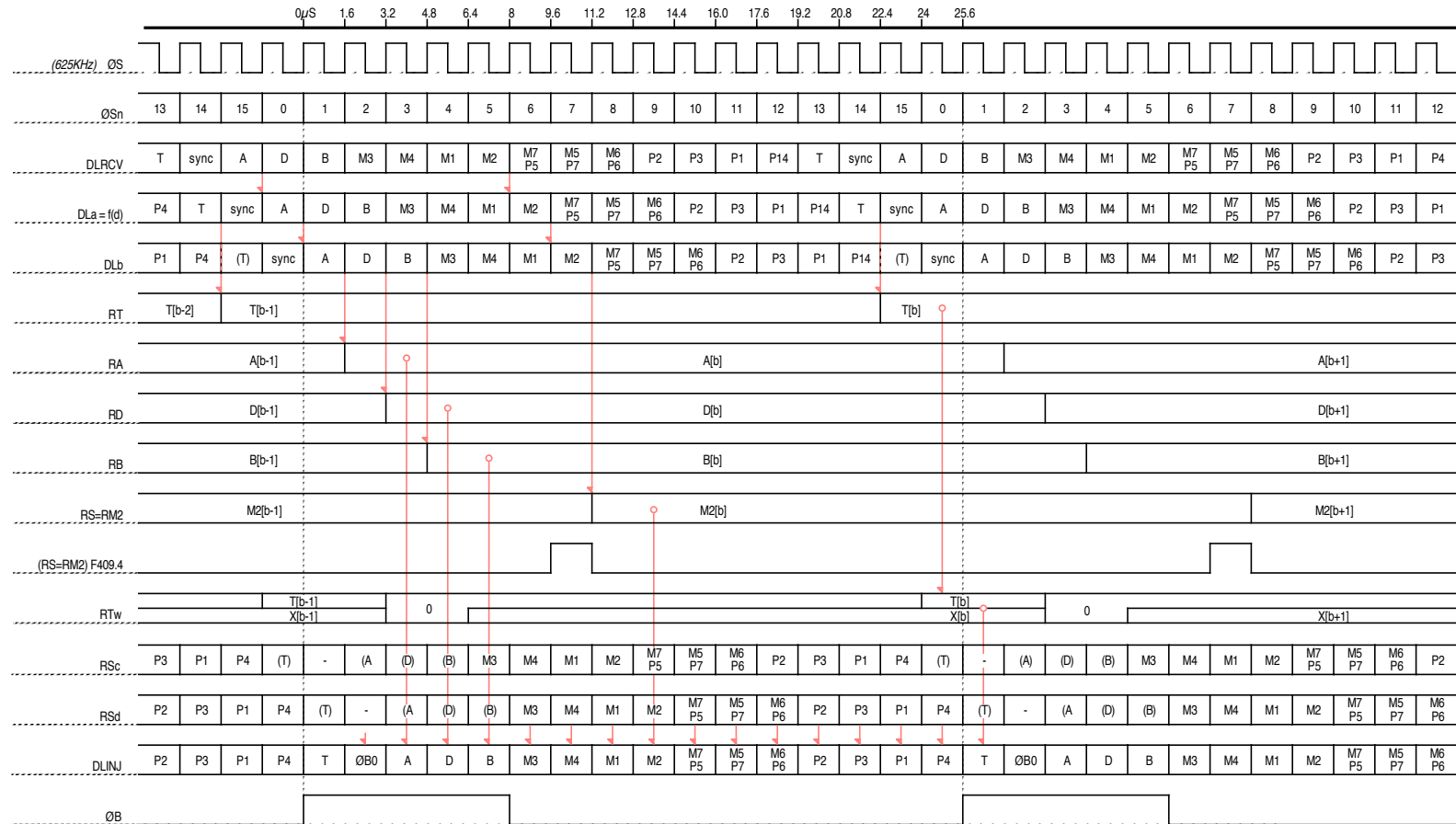
Fine Phase Comparator Timing



Observed Normal Operation of ADL Sync



Delay Line Timing



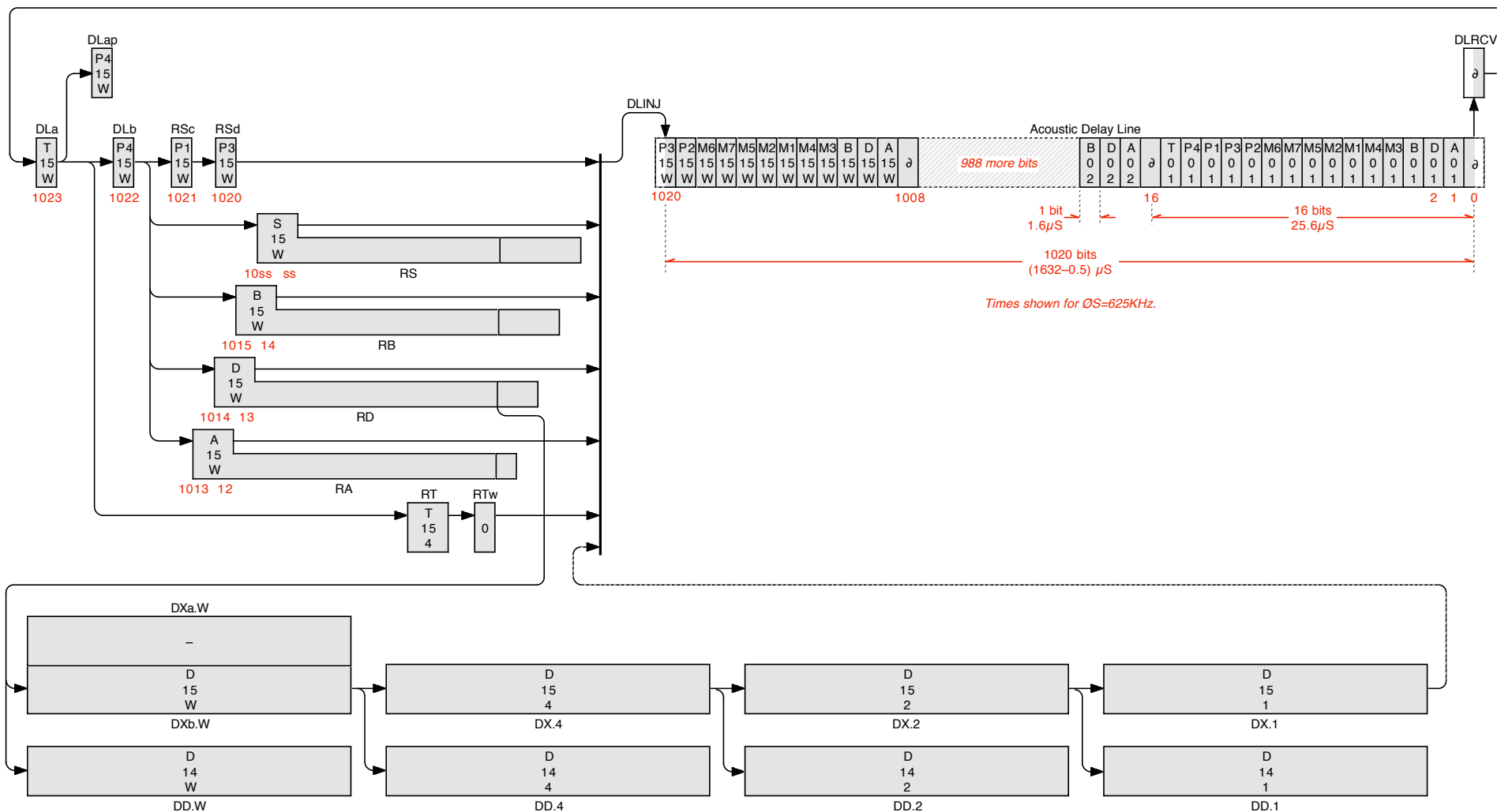
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Section: Delay Line Timing

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Delay-Line Storage State
during ØS14 of ØB3 of ØD15
and basic bit paths during idle



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Section: Delay Line Organisation

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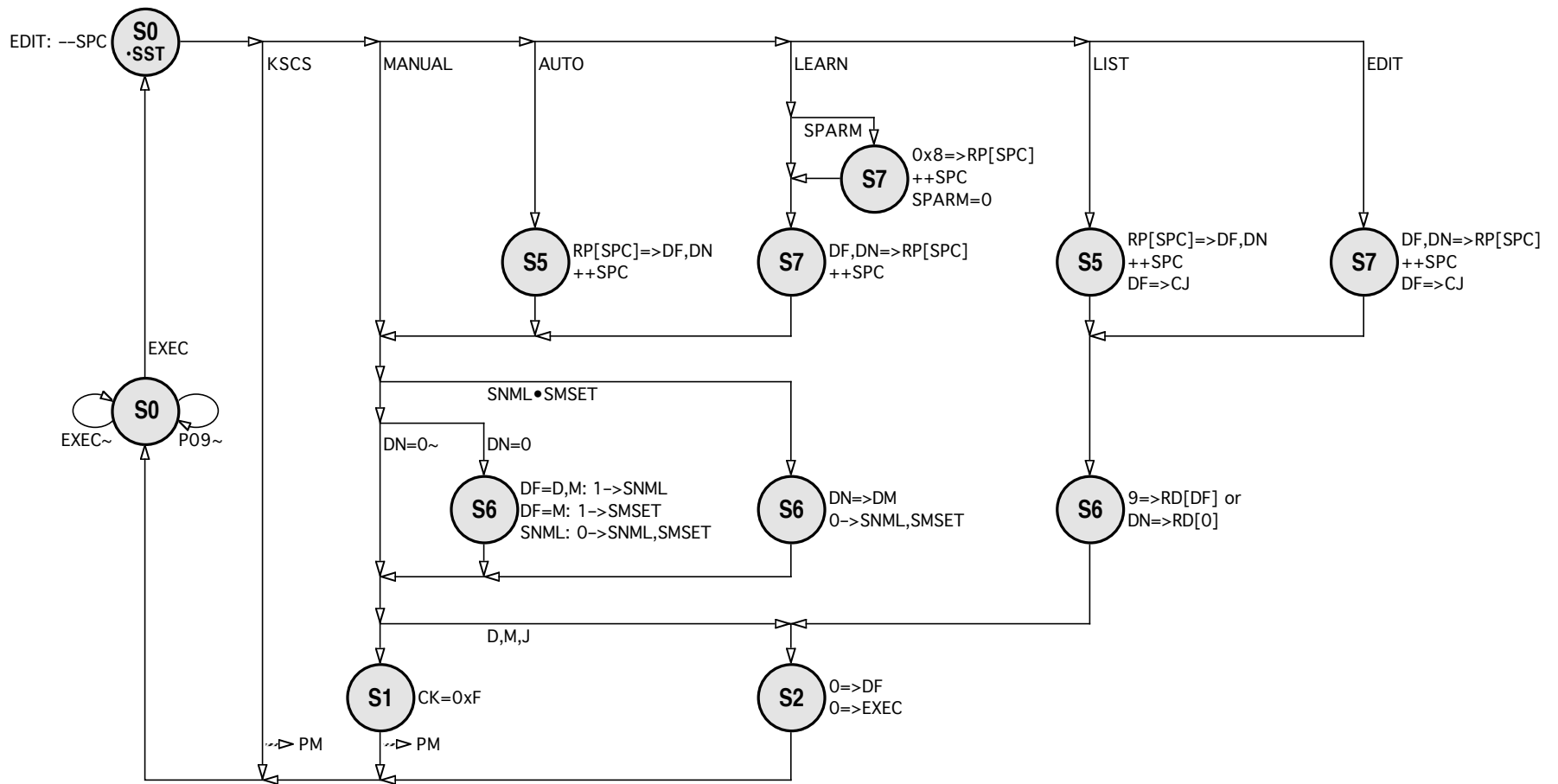
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```
<register> = A,B,C,D,M1,M2,M3,M4,M5,M6,M7,P1,P2,P3,P4
```

<register>	= R, B, C, D, M1, M2, M3
<digit>	= 0 (LSD) ... 15 (MSD)

<bit>	= 1, 2, 4, W
-------	--------------

∂ = Sync Marker

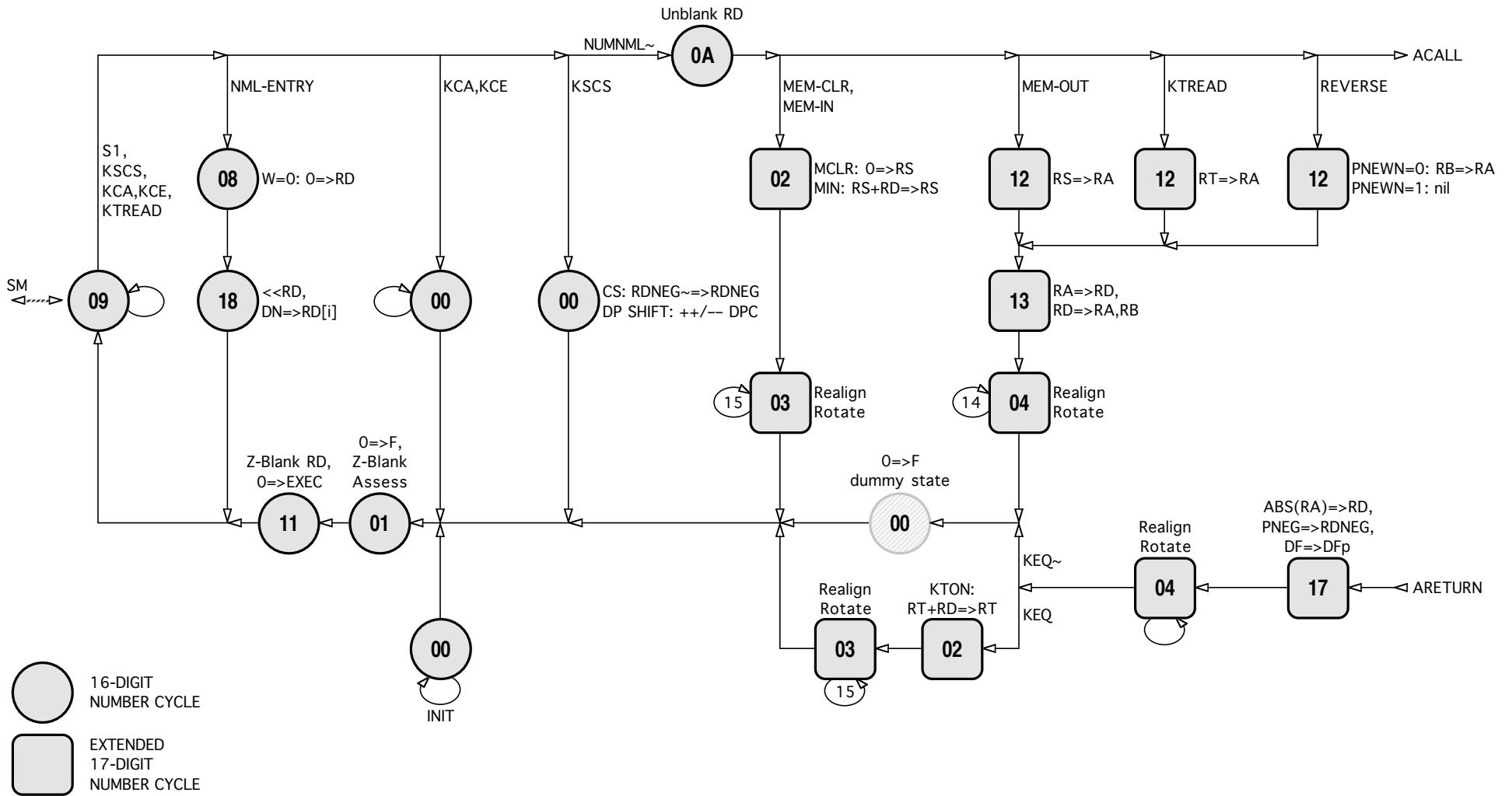


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Section: SM State Graph

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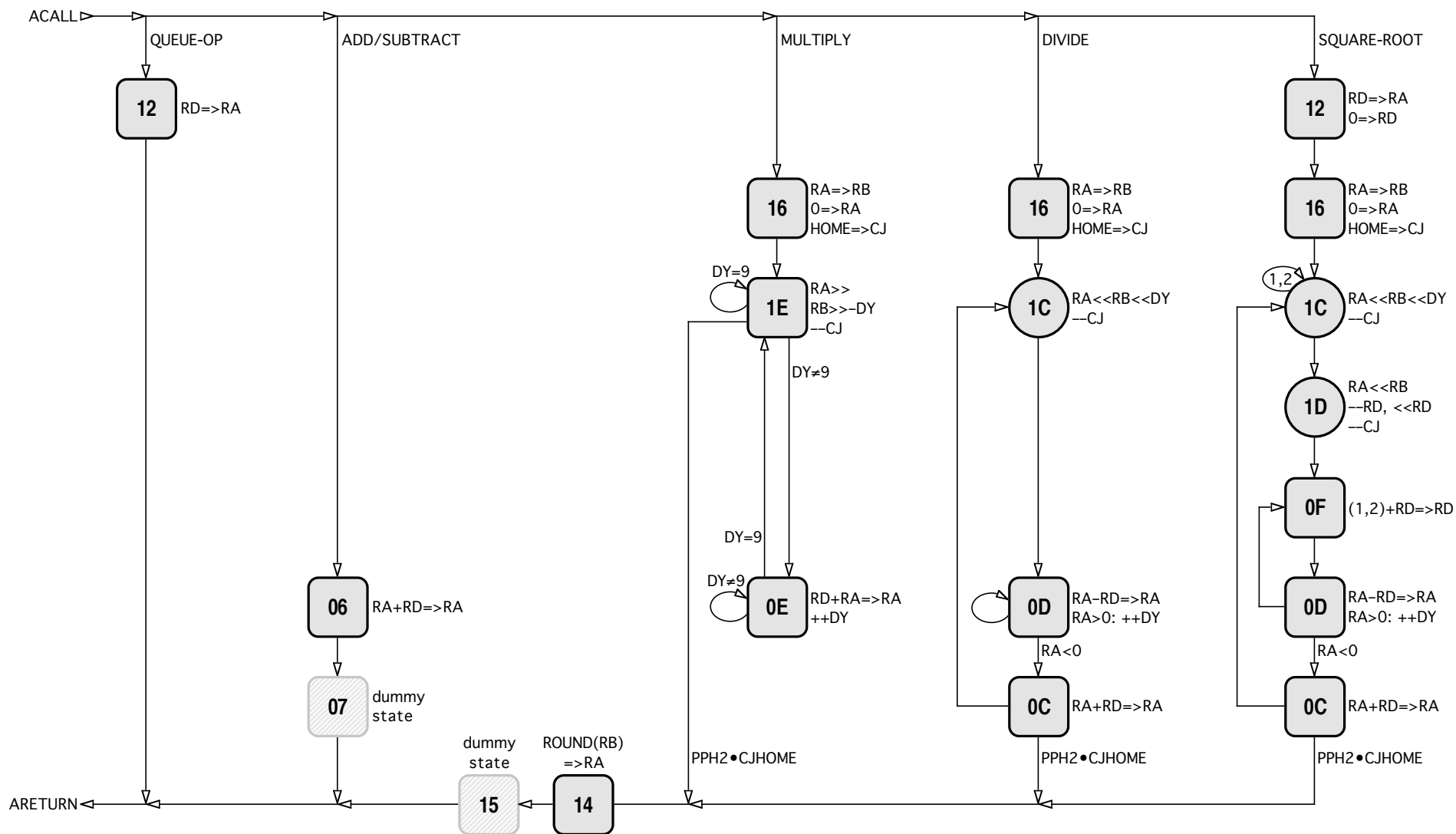


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Section: PM State Graph - Main

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Section: PM State Graph - Arithmetic

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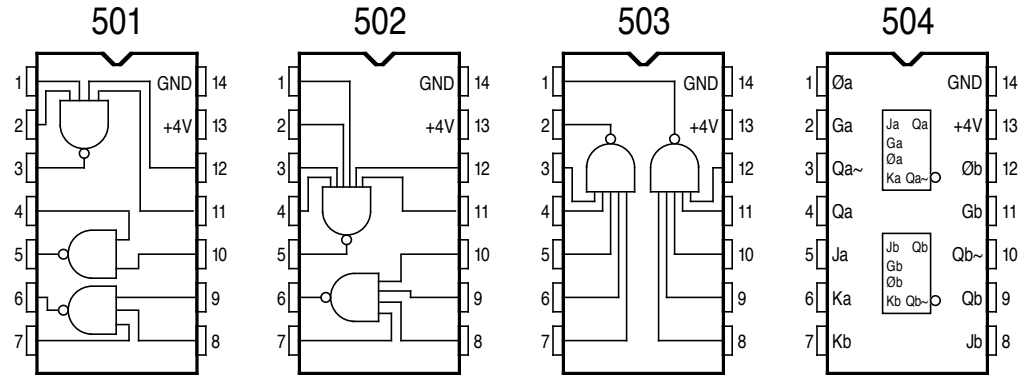
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Bit Codes

Numeral	W421	Function	8421	Function	8421
blank-0	0000	null,EOP	0000	+	1110
1	0001	(not used)	0001	-	0110
2	0010	D	0010	×	0111
3	0011	J	0011	÷	1111
4	0100	M IN	0100	=	1001
	0101	M CLR	0101	√	1011
	0110	-	0110	R	1101
	0111	×	0111	M	1010
illum-0	1000	S	1000	M IN	0100
function	1001	=	1001	M OUT	1100
	1010	M	1010	M CLR	0101
5	1011	√	1011	S	1000
6	1100	M OUT	1100	D	0010
7	1101	R	1101	J	0011
8	1110	+	1110	null,EOP	0000
9	1111	÷	1111	(not used)	0001

The W bit has a weight of 2.

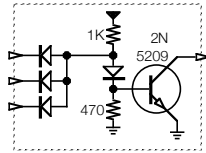
IC Pinouts



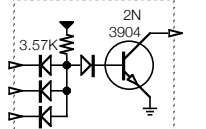
IC technology is current-sinking.
Inputs are DTL/TTL.
Gate outputs are open-collector.
Flip-flop outputs have ~ 1.1K pull-up resistors.

Inferred for 504 flip-flops:
G = Gate Input
Ø = Clock Input
G=1 enables the JK inputs.
The outputs transition on +edge of Ø.

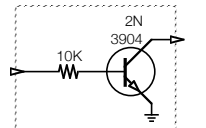
Discrete Gate Substitute (implemented/used 2024 Nov)



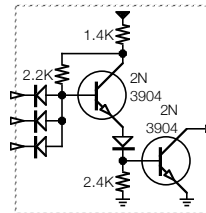
~0.5 μ S delay from input
-edge to output +edge.



Slow. Used a few times
at number cycle level.

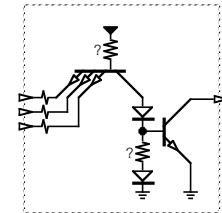
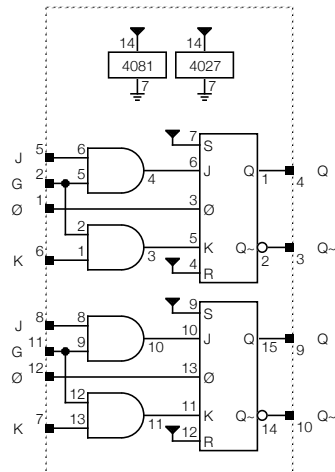


Tailored 3F309.5
for pulse capacitor drive.

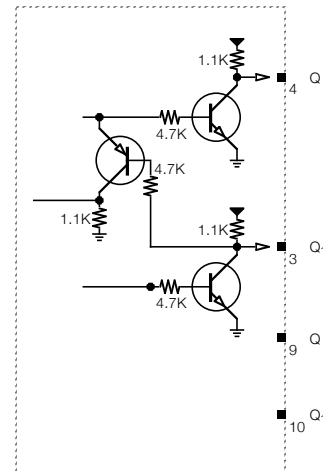


Higher speed.
Based on SN3900.

504 Substitute No Async S/R (implemented/used 2025 Feb)



RE'd from die observation.
Some presumptions
regarding input transistor.



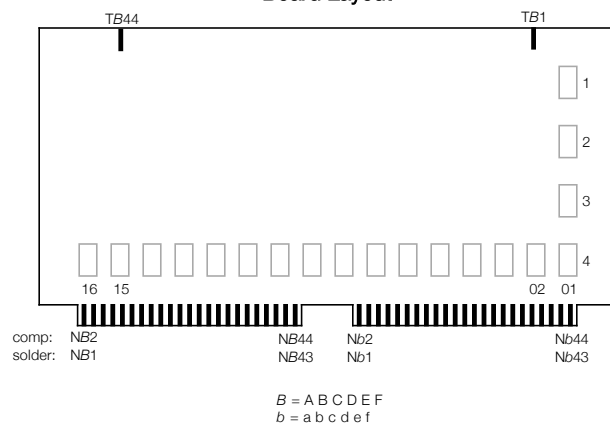
Sony SOBAX 2500 Calculator

Section: Bit Codes & IC Pinouts

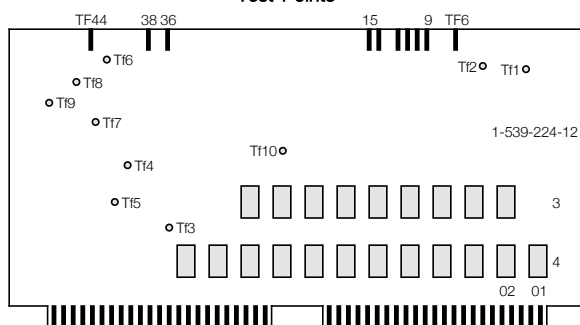
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Board Layout



Board F Test Points



• Note: ICs on Board A are oriented differently from the other boards.

Board Test Points

B	C	D	E	F
47 DXCA~	47 ØB01~	47 -	47 DM.1	47 -
46 DX B.W~	46 ØB.G	46 -	46 DM.1~	46 -
45 DX B.W	45 ØB01	45 -	45 DM.124W.G	45 -
44 DX A.W~	44 -	44 -	44 -	44 DLINJ
43 DX A.W	43 -	43 -	43 DMw~	43 -
42 DX.4	42 -	42 -	42 -	42 -
41 DX.4~	41 -	41 -	41 -	41 -
40 DX.2~	40 -	40 PM.1~	40 -	40 -
39 -	39 -	39 P18~	39 -	39 -
38 DX.2	38 -	38 PM.2~	38 -	38 QF26.B
37 -	37 -	37 PM.10	37 -	37 -
36 -	36 -	36 PM.8	36 -	36 QF21.C
35 -	35 -	35 PM.4	35 -	35 -
34 DX.24.G	34 RAw	34 PM.4~	34 -	34 -
33 -	33 -	33 SSKIP~	33 -	33 -
32 DX.1~	32 P0F	32 -	32 -	32 -
31 B210.6	31 -	31 -	31 -	31 -
30 CK.1~	30 -	30 -	30 -	30 -
29 CK.8	29 -	29 -	29 -	29 -
28 CK.8~	28 -	28 -	28 -	28 -
27 -	27 (Px2+x3+x6+x7)~	27 -	27 ØS15	27 -
26 PM.10~	26 -	26 -	26 -	26 -
25 CK.2	25 -	25 -	25 -	25 -
24 CK.1	24 -	24 -	24 -	24 -
23 CK.1248.G	23 -	23 -	23 -	23 -
22 DPC.8	22 -	22 -	22 SPPr.1	22 -
21 -	21 -	21 -	21 SPPr.1~	21 -
20 DPC.8~	20 -	20 P0A	20 SPPr.4	20 -
19 DPC.4~	19 -	19 RDNEG	19 SPPr.4~	19 -
18 DPC.4	18 -	18 RDNEG.J	18 SPPr.124.G	18 -
17 DPC.2~	17 P1C~	17 -	17 SPd.1~	17 -
16 DPC.2	16 -	16 -	16 SPd.1	16 -
15 DPC.1	15 -	15 -	15 SPd.1248.G	15 QF10.B
14 DPC.1~	14 P1E~	14 D208.9	14 -	14 TNUPF~
13 DPC.1248.G	13 -	13 DFp.1	13 SM.4~	13 -
12 ØDEXT	12 P1E	12 DFp.1~	12 SPd.8.K	12 TNUPF
11 -	11 OVf	11 DFp.1248.G	11 SM.1	11 ADLRD
10 INTØ	10 DYINC	10 -	10 SM.2	10 DLRCV
9 C.J.8~	9 DYINC~	9 -	9 SM.2~	9 DLRCV~
8 C.J.1248.G	8 OVf~	8 -	8 SMSET	8 -
7 C.J.8	7 DY.1	7 -	7 SMSET~	7 -
6 C.J.4	6 DY.1~	6 DF.8	6 EXEC~	6 QF7.B
5 C.J.2	5 DY.124.G	5 -	5 DN.1~	5 -
4 C.J.1	4 DY.4~	4 DF.4	4 DN.124W.G	4 -
3 C.J.1~	3 DYw~	3 DF.2	3 DN.2	3 -
2 C.J enable ++/digit	2 DY.4	2 DF.1248.G	2 DN.4	2 -
1 C.JHOME	1 DY.W.G	1 DF.1	1 DN.W	1 -

Sony SOBAX 2500 Calculator

Section: Board Layout & Test Points

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Section: Connectors
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Notes:
• Italicised expressions are connections with no signal name in the schematic.

• Bold-faced expressions are signal sources.

A			PM.4~ 2 1 PM.4			PM.4~ 2 1 PM.4~			PM.4~ 2 1 F44			PM.4~ 2 1 DXwb~			F409.4~ 2 1 F310.8								
ØD0~	44	43	9	9	44	43	ØD0	OVF~	44	43	P09~	OVF~	44	43	F43	d1, e26	44	43	E43				
ØD2~	42	41	—	8~	42	41	PM.8	PM.8	42	41	P13+17	PM.8	PM.10~	42	41	P09~	e11	42	41	KLEARN~			
ØD4~	40	39	7	7	40	39	CHGSGN~	PM.8~	40	39	P1D~	PM.8~	ØD0~	40	39	RSw	RSw	40	39	RDw~			
8~	38	37	6	6	38	37	ØD11~	PM.10~	38	37	P0A~	PM.10~	KTON	38	37	RS	RS	38	37	KCHECK~			
ØD11~	36	35	5	5	36	35	PM.10	PM.10	36	35	(P01+05+07~11+13+17)~	36	35	RS	PM.10	36	35	RT	36	35	RD		
—	34	33	4	4	34	33	PM.2~	PM.2	34	33	E32	PM.2	PM.2	34	33	RTw~	RTw~	34	33	RB			
OVF~	32	31	3	3	32	31	PM.2	PM.2	32	31	RBw	PM.2	C33, D34	32	31	ØD0	ØD0	32	31	RBw			
—	30	29	2	2	30	29	ØD0~	PM.1	30	29	Px2+ x3 + x6 + x7	30	29	P02+03	30	29	KF.8~	RAW	30	29	SM.1		
—	28	27	1	1	28	27	PM.1~	PM.1	28	27	(Px0+ x1)~	(Px0+ x1)~	KTREAD	28	27	E ØS	E ØS	28	27	RSwENB			
—	26	25	0	0	26	25	D26	ØD0	26	25	RAw	e3, B25	YB	26	25	F26	E25	26	25	pwr off			
ØB3	24	23	—	YB	24	23	DXCA	DXCA	24	23	(PFSR~·SST·x)~	—	ØB3	24	23	ØS5	ØS5	24	23	pwr off			
ØD15~	22	21	—	ØD15~	22	21	ØD15	ØD15	22	21	ØD15~	—	ØB3	22	21	ØS10	ØS10	22	21	RA			
DM=M1	20	19	—	Q	20	19	ØB3	ØB3	20	19	RDNEG	RDNEG	ØD15	20	19	ØS14	ØS14	20	19	ØB3			
RDNEG	18	17	ØDEXT~	ØDEXT~	18	17	DX	DX	18	17	RA	MAR	18	17	DX	DX	18	17	ØS0	ØS0	18	17	ØD15·B3
funct ind.	16	15	DP	funct ind.	16	15	ØB0	ØB0	16	15	D16	C15	16	15	—	DM=M1	16	15	ØS4	INIT~	16	15	ØS4
SPEXP	14	13	INIT~	DY=0~	14	13	C14	B13	14	13	DY=8~	DY=8~	14	13	— (PFEQ)	SPEXP	14	13	SP1ST	ØB0	14	13	GND
SP1ST	12	11	KCHECK~	DP	12	11	DXwa~	DXwa~	12	11	P16~	P16~	12	11	E12	D11	12	11	INITP~	INITP~	12	11	GND
ØB	10	9	ØB	INITP~	10	9	XOVF	XOVF	10	9	(P13+17)~	(P13+17)~	10	9	SM.2	SM.2	10	9	Ø	Ø	10	9	V-10
V+4	8	7	V+4	ØD15·B3	8	7	ØB3~	ØB3~	8	7	P11+16	P11+16	8	7	ØD15·B3	ØD15·B3	8	7	Ø	Ø	8	7	V+4
GND	6	5	GND	ØB	6	5	ØB	ØB	6	5	ØB	ØB	6	5	ØB	ØB	6	5	ØB	ØB	6	5	ØB
V+8 unreg	4	3	V+8 unreg	V+4	4	3	V+4	V+4	4	3	V+4	V+4	4	3	V+4	V+4	4	3	V+4	V+4	4	3	V+4
V+200	2	1	V+130	GND	2	1	GND	GND	2	1	GND	GND	2	1	GND	GND	2	1	GND	GND	2	1	GND

Section	Signal	Description
Timing	ØS	Master timing and power-on initialisation.
	ØSn	Channel slice clock, this is the master clock.
		Channel slice timing. The bits of the 15 main registers are interleaved in the Acoustic Delay Line by slicing each register-layer bit into 16 channels. The remaining slice is used for synchronizing the frequency of the master clock to the cycle time of the delay line.
	ØB	Register-layer bit clock bit.
	ØBn	Bits of a digit.
	ØDn	Digits of a number.
	ØDEXT	During some calculation phases, the 16-digit cycle is extended one digit period by inserting another digit period between ØD11 and ØD12. The inserted period is ØDINS.
		Ready to start tuning process after power-on.
	TNRDY	Tune UP Fine. 1 enables slow charge of charge pump controlling master clock.
	TNUPF	Tune UP Coarse. 1 enables fast charge of charge pump controlling master clock.
	TNUPC	Tuning Voltage. Frequency control input to master clock.
	TNV	Initialisation. 1 when power is turned on, goes 0 after initialisation is complete.
	INIT	Initialisation pulses. A stream of pulses during initialisation.
	INITP	Power Off Pulse.
	PWROFFP	
Keyboard		The keyboard and encoders for numerals and functions.
	KMAN	Manual mode.
	KAUTO	Execute program mode.
	KLEARN	Learn program mode.
	KOPER	Operate mode.
	KCHECK	Program LIST or EDIT mode.
	KEDIT~	Program EDIT mode.
	KTON	Tally mode on.
	KTREAD	Tally read.
	KR54	5 up / 4 down rounding mode.
	KRDWN	Round down mode (truncate).
	KRØD	Selected digit pulse for rounding.
	KCA	Clear all.
	KCE	Clear entry.
	KSL	Shift left.
	KSR	Shift right.
	KSCS	Shift or change sign.
	KDP	Decimal point.
	KPS	Program step (S key).
	KF.1,2,4,8	Encoded function keys. These are the same as DF.1,2,4,8.
	KN.1,2,4,W	Encoded numeral keys.
Supervisor	SM.1,2,4	S-Machine state register bits.
	S<n>	S-Machine states {0,1,2,5,6,7}.
	EXEC	Execution active.
	OVF	Overflow latch.
	SST	Start
	SNML	Numeral expected.
	SMSSET	In MEM-SET operation.
	SMSKIP	Skip instructions during program execution.
	SADDEOP	Add an End-of-Program instruction (function code 0) into the program store.
Procedure	PM.1,2,4,8,10	P-Machine state register bits (hex).
	P<2-hex>	P-Machine states - 0::1F.
	PNCEXT	States which extend the number cycle to 17 digits.
	PF...	Combinations of the function register DF and PM state.
	PINFX	Infix operand management.
	PNEWN	A new number is in RD (first numeral has been entered).
	PNEWN2	
	PDPE	DP entered during number entry.
	PNEG	Negation tracking flag during procedure execution.
	PPHE,PPH2	Phase End and Phase 2 flags for M,D,Q.
	PQPA	Pair Aligned for square root.
	PQRDØ	Square root, radicand digits of RB during number cycle.

Section	Signal	Description
CJ Counter		Utility counter
	CJHOME	
CK Counter		Utility counter: duty cycle dimming for thousands markers, realign-rotate loop counter
	CKHOME DPCTH	
DPC Counter		Decimal point position counter.
	UNITØD DP	The current ØD is the units digit. Signal to the display to turn on the decimal point.
SPC Counter		The program counter. This must select one of the 7 program registers in the E group as well as track a position within the selected register.
		Program at beginning.
		Program memory is expanding into the M7,6,5.
		ØD scanning is at the program counter location.
		Timing slice for selecting 1 of 7 program registers in the E register group.
	SP1ST SPEXP SPOVF SØDATPC RPØS	
Digits F & Fp		4-bit Function registers.
	DF.1,2,4,8 DFp.1,2,4,8	Function keystrokes and program instruction to be executed. Previous function.
Digit N		4-bit register for numeric keystrokes.
	DN DN=0	Bit stream output.
Digit X		4-bit register for arithmetic.
		Bit stream from the X register.
	DX DXCA DXOVF	Carry Flag.
Digit Y		4-bit register, incrementer.
		Bitstream output.
		DY performing an increment.
	DY DYINC DY=0 DY=8	
Digit M		4-bit register to indicate which memory is currently selected.
		Bit stream from the M register.
	DM DM=M1 RMØS	Memory 1 is selected. Timing slice for selecting 1 of 7 memory registers in the S register group.
Misc. Flags		Goes high during digits which are part of the integral portion of the number.
	INTØ RNDØ	
		Assessment of last RD digit.
	RDD=0,RDD>0 RDNEG	The number in the RD register is negative.
Register		15 16-digit registers for numbers and program instructions.
		Bit stream from the A register - accumulator.
		Bit stream from the B register - previous operand.
		Bit stream from the D register - current / displayed operand.
		During idle, illuminated zeroes are encoded as 1000, blanked zeroes remain 0000.
		11 16-digit registers shared between the 7 memories and program instructions.
		4 of these registers are reserved for memories 1,2,3 and 4.
		4 are reserved for program instructions.
		The remaining 3 are shared by memories 5,6,7 and program instructions in reverse overlapping order. Thus a long program will cut into memory 7, then memory 6 then 5.
		The maximum length of a program is (4+3)*16=112 instructions (functions).
		Bit stream from the Tally register.
	RA RB RD	
RT		Data selector for bit-stream into the A register.
	RS	
Raw		
	RBw RDw RTw RSw RSwENB	
		Enable input to the currently selected register in the S register group.
RACOMP RDCOMP RP		Complementary form of bit stream from the A register in accordance with PNEG.
		Complementary form of bit stream from the D register in accordance with RDNEG.
Channel		Bit stream from the S register for program instruction purposes.
ADLINJ ADLRD		Data bits for injection to the ADL.
		Reformed read pulses from the ADL.

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Section: Signal Names

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