

Toshiba BC-1212 Calculator

Contents	
Section	Page
Title & Contents (this page)	1
Notes	2
Block Diagram	3
Signals & State Diagram	4
State Descriptions	5
Timing Diagram	6
Timing	7
Keyboard	8
Control (Flag Registers)	9
Control (State Sequencing)	10
Control (Outputs)	11
Registers & Arithmetic	12
Decimal Point & Digit Counters	13
Display	14
Power Supply	15
IC Pinouts	16
Physical Layout & Connectors	17

Toshiba BC-1212 Calculator

Section: Title and Contents

Page: 1

Rendition: 2020 May 19

This schematic has been derived primarily through the reverse engineering of a Toshiba BC-1212 calculator, with some observation of a poor copy of the manufacturer's schematic. This is not the manufacturer's schematic.
bhlprt / 1996 Jul

Notes

- ◆ The symbol  denotes a physical connector pin where *c*=connector, and *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- ◆  connection between different sections.
 connection limited to same section.
 Arrows indicate direction of signal or energy flow.
- ◆ The symbol  denotes V-24.
- ◆ Capacitance in microfarads unless otherwise indicated.
- ◆ See www.cs.ubc.ca/~hilpert/eec for additional information.

Log

- ◆ These drawings based on unit with Serial No. 165632 z and a manufacturer schematic which appears to be dated 69/3/13.
- ◆ 1996 Jul: Initial drawing / bhilpert.
 2000 Apr: State diagrams and descriptions added / bh.
 2007 Jan: Some minor reorganisation of notes / bh.
 2011 May: Several symbol name corrections, noticed by Pavel Zima / bh.
 2020 May: Format updates / bh.

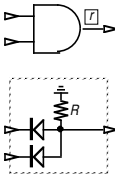
Logic Implementation

Most AND and OR gates are constructed from discrete diodes and resistors. Some gates, and more complex logic elements, are contained in integrated circuits.

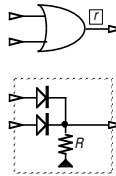
Gate symbols and signal names are presented in accordance with positive logic:
 logic 1 = 0V, GND
 logic 0 = V-24

The internal construction of discrete gates is shown in the following diagrams. A wire-AND or wire-OR construction is indicated by the input line traversing the width of the gate.

AND Gate

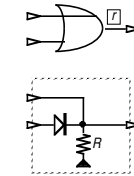


OR Gate



OR Gate

with 'wired' input



Most outputs have load resistors (*R*) connected from the output to one side of the power supply. For outputs from integrated circuits the resistor always goes to V-24. To reduce clutter these resistors are indicated in the schematic by one of the following letters (*r*) in a box near the output. The letters are the same as those printed on the circuit board to identify resistor values.

Symbol (<i>r</i>)	Resistance (<i>R</i>)
P	33K
Q	39K
R	24K
S	47K
V	100K
Y	470K
Z	220K
n	330K
—	no resistor

The TM4000 / μ PD Integrated Circuit Family

The integrated circuits are from an early family of MOS SSI / MSI technology produced by several Japanese manufacturers during the late 1960's to early 1970's. (Note these ICs are not CMOS and should not be confused with standard CMOS series ICs.)

- ◆ Outputs are open-collector, closing to GND (logic 1) and requiring external pull-down resistor to V-24 (logic 0). (See table above.)
- ◆ Inferred for flip-flops:
 The flip-flops in this logic family appear to be Master/Slave D-type flip-flops with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while all outputs are changed synchronously by a single clock signal.
 $\emptyset C$ = Capture Input (master section clock)
 $\emptyset T$ = Transition Input (slave section clock)
 The state of the D input is captured when $\emptyset C$ is logic 0 (V-24).
 The Q output is set in accordance with the captured state when $\emptyset T$ goes to logic 0.

Gate Identification

Gates and logic elements are identified by a symbol taking one of the following forms:

x / y refers to a gate constructed from discrete components
 $x /$ "
 $/ y$ "
 $g - n$ refers to a gate contained within an integrated circuit
 where
 x = number printed on board beside load resistor
 y = number on original schematic
 g = gate type identifier (see table below)
 n = number

Gate Type ID	Logic Element	IC Type
0	flip-flop	TM4103 or μ PD10
3	inverter	μ PD13
4	2 by 2 AND-OR gate	TM4005 or μ PD14
5	64-bit shift register	TM4105
6	60-bit shift register	TM4106
As	serial adder	TM4006

Some discrete gates have no distinguishing identifier.

There are two ICs identified as "0-9" on the boards and in the original schematic. This schematic distinguishes them as "0-9S" and "0-9D".

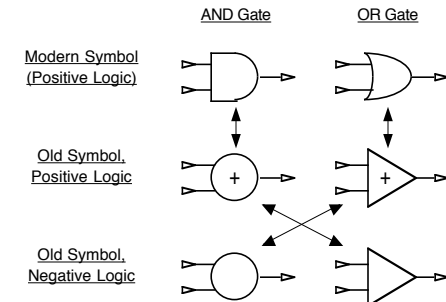
See "Physical Layout and Connectors" page for more about IC and gate location.

Original Schematic

The original schematic has some errors and uses some undocumented shorthand nomenclature.

- ◆ Logic 1 is GND (0V), logic 0 is V-24.
- ◆ Signals are named in terms of positive logic.

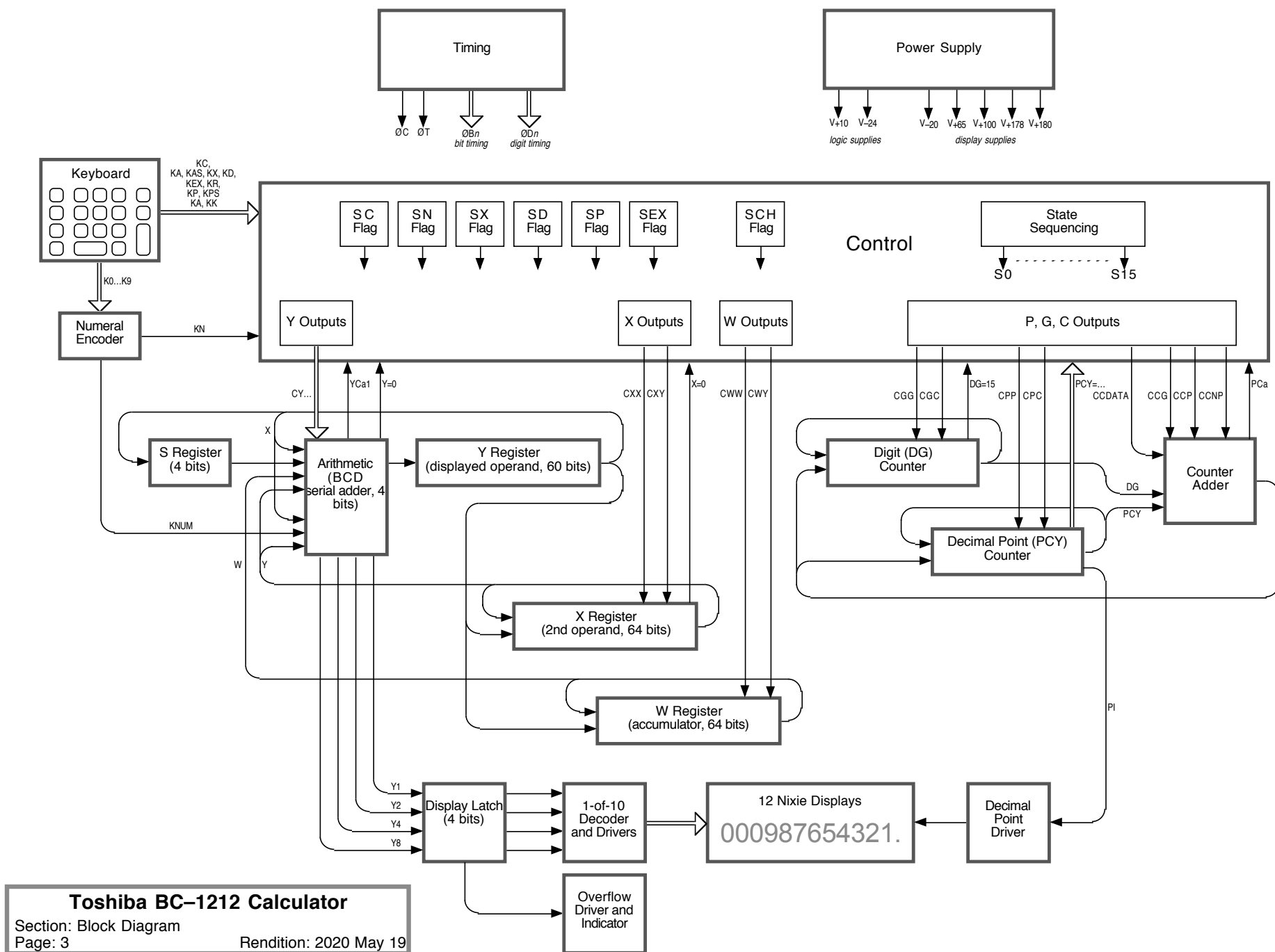
An old set of gate symbols is used. Both positive logic and negative logic gates are represented. Gate symbols with a "+" in them are positive logic gates, otherwise the gate is negative logic.



The double-ended arrows indicate identical construction, thus a positive-logic AND gate is constructed in the same manner as a negative-logic OR gate.

For the most part, the control portion of the calculator is constructed in terms of negative logic, the data portion is constructed in terms of positive logic.

Toshiba BC-1212 Calculator



Signal Names

Section	Signal	Description
Timing	Ø...	Master timing.
	ØC	Master clock, data capture phase.
	ØT	Master clock, toggle outputs phase.
	ØB...	Bit timing.
	ØD...	Digit timing (4 bits constitutes a digit).
	ØB8C	Capture pulse at the end of each digit.
	ØD16B8C	Capture pulse at the end of each full number cycle.
Keyboard	K...	The keyboard and numeral encoder. These signals all go to control.
Control	S..., C...	The state machine.
	SST	Flag indicating start of operation.
	SX	Flag indicating a multiply operation is pending.
	SD	Flag indicating a divide operation is pending.
	SXD	Combination of SX OR SD.
	SN	Flag indicating beginning/end of operands.
	SC	Flag indicating clear operation.
	SP	Flag indicating addition/subtraction and DP pressed.
	SCH	Flag to capture data conditions during the number cycle.
	S0...S15	The states of the state machine.
	CY...	Outputs from control to the Y register.
	CX...	" X register.
	CW...	" W register.
Y Register	Y...	The operand being displayed. Arithmetic is also incorporated in this register.
	Y1,Y2,Y4,Y8	BCD numerals on their way to the display.
	Y=0	
	YCa1	Borrow signal for the divide algorithm.
X Register	X...	The second operand.
	X=0	
W Register	W	The accumulator.
PCY Counter	PCY...	Point Counter for the Y register. The decimal point timing counter.
	PCY=0	
	PCY=5	
	PCY<14	
	PCa	Signal to the display to turn on the decimal point at the appropriate time.
DG Counter	DG...	Digit counter. Used during multiply and divide to count digits.
	DG=15	

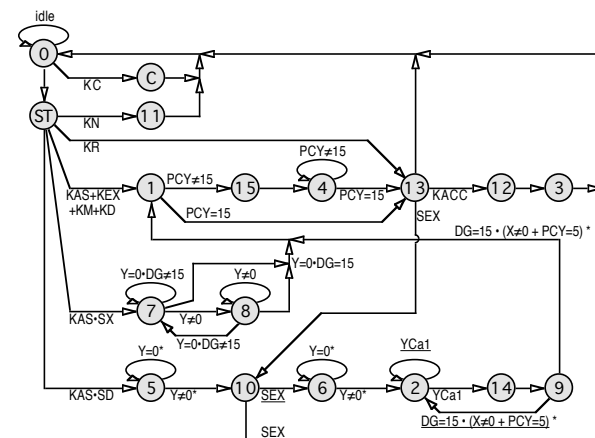
♦ A lowercase "n" in a signal name indicates the logical NOT operation.

State Diagram

Lines represent state transitions occurring at the end of each full number cycle. Labels for these lines are the conditions under which the transition occurs. Note the condition must exist at the end of the number cycle (ØD16B8C).

The SCH (presumably Catch-and-Hold) flip-flop is used to latch conditions which occur before the end of the number cycle. Labels noted with "*" are conditions caught by the SCH flip-flop.

The state numbers appear to have been chosen to simplify the hardware and have no symbolic relation to their place in the algorithm. Full descriptions of the activity which occurs during a state are presented in the table on the following page.



Algorithm Notes

The PCY and DG registers function as count-by-16 counters, thus the operations upon them are base 16.

During the display state (S0) the PCY counter decrements once per digit. When the bit pattern in PCY is 15, the decimal point indicator is turned on. Consequently, the value which appears in PCY during ØD16 is the number of decimal positions currently being displayed. i.e. If there are 3 decimal positions in the display, the PCY register will contain 3 during ØD16.

Negation is accomplished in the adder with no extra number cycles:

- The B input to the operand adder is complemented.
- Intra-digit carry in operand adder is normal due to double inversion.
- Initial (beginning of number cycle) borrow of 1 is generated in operand adder.
- Tens carry for sum≥16 is inverted.
- Tens carry generates correction in normalisation adder of 9+1=10.
- 9 is from inversion of 6, 1 is from first bit carry generation in normalisation adder.
- Otherwise correction is 15+1=0

Toshiba BC-1212 Calculator

Section: Signals and State Diagram

Page: 4

Rendition: 2020 May 19

State	Intent	Register Actions	PCY Counter Actions	DG Counter Actions
0	Idle (display loop).	—	PCY – 1 → PCY each digit, when PCY =15 turn on decimal point.	—
C	Clear just about everything.	0 → Y; 0 → X	0 → PCY	—
ST	Start. All sequences except clear come through this state to begin.	—	If multiply then PCY + PS → PCY.	0 → DG
11	Numeral and decimal point entry.	If numeral, then shift Y left one digit and enter keyboard numeral into LSD of Y.	If SP set (DP has been pressed) and not KDP then PCY + 1 → PCY. if KDP then set SP.	—
1	First stage of aligning the entered number (Y) to the selected number of decimal point positions (PS).	—	During first digit, if PCa from state 1 then PCY – 2 → PCY else PCY – 1 → PCY. PCY – 1 → PCY during all other digits.	—
15	Clear excess decimal places if more decimal places were entered than are selected by the decimal point position switch.	Clear digits of Y until PCY = 14 or 15.	PCY – PS – 1 → PCY	—
4	Rotate Y until in proper position according to PS. PCY was prepared for this phase during state 1. Loop terminates when PCY = 15.	Shift Y left one digit.	PCY + 1 → PCY	—
13	A somewhat overloaded state.	If addition then Y + X → Y. If subtraction then X – Y → Y. If multiply or divide then Y → X. If exchange do nothing. If recall then W → Y and, if accumulate then 0 → W.	PS → PCY	—
12	Accumulator update.	Y + W → Y; original Y → W.	—	—
3	Used during accumulator update.	Y ↔ W	—	—
7	During multiply, shift Y left until MSD of Y is non-zero.	Shift Y left one digit.	—	DG + 1 → DG
8	During multiply, repeatedly add multiplicand (X) to result (Y) and decrement multiplier (MSD of Y). Loop terminates when MSD of Y = 0.	Y + X → Y; —Y(MSD)	—	—
5	During divide, shift Y (the dividend) left as far as possible.	Shift Y left one digit.	PCY + 1 → PCY	—
10	During divide or exchange, swap X and Y registers.	X ↔ Y	If dividing then PS – PCY → PCY. If exchanging then PS → PCY.	—
6	During divide, shift Y (now the divisor) left as far as possible.	Shift Y left one digit.	PCY + 1 → PCY	—
2	During divide, repeatedly subtract divisor from dividend and increment quotient. Loop terminates when dividend goes negative (too many subtractions).	Y – X → Y; ++Y(LSD)	—	—
14	During divide, restore dividend and quotient because state 2 terminated with one extra subtraction.	Y + X → Y; —Y(LSD)	PCY + 1 → PCY	DG + 1 → DG (DG – 1 → DG 15 times)
9	During divide, ?	Shift digits of Y left until SCH occurs, clear other digits.	—	DG – 1 → DG each digit.

Toshiba BC-1212 Calculator

Section: State Descriptions

Page: 5

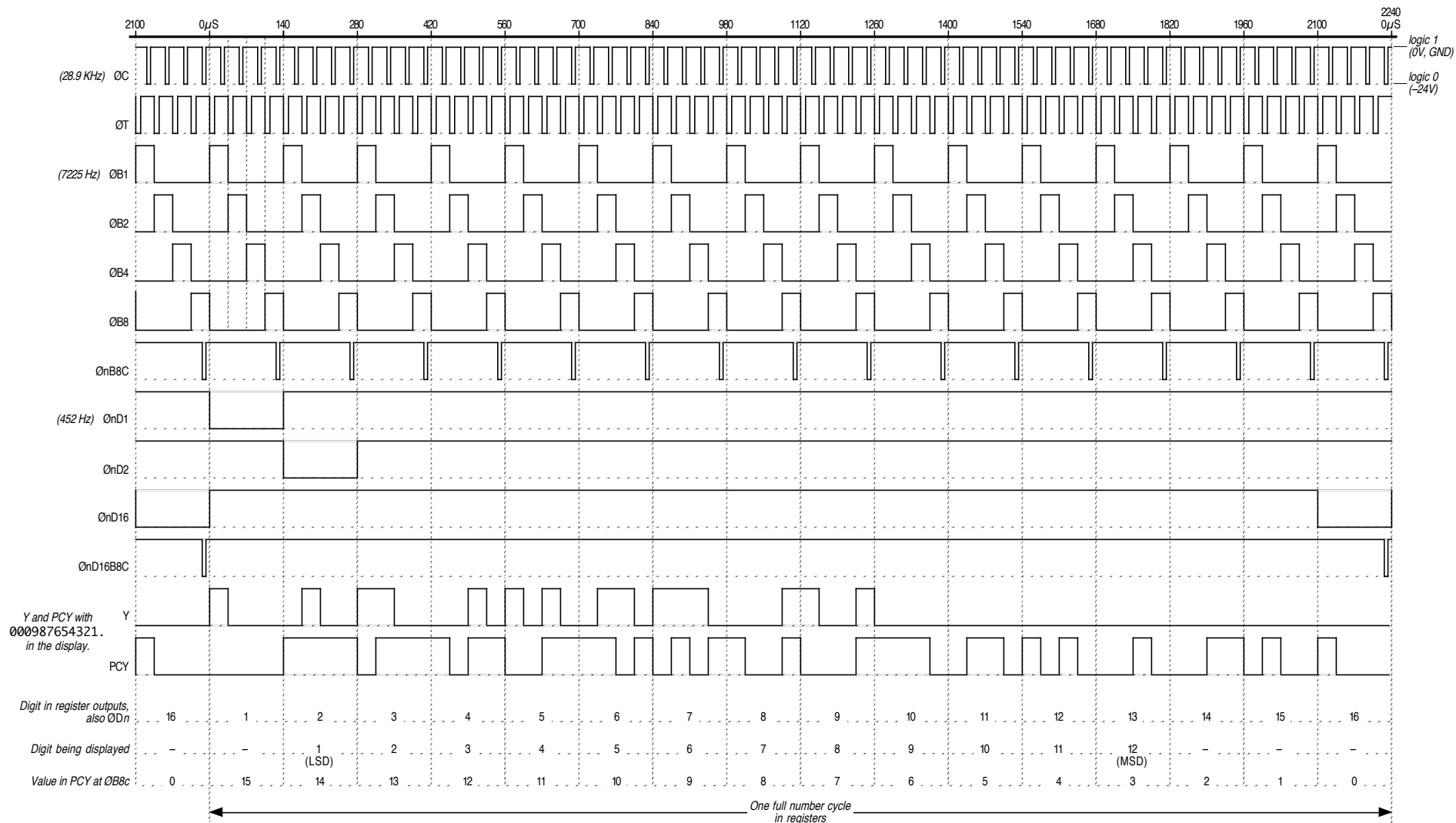
Rendition: 2020 May 19

Note:

PS = Point Set, the number of decimal positions selected by the decimal point position switch

LSD = Least Significant Digit

MSD = Most Significant Digit

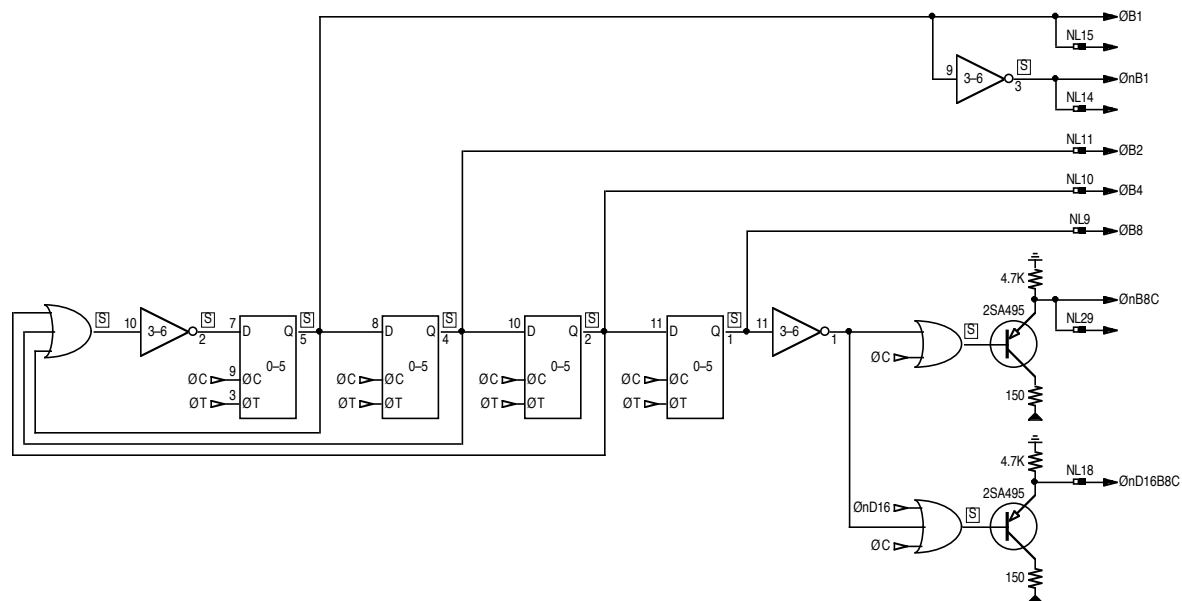


Toshiba BC-1212 Calculator

Section: Timing Diagram

Page: 6

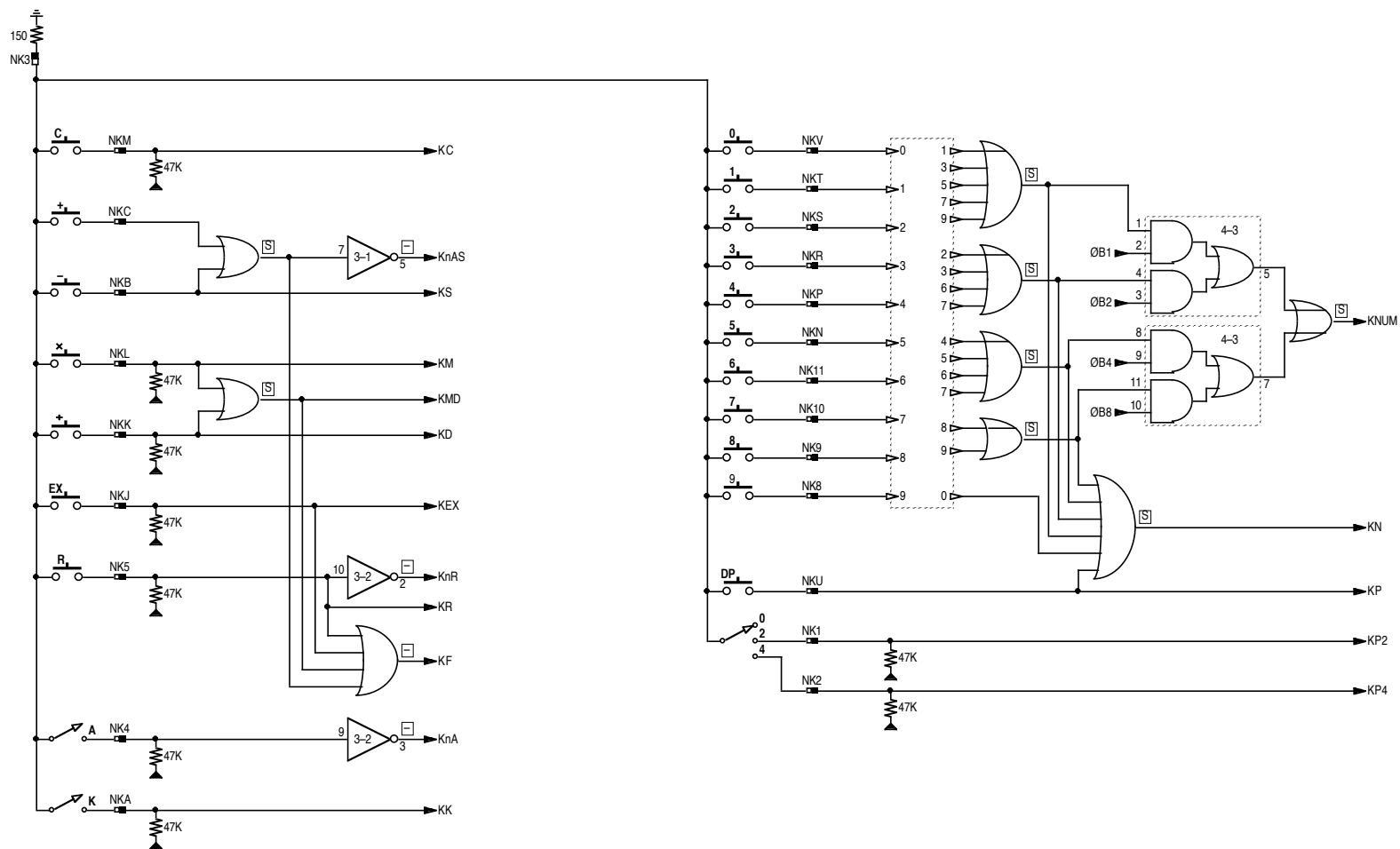
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Toshiba BC-1212 Calculator

Section: Timing
Page: 7

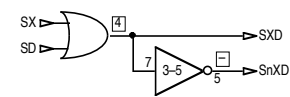
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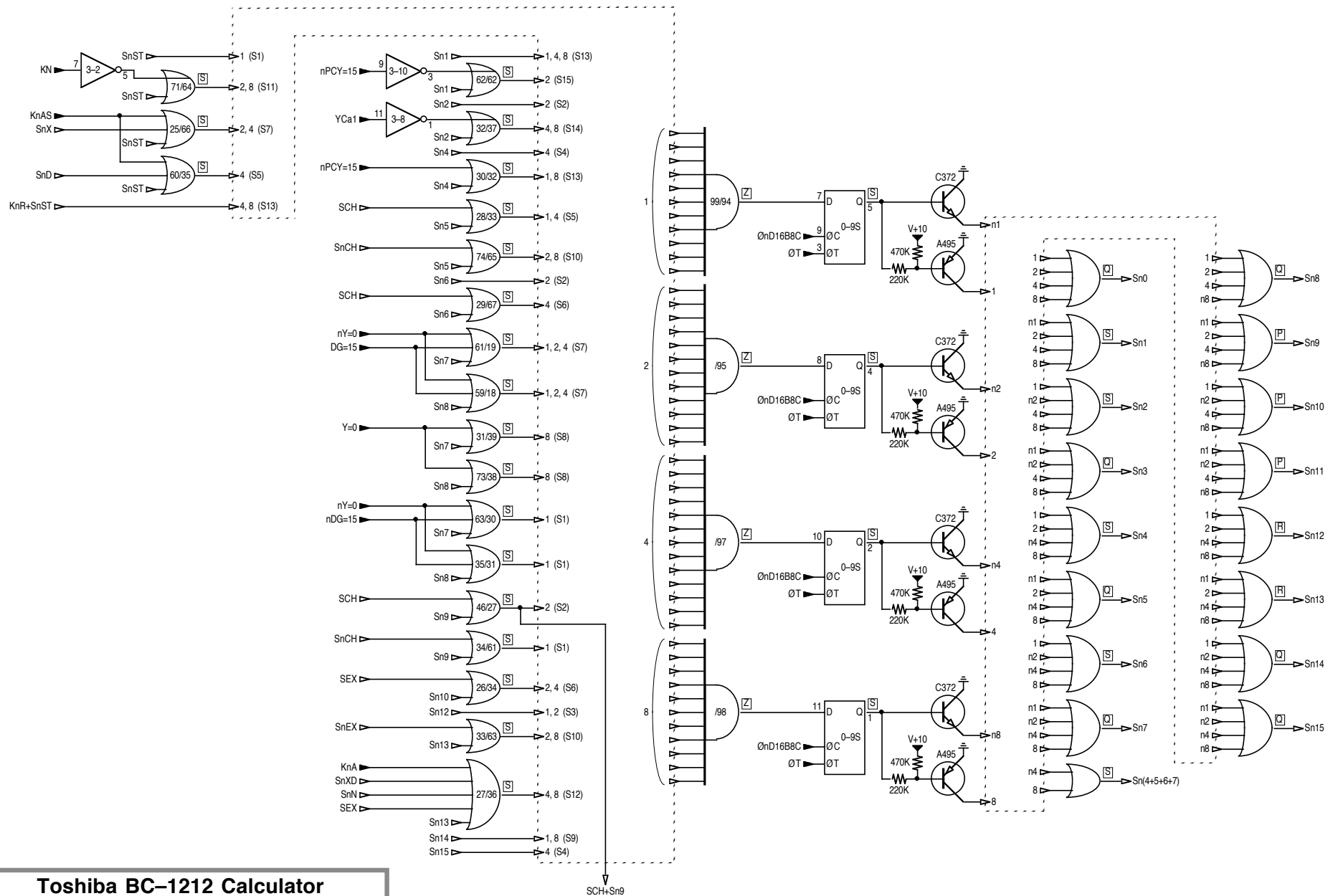


Toshiba BC-1212 Calculator

Section: Keyboard
Page: 8

Rendition: 2020 May 19



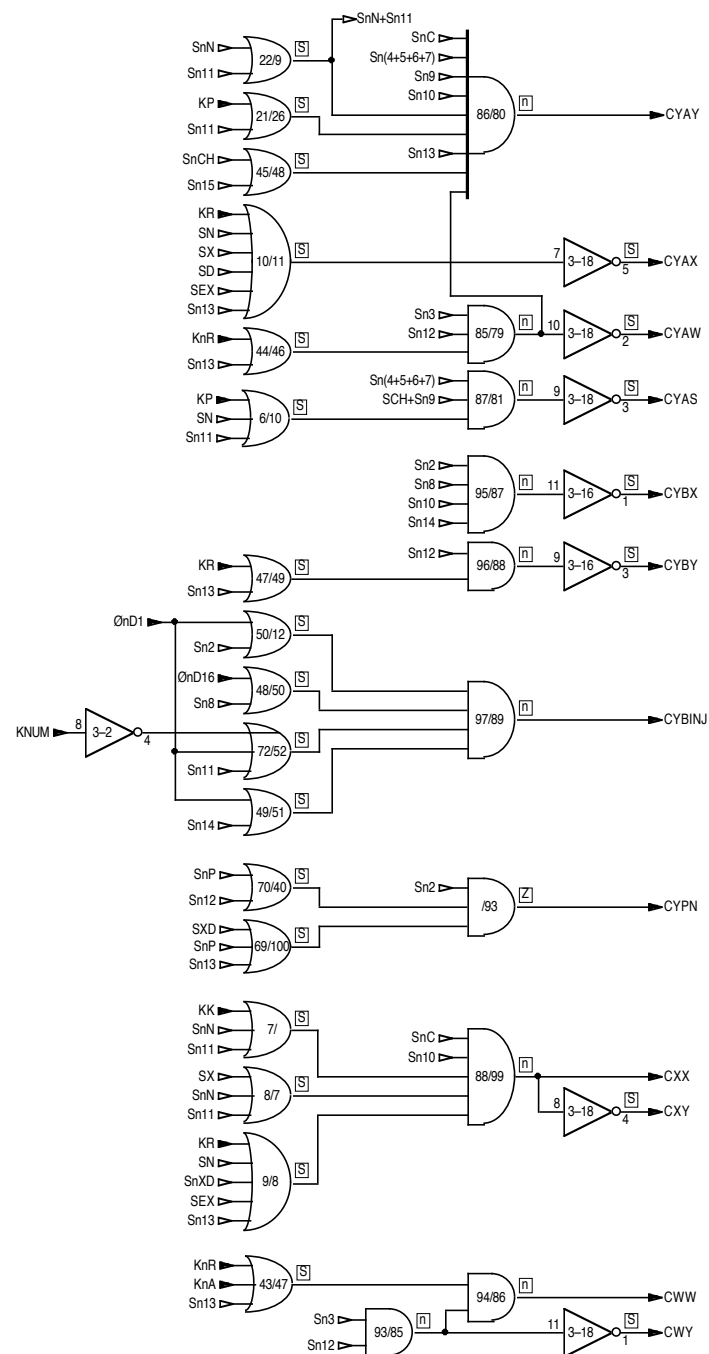
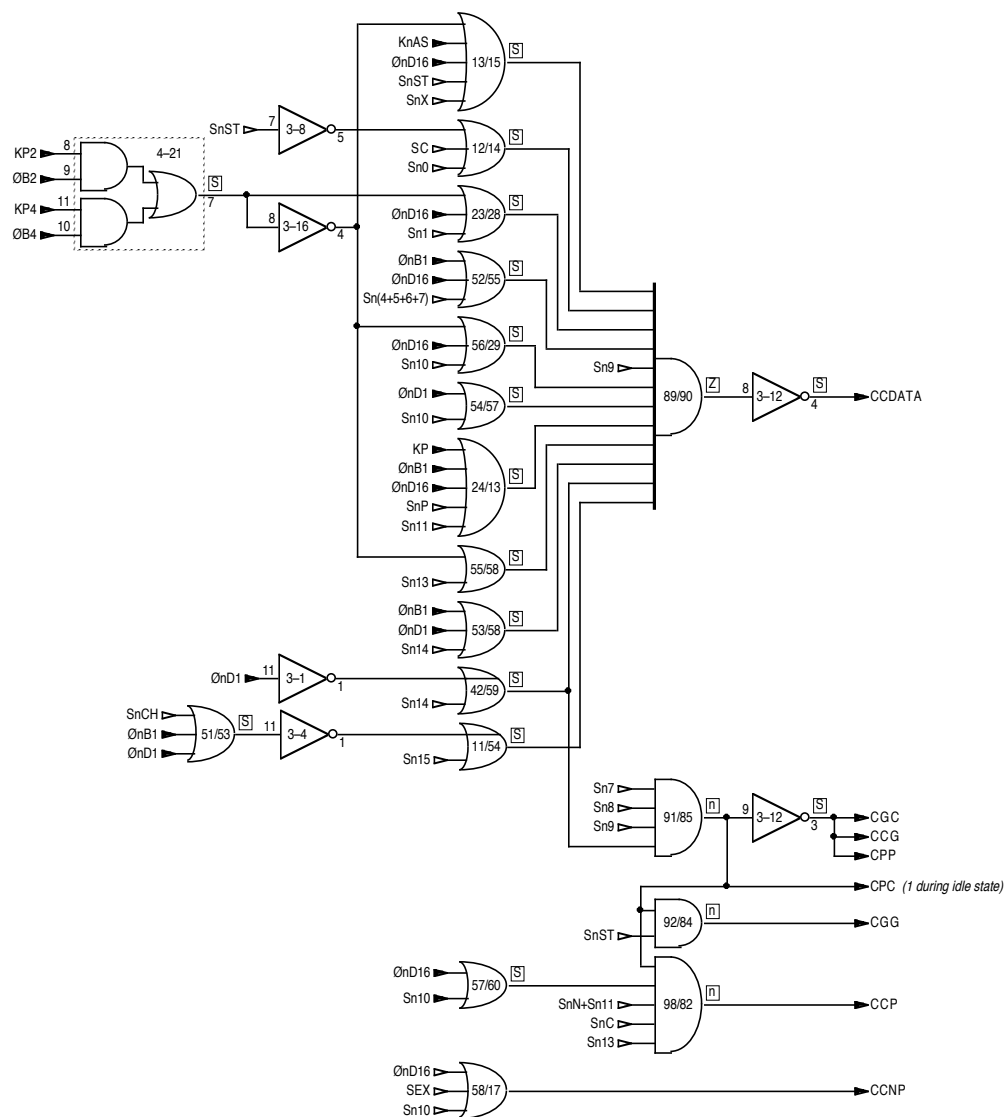


Toshiba BC-1212 Calculator

Section: Control (State Sequencing)

Page: 10

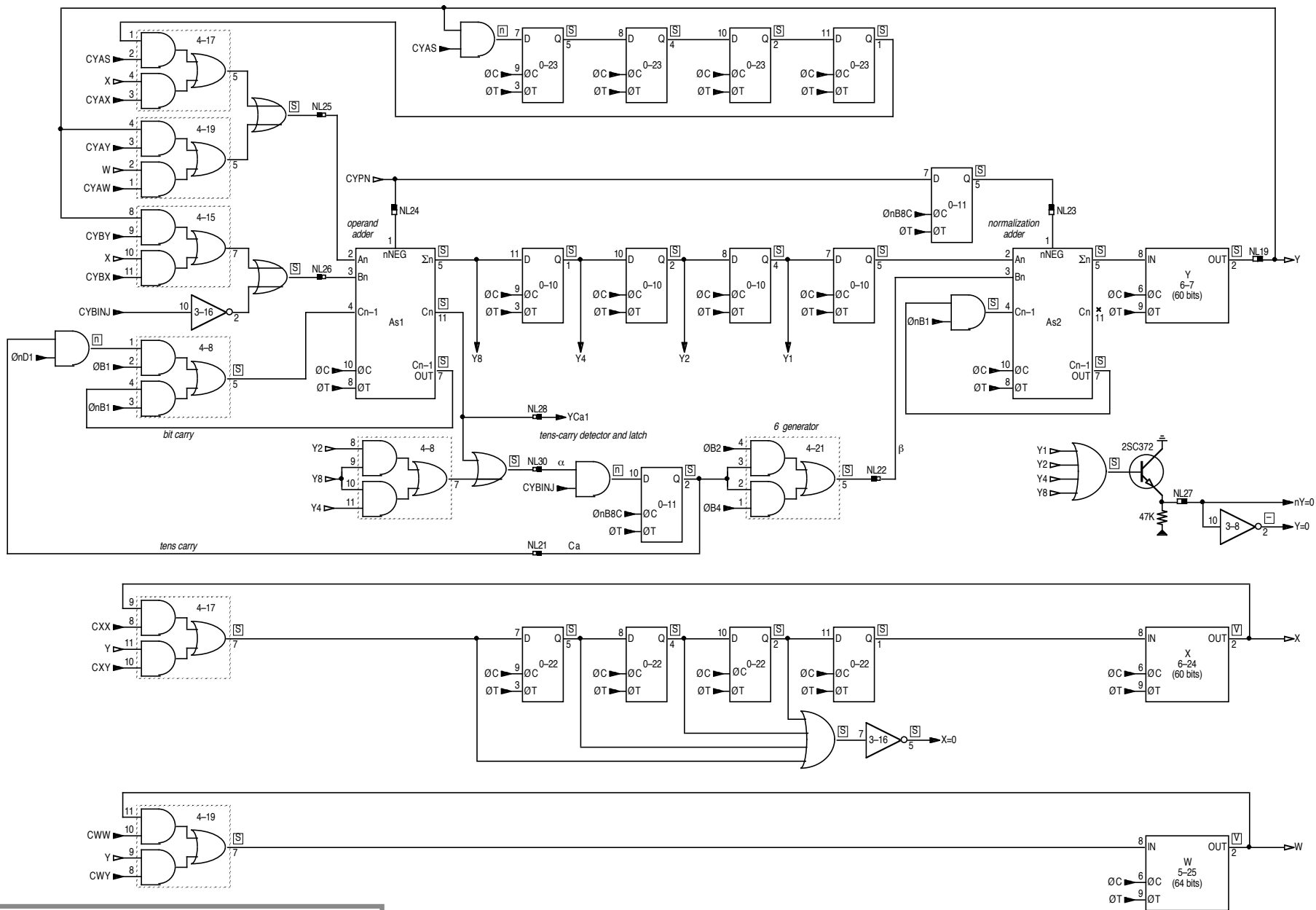
Rendition: 2020 May 19



Toshiba BC-1212 Calculator

Section: Control (Outputs)
Page: 11

Rendition: 2020 May 19

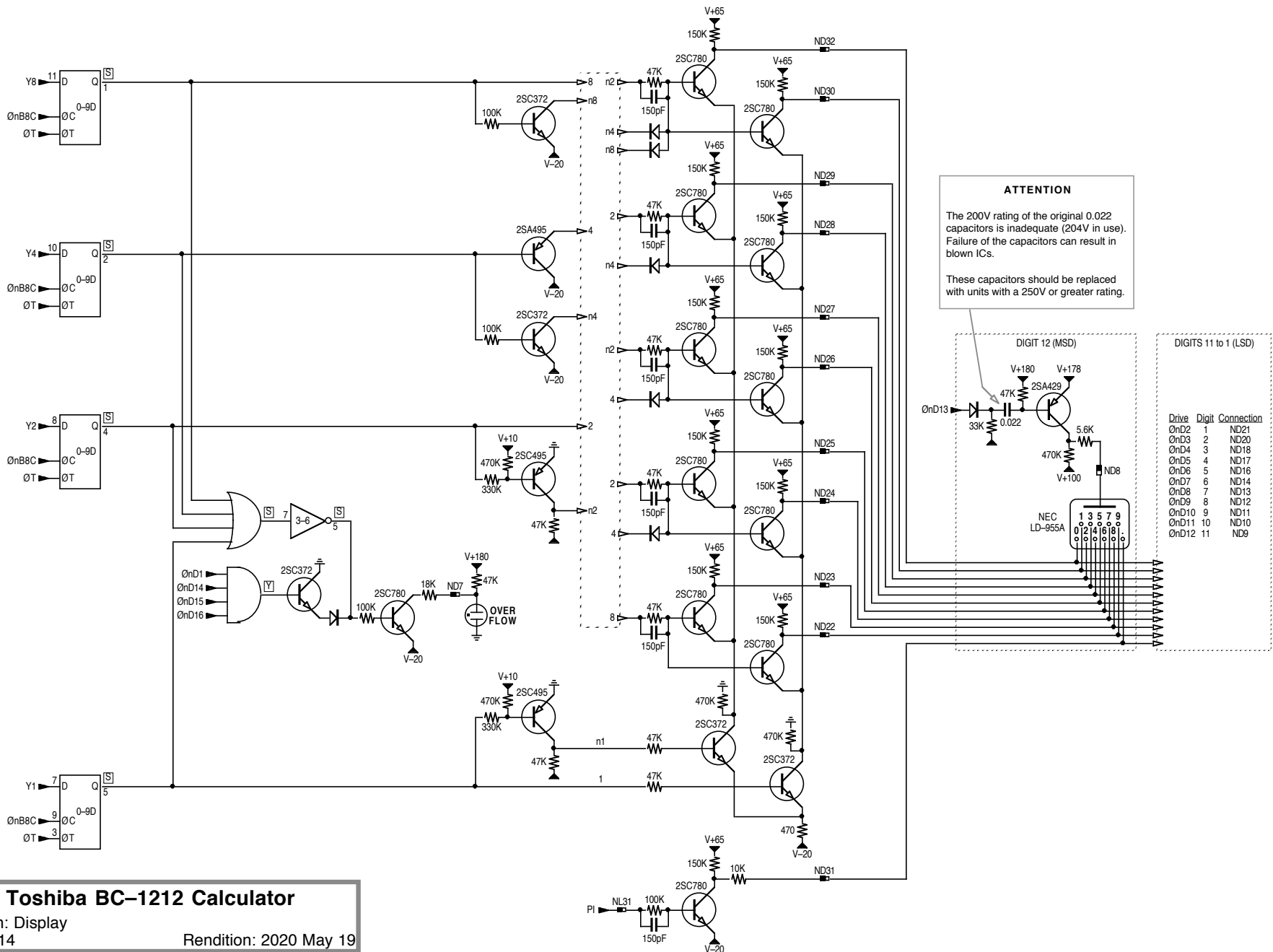


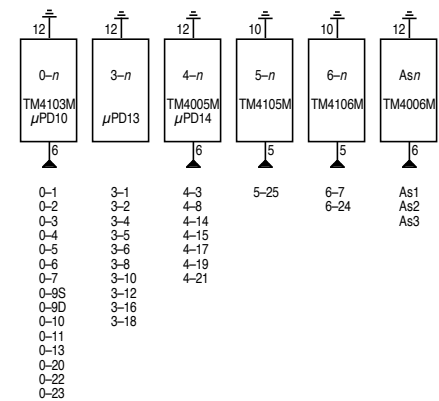
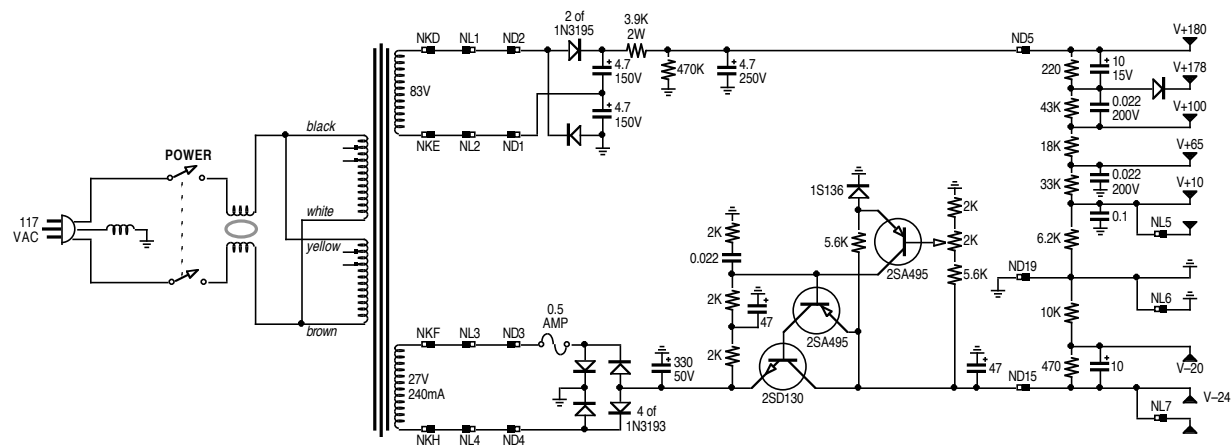
Toshiba BC-1212 Calculator

Section: Registers and Arithmetic

Page: 12

Rendition: 2020 May 19



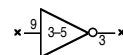


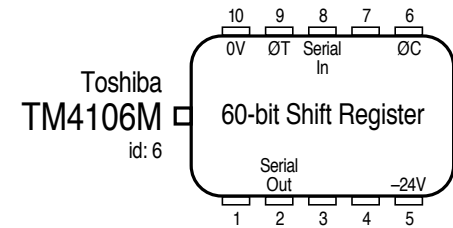
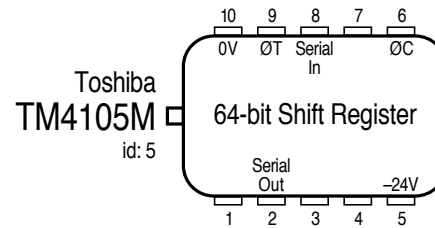
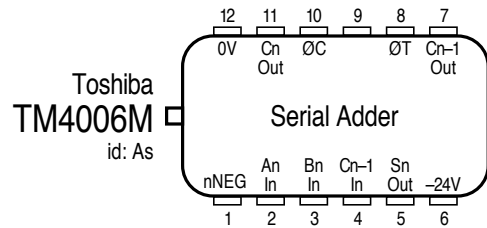
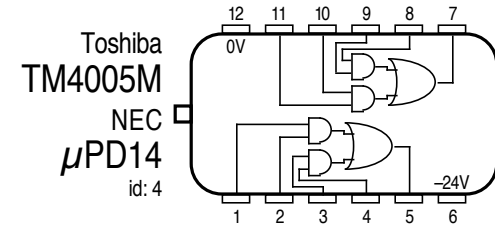
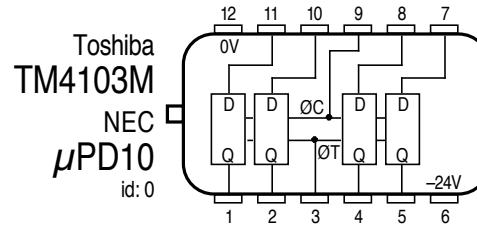
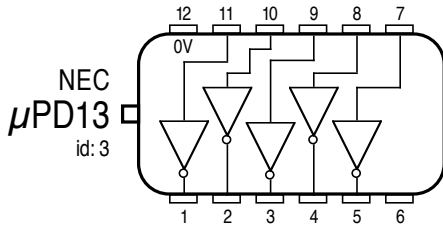
Toshiba BC-1212 Calculator

Section: Power Supply
Page: 15

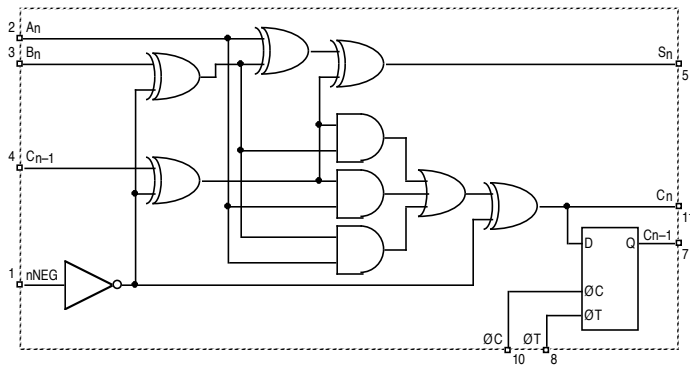
Rendition: 2020 May 19

Unused Gates





Equivalent Internal Structure
of TM4006 Serial Adder



Toshiba BC-1212 Calculator

Section: IC Pinouts
Page: 16

Rendition: 2020 May 19

- ◆ Logic 1 = 0V
Logic 0 = -24V
- ◆ Outputs are open-collector, closing to 0V (logic 1) and requiring external pull-down resistor to -24V (logic 0).

Connectors

NK			NL			ND		
KK	A	1	KP2	1	<i>xfmr hi-V</i>	1	<i>xfmr hi-V</i>	
KS	B	2	KP4	2	<i>xfmr hi-V</i>	2	<i>xfmr hi-V</i>	
KADD	C	3	kybd GND	3	<i>xfmr lo-V</i>	3	<i>xfmr lo-V</i>	
<i>xfmr hi-V</i>	D	4	KA	4	<i>xfmr lo-V</i>	4	<i>xfmr lo-V</i>	
<i>xfmr hi-V</i>	E	5	KR	5	V+10	5	V+180	
<i>xfmr lo-V</i>	F	6	—	6	GND	6	—	
<i>xfmr lo-V</i>	H	7	—	7	V-24	7	overflow	
KEX	J	8	key 9	8	ØnD15	8	digit 12	
KD	K	9	key 8	9	ØB8	9	digit 11	
KX	L	10	key 7	10	ØB4	10	digit 10	
KC	M	11	key 6	11	ØB2	11	digit 9	
key 5	N	12	—	12	—	12	digit 8	
key 4	P	13	—	13	ØT	13	digit 7	
key 3	R	14	—	14	ØnB1	14	digit 6	
key 2	S	15	—	15	ØB1	15	V-24	
key 1	T	16	—	16	ØnD16	16	digit 5	
KP	U	17	—	17	ØC	17	digit 4	
key 0	V	18	—	18	ØnD16B8C	18	digit 3	
				19	Y	19	GND	
				20	ØnD1	20	digit 2	
				21	Ca	21	digit 1	
				22	β	22	numeral 9	
				23	<i>SYPN delayed</i>	23	numeral 8	
				24	SYPN	24	numeral 7	
				25	<i>Y op adder, A in</i>	25	numeral 6	
				26	<i>Y op adder, B in</i>	26	numeral 5	
				27	nY=0	27	numeral 4	
				28	Ca1	28	numeral 3	
				29	ØnB8C	29	numeral 2	
				30	α	30	numeral 1	
				31	—	31	decimal point	
				32	PI	32	numeral 0	

Note:

- ♦ Italicised expressions are connections with no signal name in the schematic.

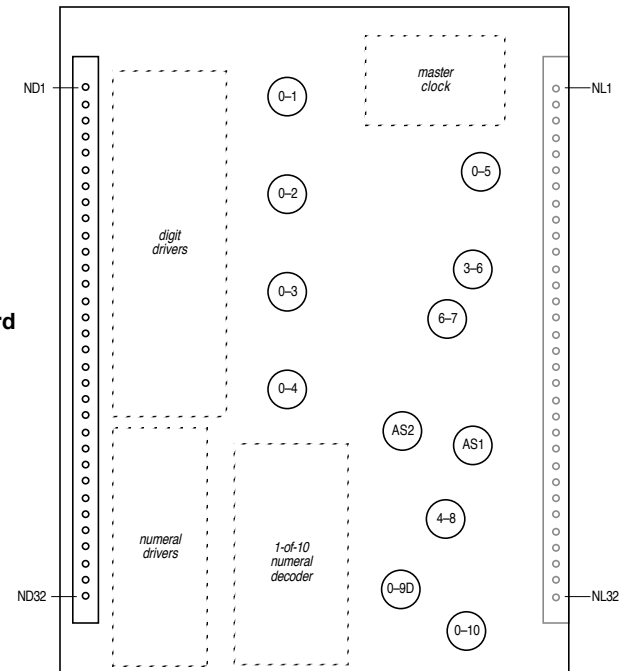
Toshiba BC-1212 Calculator

Section: Physical Layout and Connectors

Page: 17

Rendition: 2020 May 19

Middle Board
(top view)



Lower Board
(top view)

