

HITACHI MOS INTEGRATED CIRCUIT HD3101

DESCRIPTIONS

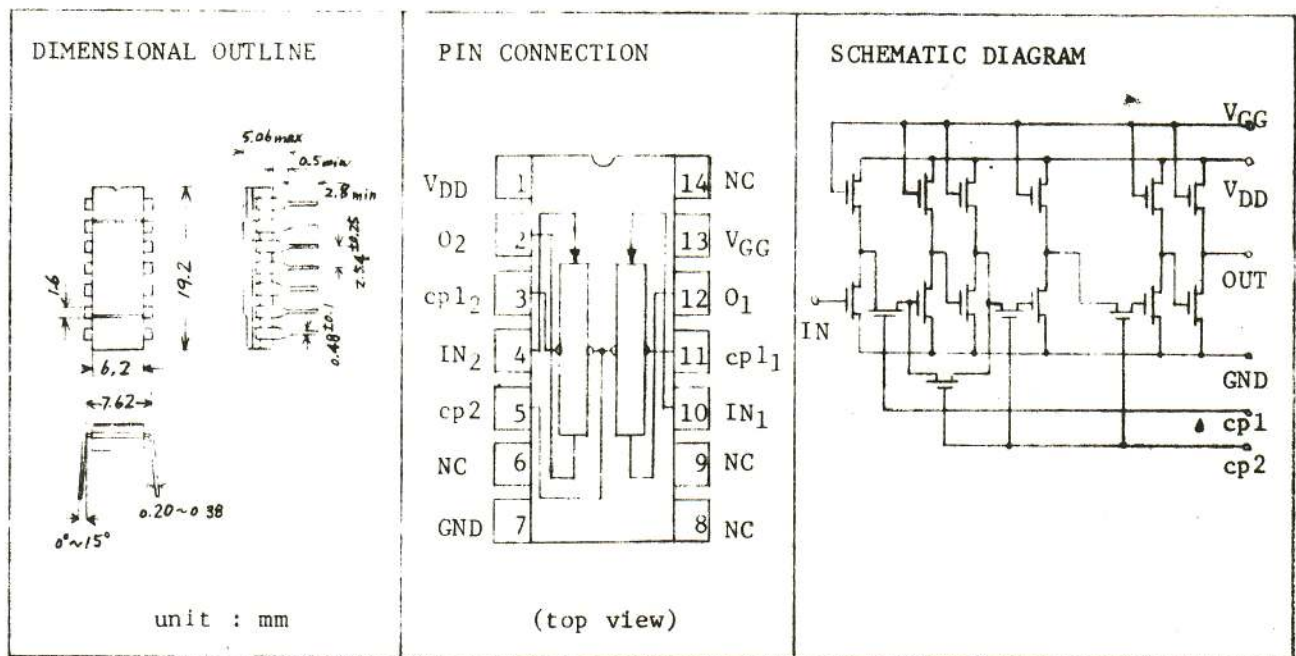
The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3101 is a dual 8 bits quasi-static shift register constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator.

And HD3101 is available in a dual in line type ceramic package (14 leads).

The HD3101 functions as an 8 or 16 bits shift register, an 8 or 16 bits ring counter, and others.

The features of HD3101 are as follows:

- Integrated zener clamp protects gates.
- Large noise margin $NM_L = 1.0V$, $NM_H = 2.0V$
- Wide operating frequency range DC to 100 kHz.
- Wide operating temperature range $-20^{\circ}C$ to $+75^{\circ}C$.



ABSOLUTE MAXIMUM RATINGS at 25°C ambient temperature

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating temperature	T_{opr}	$-20 \sim 75$	$^{\circ}C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^{\circ}C$

(to be continued)

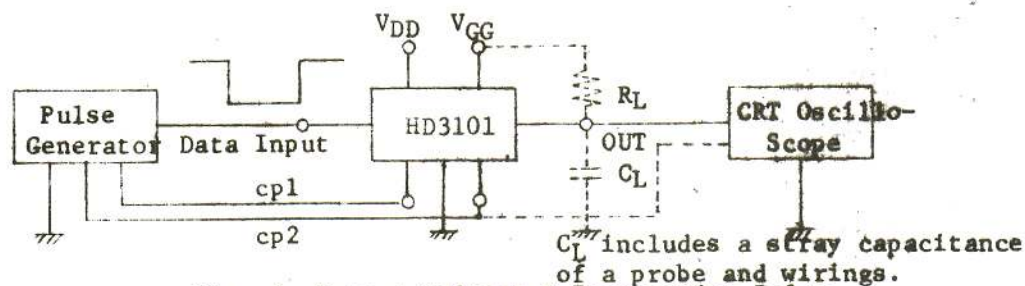
ELECTRICAL CHARACTERISTICS

($-V_{GG}=24V \pm 10\%$, $-V_{DD}=14V \pm 10\%$, $T_a=25^\circ C$)

ITEMS		SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	0 Level	$-V_{IL}$	9.0			V	$T_a=75^\circ C$
	1 Level	$-V_{IH}$			4.0	V	
Output Voltage	0 Level	$-V_{OL}$	10			V	$T_a=75^\circ C$, $cpw=1.0\mu s$, $f_{cp}=5kHz$
	1 Level	$-V_{OH}$			2.0	V	
Clock Voltage	0 Level	$-V_{cPL}$	19		26.4	V	$T_a=75^\circ C$, $cpw=1\mu s$
	1 Level	$-V_{cPH}$			4.0	V	
Min. Clock Frequency	Clock 1	f_{cplmin}			0	Hz	$cpw=1.0\mu s$, $f_{cp2}=5kHz$, $T_a=75^\circ C$
	Clock 2	f_{cp2min}			5	kHz	$cpw=1.0\mu s$, $f_{cpl}=5kHz$, $T_a=75^\circ C$
Clock Pulse Width		cpw	1.0			μs	See Fig. 2.
Clock Capacitance		C_{cp}			13	pF	$f=1MHz$, $V_{cp}=0V$
Input Resistance		R_{in}	10			M Ω	$-V_{in}=26.4V$
Input Capacitance		C_{in}			5.0	pF	$f=1MHz$, $V_{in}=0V$
Output Capacitance		C_{out}			8.0	pF	$f=1MHz$, $V_{out}=0V$
Power Dissipation		P_d			100	mW	$-V_{GG}=-V_{cp}=24V$, $-V_{DD}=14V$
Propagation Delay Time	falling	t_{PHL}			1.5	μs	$-V_{in}=0 \sim 12.6V$, $f_{cp}=10kHz$, $C_L=20pF$, $R_L=\infty$, See Fig. 1 & 2
	rising	t_{PLH}			1.0	μs	
Clock Pulse Delay		cpd'	1.0			μs	See Fig. 2.

NOTE : Cpl is controllable when cp2 is given at from 5kHz to 100kHz repetition rate.

Cp2 is uncontrollable and always must be given at from 5kHz to 100kHz repetition rate.



OUTPUT WAVE FORMS

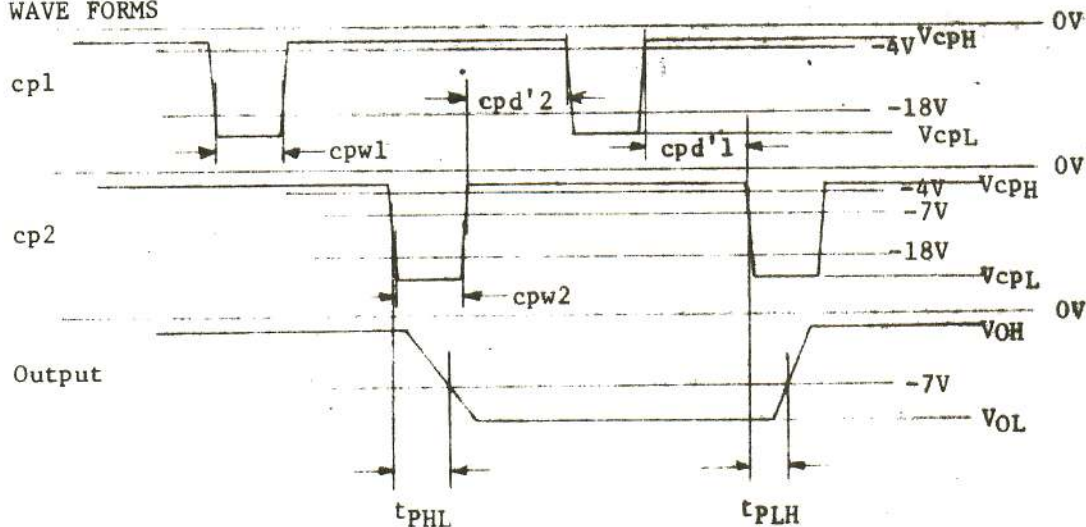


Fig. 2. Clock & Output Wave Forms

(to be continued)

TYPICAL TIMING CHART

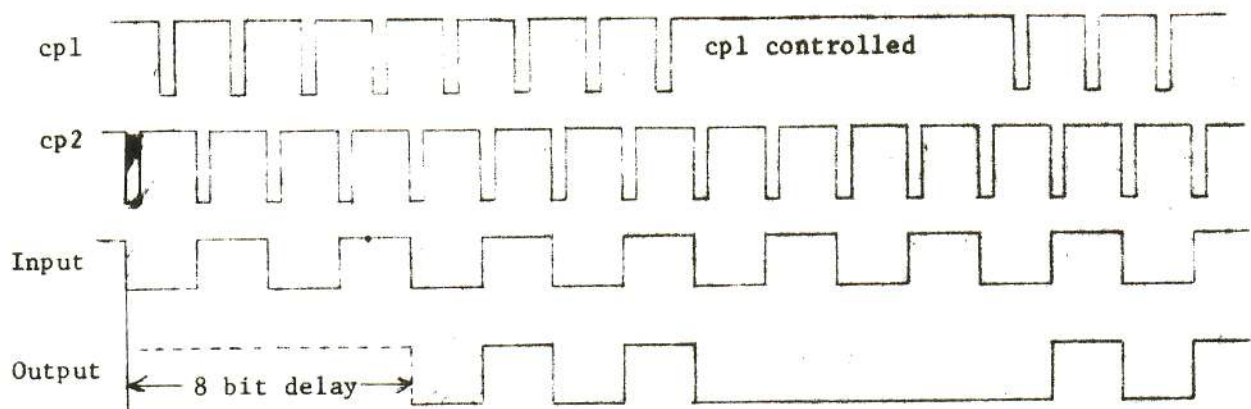


Fig. 3. Timing Chart

CLOCK PULSE GENERATOR BLOCK DIAGRAM

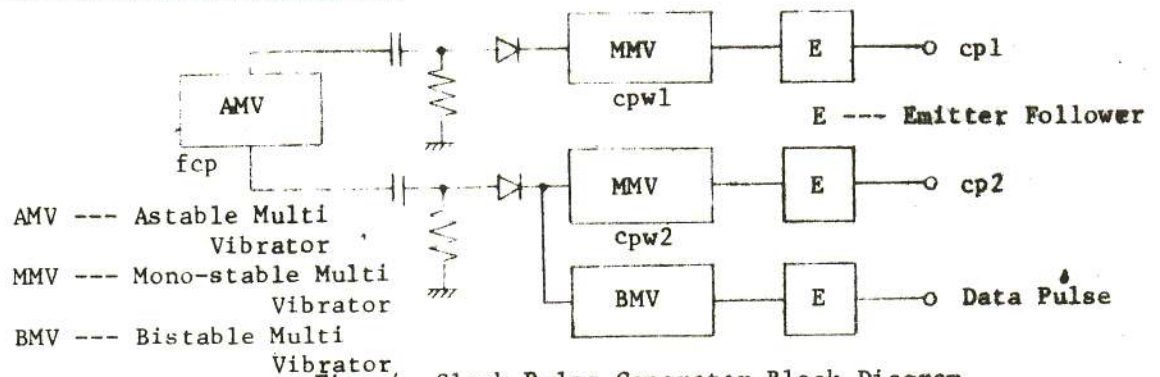


Fig. 4. Clock Pulse Generator Block Diagram

HITACHI MOS INTEGRATED CIRCUIT HD3103

DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3103 is a five MOS FETs constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3103 is available in a dual in line type ceramic package (16 leads).

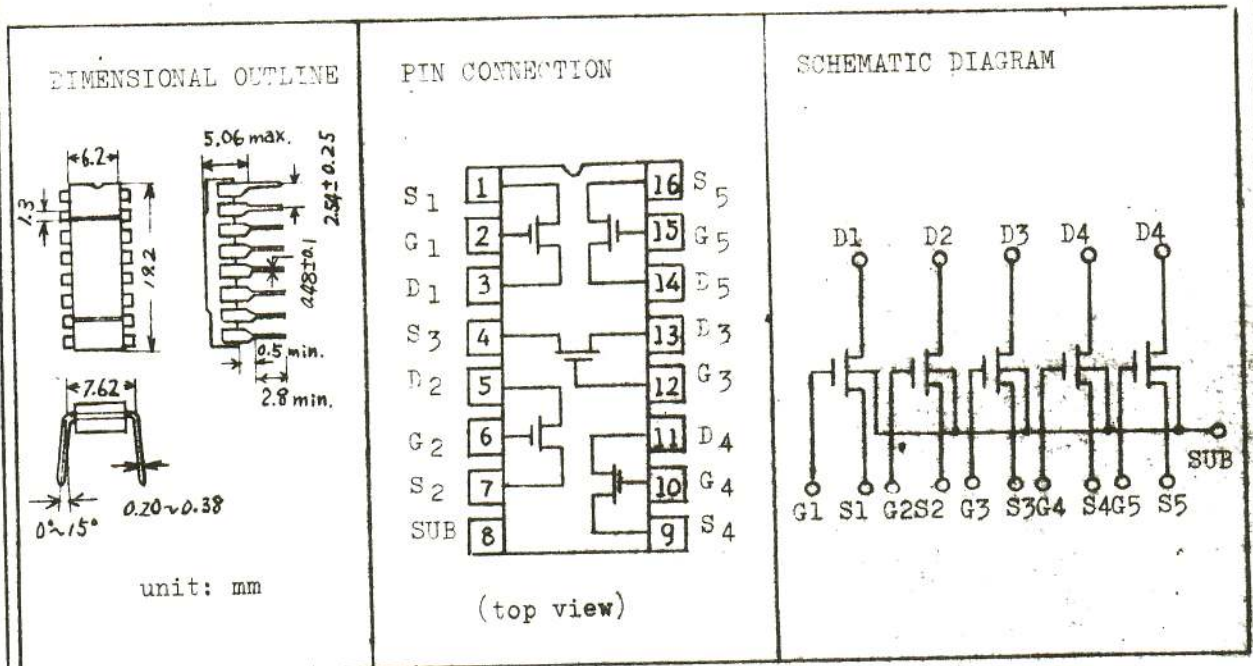
The HD3103 functions as a transfer gate, an inverter, exclusive OR circuits, and others.

The features of HD3103 are as follows :

Integrated zener clamp protects gates.

Large noise margin $NM_L = 10.0V$, $NM_H = 1.5V$

Wide operating temperature range $-20^{\circ}C$ to $+75^{\circ}C$



ABSOLUTE MAXIMUM RATINGS at $25^{\circ}C$ ambient temperature

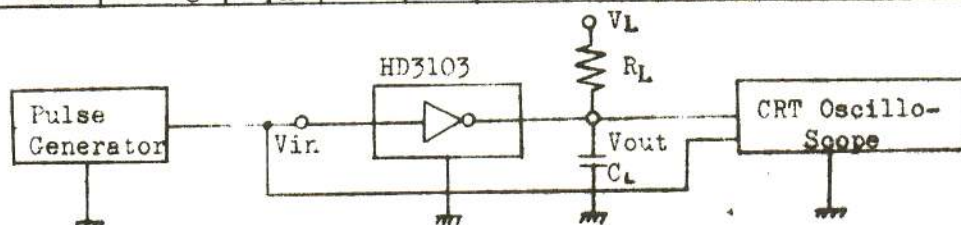
ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	-VT	-0.3~30	V
Operating Temperature	Topr	-20 ~ 75	$^{\circ}C$
Storage Temperature	Tstg	-55~150	$^{\circ}C$

(to be continued)

ELECTRICAL CHARACTERISTICS

($-V_L = 24V \pm 10\%$, $T_a = 25^\circ C$)

ITEMS		SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	0 Level	$-V_{IL}$	9.0			V	$T_a = 75^\circ C$
	1 Level	$-V_{IH}$			3.5	V	
Output Voltage	0 Level	$-V_{OLA}$	19			V	$R = 200K\Omega, T_a = 75^\circ C, -V_{in} = 3.5V$
	1 Level	$-V_{OHA}$		2.5		V	$R = 20K\Omega, T_a = 75^\circ C, -V_{in} = 9V$
	0 Level	$-V_{OLB}$	15			V	$R = 200K\Omega, T_a = 75^\circ C, -V_{in} = 4V$
	1 Level	$-V_{OHB}$		2.0		V	$R = 20K\Omega, T_a = 75^\circ C, -V_{in} = 9V$
	1 Level	$-V_{OHA}$		1.0		V	$R = 20K\Omega, T_a = 75^\circ C, -V_{in} = 15V$
Input Resistance		R_{in}	10			M Ω	$-V_{in} = 26.4V$
Input Capacitance	Drain	C_{ds}		8.0		pF	$-V_{DS} = 0V, f = 1MHz$
	Source	C_{ss}		8.0		pF	$-V_{SS} = 0V, f = 1MHz$
	Gate	C_{gs}		8.0		pF	$-V_{GS} = 0V, f = 1MHz$
Propagation Delay Time	falling	t_{PHL}		1.2		us	$-V_{in} = 0 \sim 12.6V$, See Fig.1 & 2.
	rising	t_{PLH}		1.2		us	$R = 20K\Omega, C_L = 50pF$



* C_L includes a stray capacitance of a probe and wirings.

Fig. 1. Propagation Delay Testing Circuit.

OUTPUT WAVE FORMS.

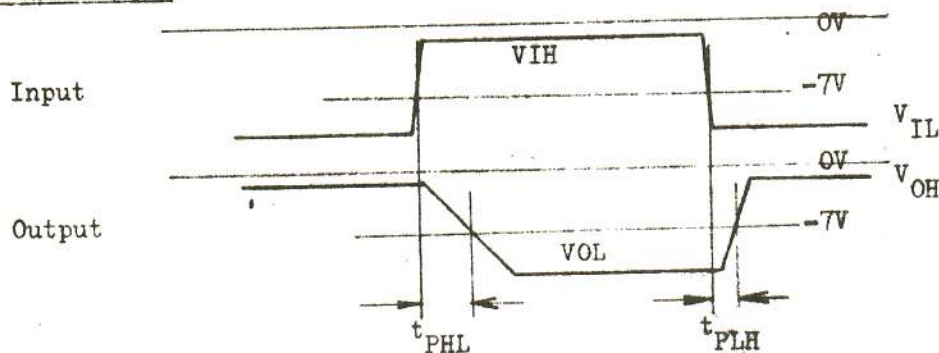


Fig. 2. Definition of t_{PHL} and t_{PLH}

HITACHI MOS INTEGRATED CIRCUIT HD3104

DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated circuit HD3104 is a dual 4 input AND gate + two inverters constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3104 is available in a dual in line type ceramic package (16 leads).

The HD3104 functions as a 4 input AND gate (positive logic), inverters, a 4 input NAND gate (positive logic), and others.

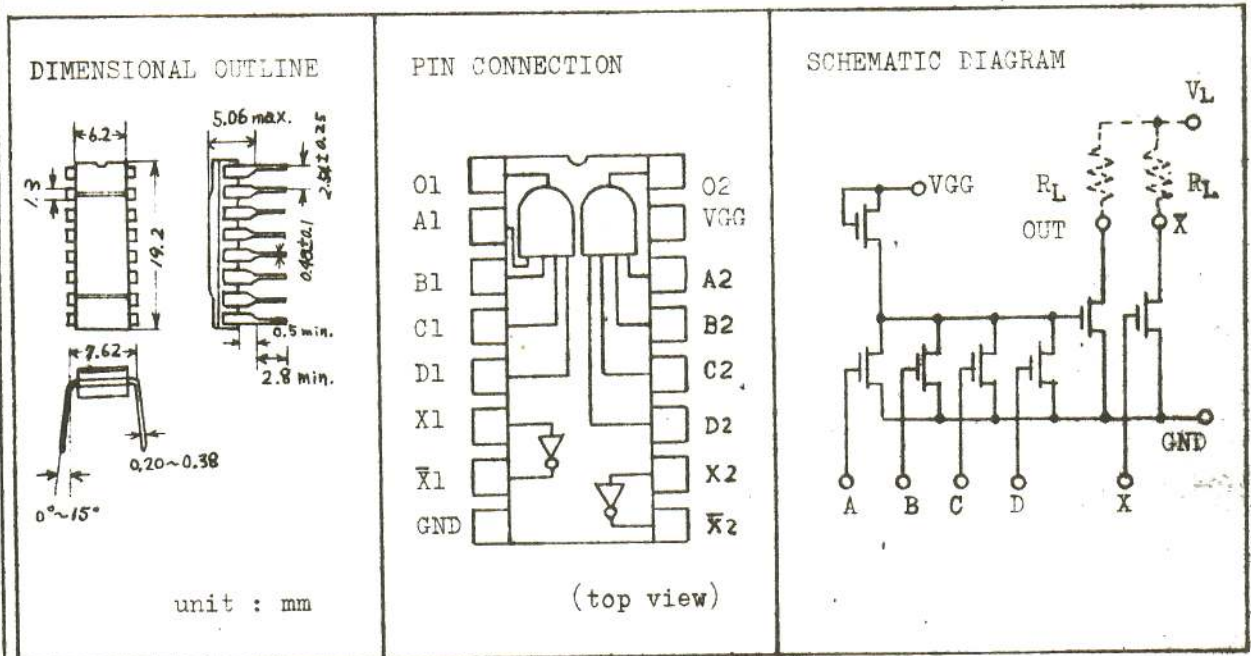
The features of HD3104 are as follows :

Integrated zenerclamp protects gates.

Large noise margin $NM_L = 10.0V$, $NM_H = 2.0V$

Wide operating temperature $-20^{\circ}C$ to $+75^{\circ}C$

* inverter part



ABSOLUTE MAXIMUM RATINGS at $25^{\circ}C$ ambient temperature.

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating temperature	T_{opr}	$-20 \sim 75$	$^{\circ}C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^{\circ}C$

*Inverter part.

grade	NM_L	NM_H
A	10V	1.5V
B	6V	2.0V

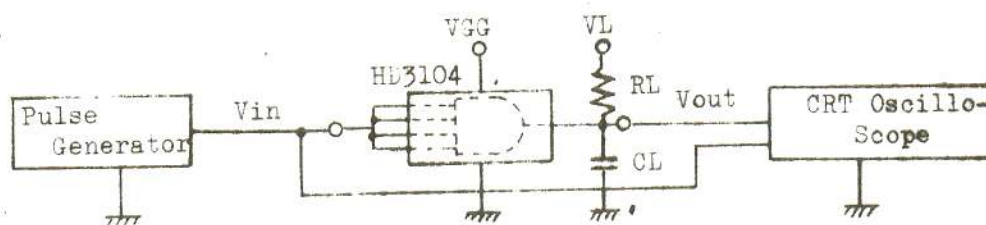
(to be continued)

ELECTRICAL CHARACTERISTICS.

($-V_{GG}=24V \pm 10\%$, $T_a=25^\circ C$, $-V_L=-V_{GG}$).

ITEMS	SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	0 Level -V _{IL}	9.0			V	$T_a=75^\circ C$
	1 Level -V _{IH}			4.0	V	
Output Voltage	0 Level -V _{OLA}	19			V	$R=200K\Omega$, $T_a=75^\circ C$, $-V_{in}=9V$
	1 Level -V _{OHA}			2.0	V	$R=20K\Omega$, $T_a=75^\circ C$, $-V_{in}=4V$ (9V)
	0 Level -V _{OLB}	19 (15)			V	$R=200K\Omega$, $T_a=75^\circ C$, $-V_{in}=9V$ (4V)
Input Resistance	R _{in}	10			M Ω	$-V_{in}=26.4V$
Input Capacitance	gate C _{in1}			5.0	pF	$f=1MHz$, $-V_{in}=0V$
	inverter C _{in2}			8.0	pF	
Output Capacitance	C _{out}			8.0	pF	$f=1MHz$, $-V_{out}=0V$
Power Dissipation	P _d			50	mW	$-V_{GG}=24V$, $-V_{in}=14V$
Propagation falling	t _{PHL}			1.5	us	$-V_{in}=0 \sim 12.6V$, See Fig.1 & 2.
Delay Time rising	t _{PLH}			2.0V	us	
						$R=20K\Omega$, $C=50pF$

*....The value which is shown in parentheses is used at testing an inverter.



CL includes a stray capacitance of a probe and wirings.

Fig. 1. Propagation Delay Testing Circuit.

OUTPUT WAVE FORMS.

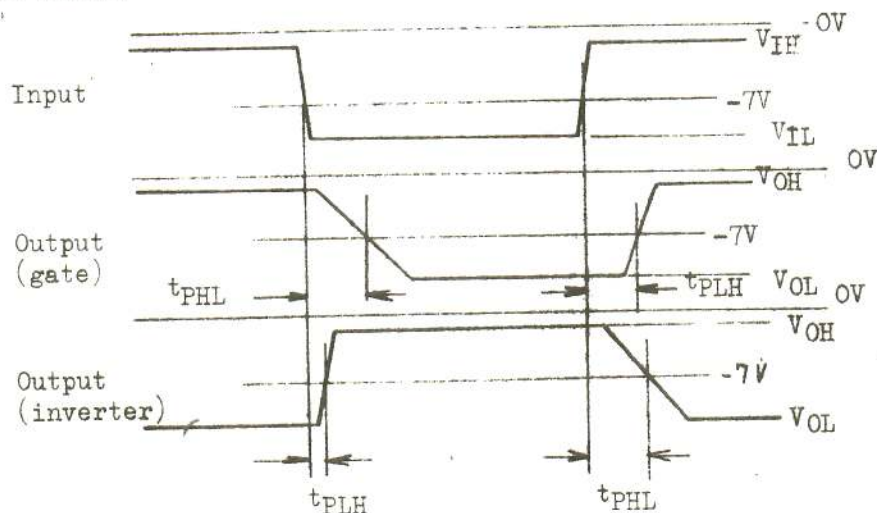


Fig. 2. Definition of a t_{PHL} & a t_{PLH}

*The following value is used at testing an inverter.

grade	-V _{1H}	-V _{OL}		-V _{OH}	
		-V _{in}	min.	-V _{in}	max.
A	3.5V	3.5V	19V	9V	2.0V
B	4.0V	4.0V	15V	9V	2.0V

HITACHI MOS INTEGRATED CIRCUIT HD3106

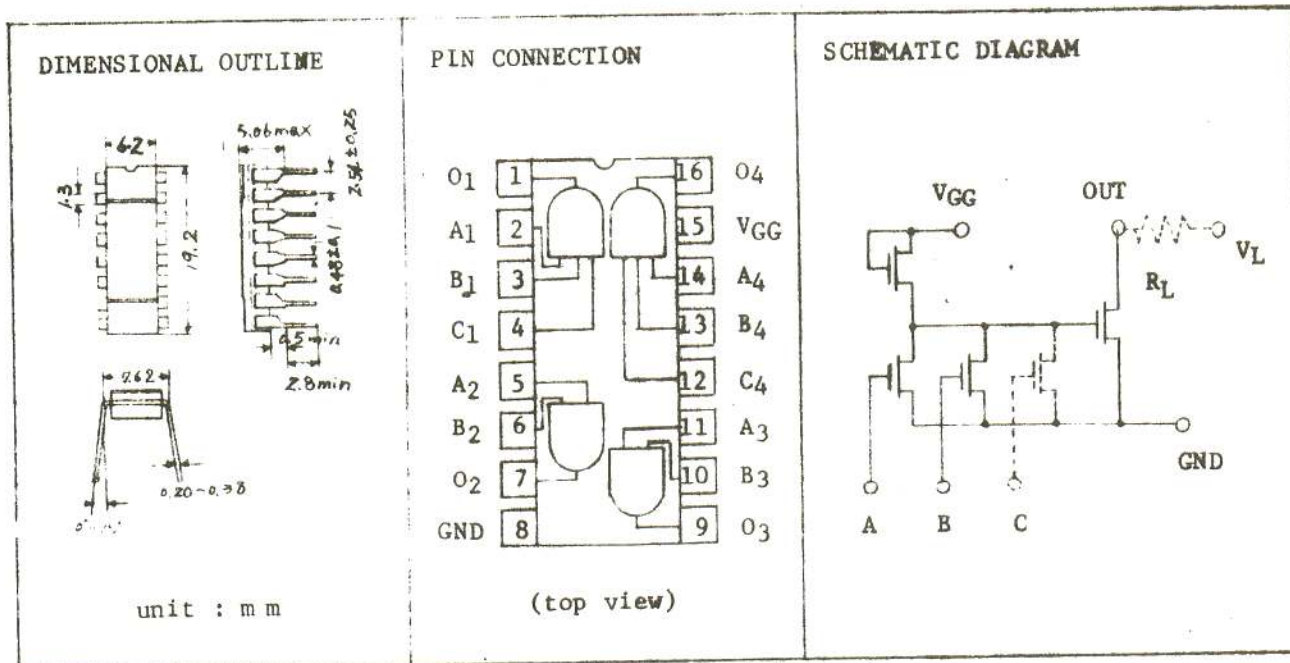
DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3106 is a dual 2 input & a dual 3 input AND gate (positive logic) constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3106 is available in a dual in line type ceramic package (16 leads).

The HD3106 functions as a 2 input AND gate, 3 input AND gate, 2 or 3 input AND-OR gate, and others.

The features of HD3106 are as follows:

- Integrated zener clamp protects gates.
- Large noise margin $NM_L = 10.0V$, $NM_H = 2.0V$
- Wide operating temperature range $-20^{\circ}C$ to $+75^{\circ}C$.



ABSOLUTE MAXIMUM RATINGS at 25°C ambient temperature

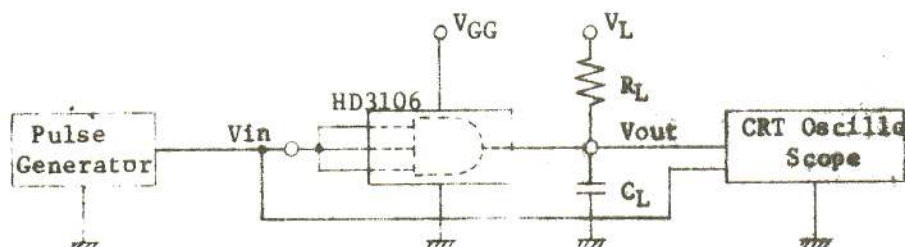
ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating Temperature	T_{opr}	$-20 \sim 75$	$^{\circ}C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^{\circ}C$

(to be continued)

ELECTRICAL CHARACTERISTICS

($-V_{GG}=24V \pm 10\%$, $T_a=25^\circ C$, $-V_L=-V_{GG}$)

ITEMS		SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	"0" Level	$-V_{IL}$	9.0			V	$T_a=75^\circ C$
	"1" Level	$-V_{IH}$			4.0	V	
Output Voltage	"0" Level	$-V_{OL}$	19			V	$R_L=200K\Omega, T_a=75^\circ C, -V_{in}=9.0V$
	"1" Level	$-V_{OH}$			2.0	V	$R_L=20K\Omega, T_a=75^\circ C, -V_{in}=4.0V$
Input Resistance		R_{in}	10			$M\Omega$	$-V_{in}=26.4V$
Input Capacitance		C_{in}			5.0	pF	$-V_{in}=0V, f=1MHz$
Output Capacitance		C_{out}			8.0	pF	$-V_{out}=0V, f=1MHz$
Power Dissipation		P_d			100	mW	$-V_{GG}=24V, -V_{in}=14V$
Propagation Delay Time	falling	t_{PHL}			1.5	μs	$-V_{in}=0 \sim 12.6V$, See Fig.1 & 2. $R_L=20K\Omega, C_L=50pF$
	rising	t_{PLH}			1.5	μs	



* C_L includes a stray capacitance of a probe and wirings.

Fig. 1. Propagation Delay Testing Circuit

OUTPUT WAVE FORMS

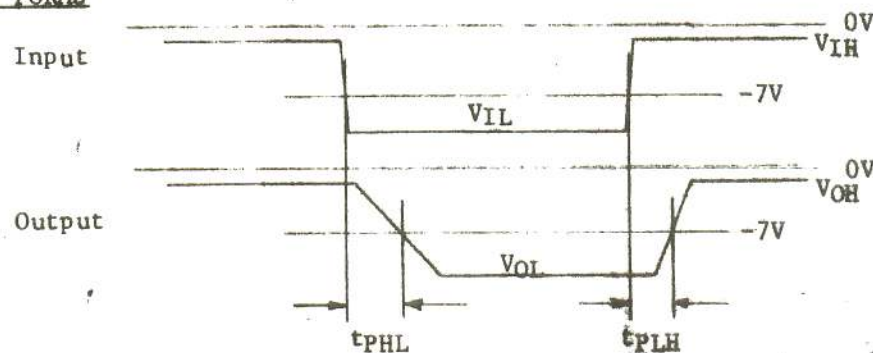


Fig. 2. Definition of a t_{PHL} and a t_{PLH}

HITACHI MOS INTEGRATED CIRCUIT HD3107

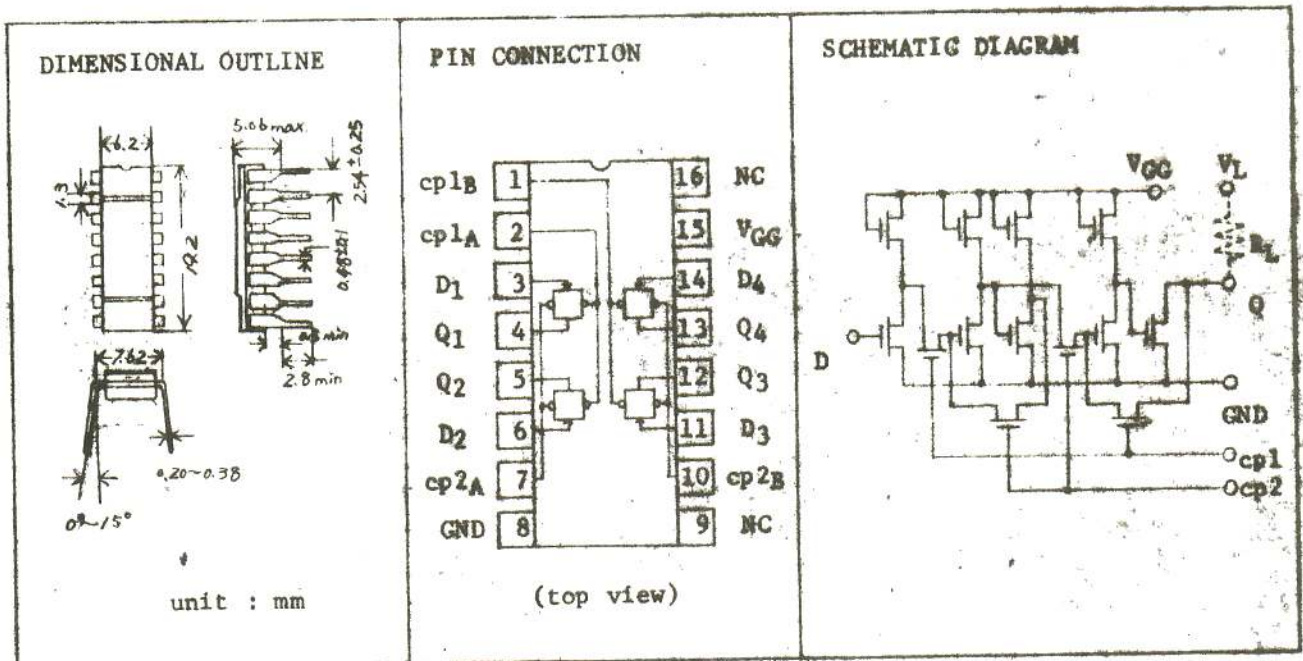
DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3107 is a quadruple quasi-static delayed flip flop constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3107 is available in a dual in line type ceramic package (16 leads).

The HD3107 functions as a 4 bits static D flip flop, a 4 bits parallel in parallel out static shift register, a 4 bits ring counter, and

The features of HD3107 are as follows:

- Integrated zener clamp protects gates.
- Large noise margin $NM_L = 10.0V$, $NM_H = 2.0V$
- Wide operating frequency range DC to 100 kHz.
- Wide operating temperature range $-20^{\circ}C$ to $+75^{\circ}C$.



ABSOLUTE MAXIMUM RATINGS

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating Temperature	T_{opr}	$-20 \sim 75$	$^{\circ}C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^{\circ}C$

(to be continued)

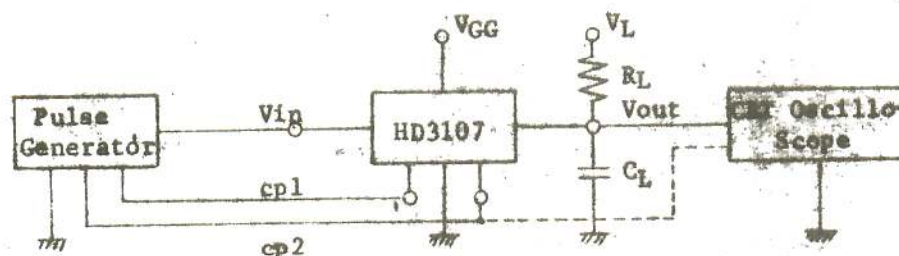
ELECTRICAL CHARACTERISTICS

($-V_{GG} = 24V \pm 10\%$, $T_a = 25^\circ C$, $-V_L = -V_{GG}$).

ITEMS	SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	"0" Level	$-V_{IL}$	9.0		V	$T_a = 75^\circ C$
	"1" Level	$-V_{IH}$		4.0	V	
Output Voltage	"0" Level	$-V_{OL}$	19		V	$R_L = 200K\Omega$ $T_a = 75^\circ C$, $cpw = 1.0\mu s$
	"1" Level	$-V_{OH}$		2.0	V	
Clock Voltage	"0" Level	$-V_{cpl}$	19	26.4	V	$T_a = 75^\circ C$, $cpw = 1\mu s$
	"1" Level	$-V_{cph}$		4.0	V	
Min. Clock Frequency	Clock 1	f_{cp1min}		0	Hz	$f_{cp2} = 5kHz$ $cpw = 1.0\mu s$ $T_a = 75^\circ C$
	Clock 2	f_{cp2min}		0	Hz	
Clock Pulse Width	cpw	1.0			μs	See Fig. 2.
Clock Pulse Delay	cpd	1.0			μs	See Fig. 2.
Clock Capacitance	C_{cp}			8.0	pF	$f = 1MHz$, $V_{cp} = 0V$
Input Resistance	R_{in}	10			$M\Omega$	$-V_{in} = 26.4V$
Input Capacitance	C_{in}			5.0	pF	$-V_{in} = 0V$, $f = 1MHz$
Output Capacitance	C_{out}			8.0	pF	$-V_{out} = 0V$, $f = 1MHz$
Power Dissipation	1	P_{d1}		120	mW	$-V_{in} = 18V$ $-V_{GG} = 24V$,
	2	P_{d2}		40	mW	$-V_{in} = 0V$
Propagation Delay Time	falling	t_{PHL}		1.5	μs	$-V_{in} = 0 \sim 12.6V$, $f_{cp} = 10kHz$, $R_L = 20K\Omega$, $C_L = 20pF$, $cpw = 1\mu s$ See Fig. 1 & 2.
	rising	t_{PLH}		2.0	μs	

NOTE : C_{p1} and C_{p2} are both controllable, and when C_{p1} is controlled, C_{p2} must be given at from 5 kHz to 100kHz repetition rate, and when C_{p2} is controlled, C_{p1} must be given at from 5 kHz to 100kHz repetition rate.

NOTE : P_{d1} and P_{d2} do not contain power dissipation which is consumed at external load resistance (R_L).



* C_L includes a stray capacitance of a probe and wirings.

Fig. 1. Output Voltage and Propagation Delay Testing Circuit

OUTPUT WAVE FORMS

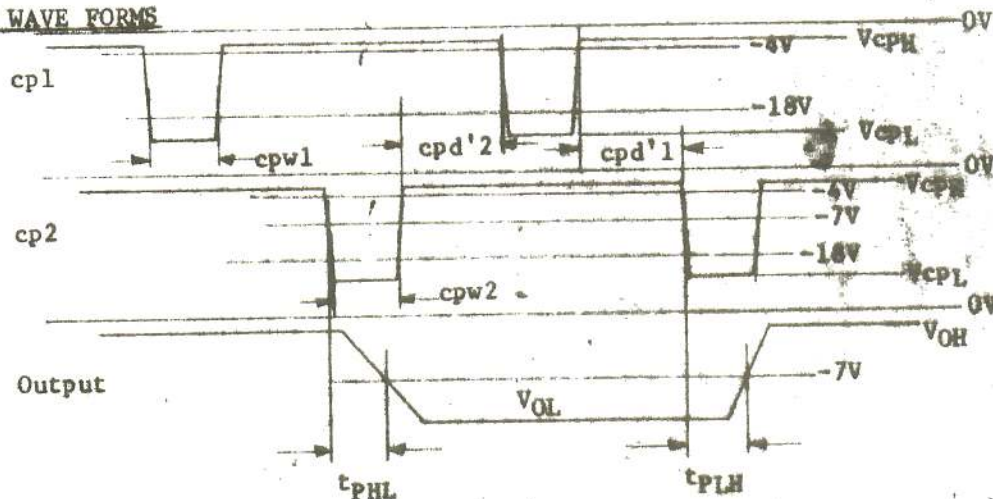


Fig. 2. Clock & Output Wave Forms

(to be continued)

TYPICAL TIMING CHART

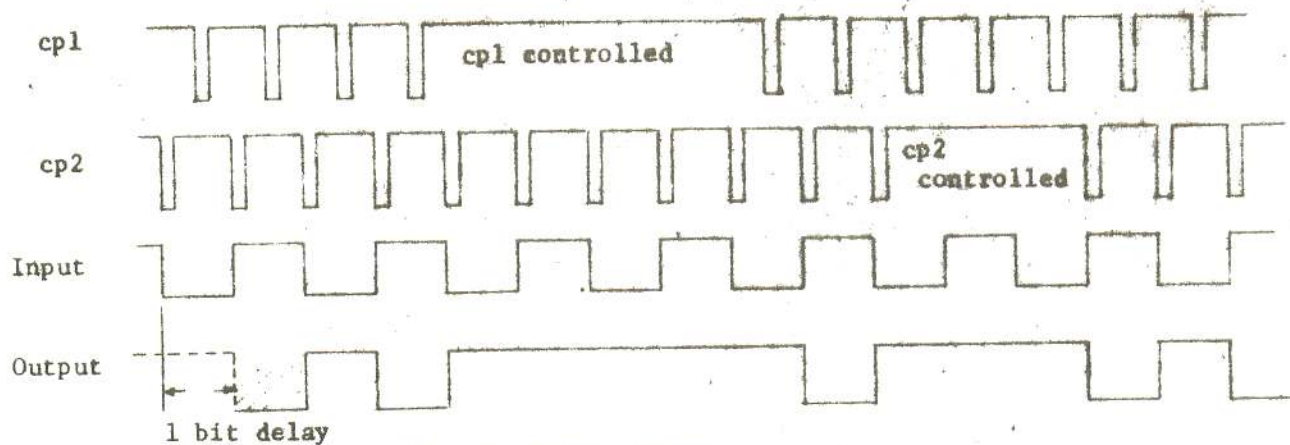


Fig. 3. Timing Chart

CLOCK PULSE GENERATOR BLOCK DIAGRAM

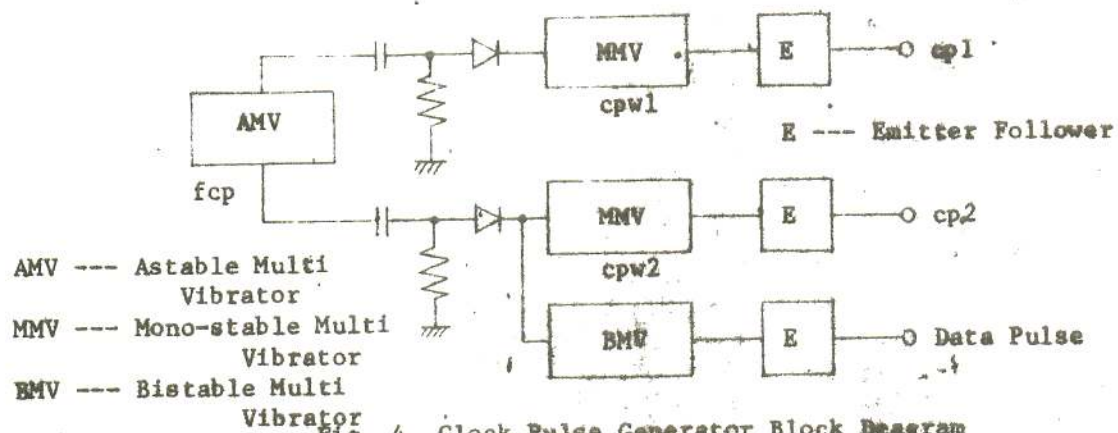


Fig. 4. Clock Pulse Generator Block Diagram

HITACHI MOS INTEGRATED CIRCUIT HD3109

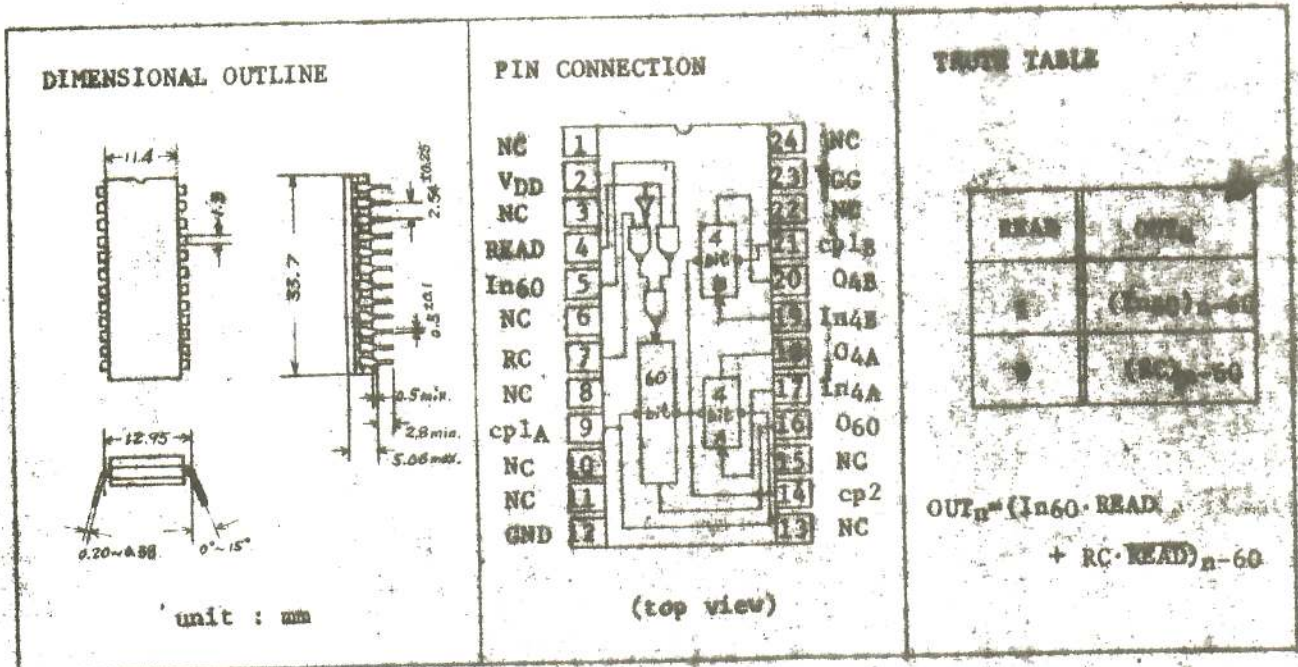
DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3109 is a 60 + 4 + 4 bits dynamic shift register with control gate constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3109 is available in a dual in line type ceramic package (24 leads).

The HD3109 functions as a 4 bits dynamic shift register, a 60 bits dynamic shift register, a 64 bits or 68 bits dynamic shift register, and others.

The features of HD3109 are as follows:

- Integrated zener clamp protects gates.
- Large noise margin $NM_L = 1.0\text{ V}$, $NM_H = 2.0\text{ V}$
- Wide operating frequency range 10kHz to 100 kHz
- Wide operating temperature range -20°C to $+75^\circ\text{C}$



ABSOLUTE MAXIMUM RATINGS at 25°C ambient temperature

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating Temperature	T_{opr}	$-20 \sim 75$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^\circ\text{C}$

(to be continued)

TYPICAL TIMING CHART

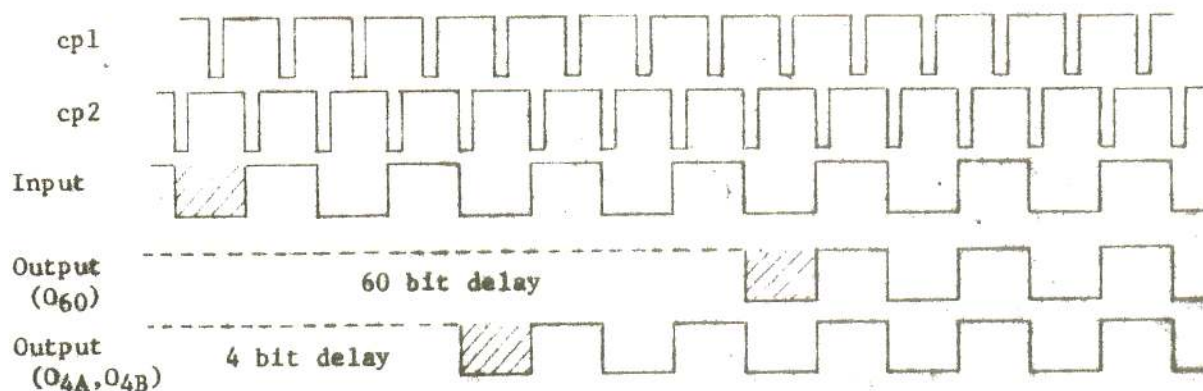


Fig. 3. Timing Chart

CLOCK PULSE GENERATOR BLOCK DIAGRAM

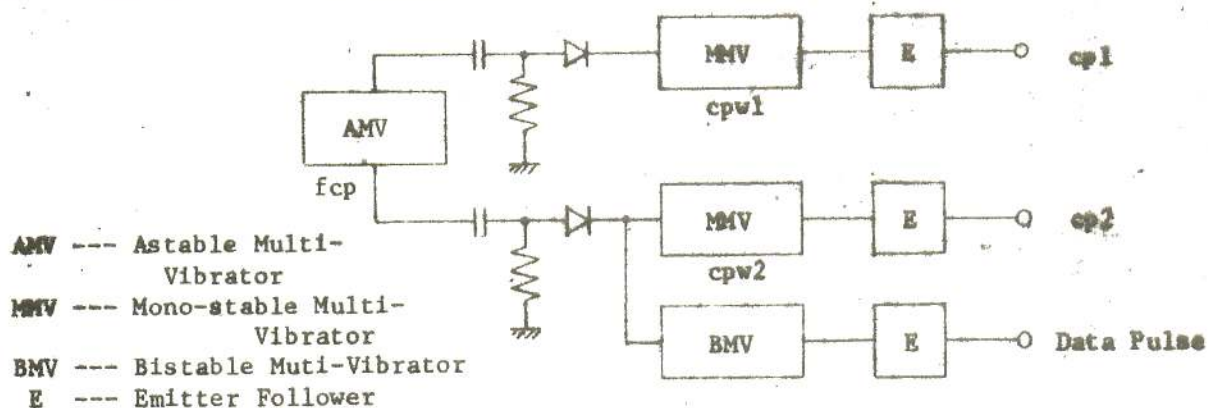


Fig. 4. Clock Pulse Generator Block Diagram

SCHEMATIC DIAGRAM

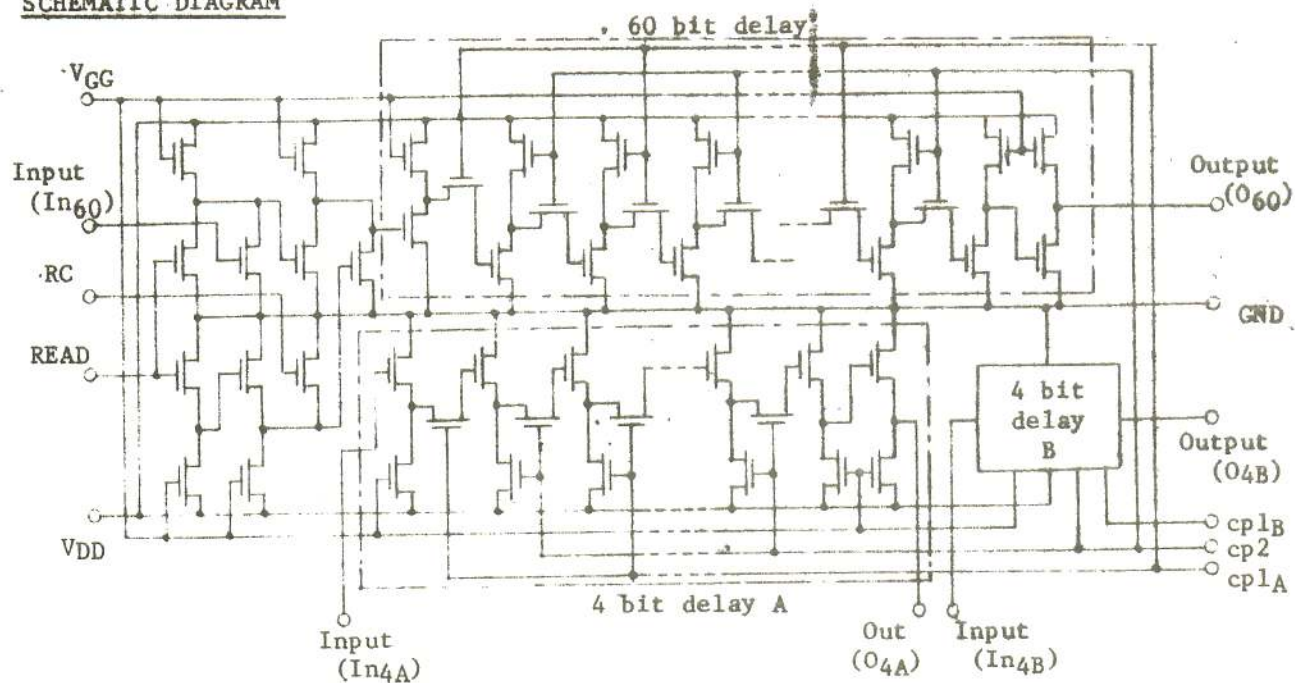


Fig. 5. Schematic Circuit

ELECTRICAL CHARACTERISTICS

($-V_{GG}=24V \pm 10\%$, $-V_{DD}=14V \pm 10\%$, $T_a=25^\circ C$)

ITEMS	SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	"0" Level	$-V_{IL}$	9.0		V	$T_a=75^\circ C$
	"1" Level	$-V_{IH}$		4.0	V	
Output Voltage	"0" Level	$-V_{OL}$	11.0		V	$R_L=100K\Omega$, $T_a=75^\circ C$, $cpw=2.0\mu s$
	"1" Level	$-V_{OH}$		2.0	V	$R_L=50K\Omega$, $f_{cp}=10KHz$
Clock Voltage	"0" Level	$-V_{cPL}$	21.6	26.4	V	$T_a=75^\circ C$, $cpw=2\mu s$
	"1" Level	$-V_{cPH}$		4.0	V	
Min. Clock Frequency	f_{cpmin}			10	KHz	$T_a=75^\circ C$
Clock Pulse Width	cpw	2.0		10	μs	See Fig.2.
Clock Pulse Delay	cpd'	1.0			μs	See Fig.2.
Clock Capacitance	C_{cp}			50	pF	$f=1MHz$, $-V_{cp}=0V$
Input Resistance	R_{in}	10			$M\Omega$	$-V_{in}=26.4V$
Input Capacitance	C_{in}			5.0	pF	$f=1MHz$, $-V_{in}=0V$
Output Capacitance	C_{out}			10	pF	$f=1MHz$, $-V_{out}=0V$
Power dissipation	P_d			70	mW	$-V_{GG}=24V$, $-V_{DD}=14V$, $f_{cp}=10KHz$
Propagation Delay Time	falling	t_{PHL}		4.0	μs	$-V_{in}=0 \sim 12.6V$, $f_{cp}=10KHz$
	rising	t_{PLH}		1.5	μs	$C_L=20pF$, $R_L=\infty$, See Fig.1 & 2.

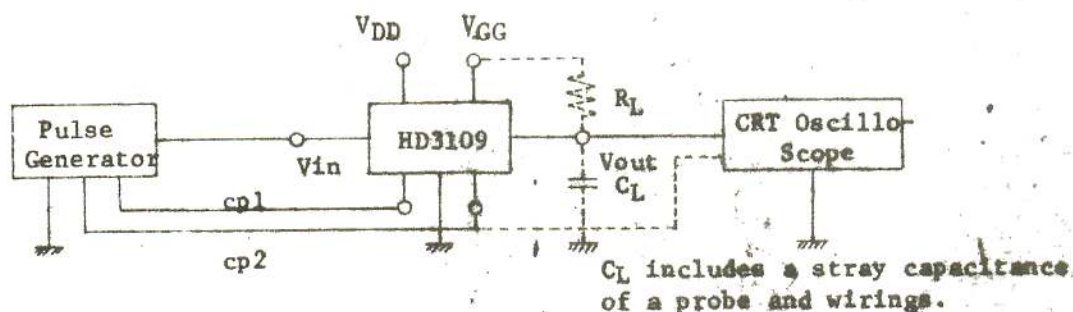


Fig. 1. Output Voltage & Propagation Delay Testing Circuit

OUTPUT WAVE FORMS

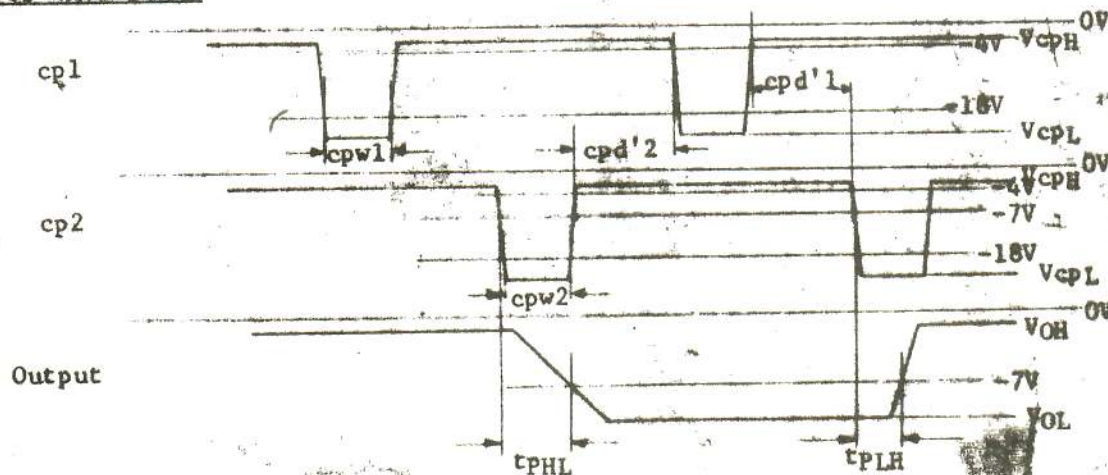


Fig. 2. Clock & Output Wave Forms

(to be continued)

HITACHI MOS INTEGRATED CIRCUIT HD3112

DESCRIPTIONS

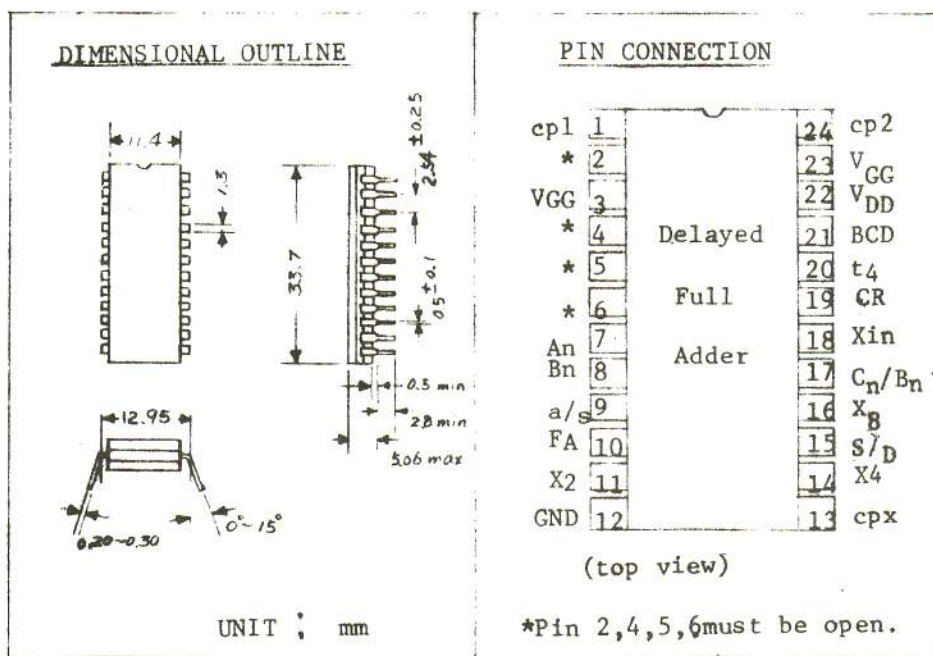
The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3112 is an integrated sub-system on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator.

And HD3112 is available in a dual-in-line type ceramic package (24 leads).

The HD3112 includes about 100 gates and performs the function of series delayed full Adder/ Subtractor.

The features of HD3112 are as follows:

- Integrated zener clamp protects gates, NML $\geq$ 2V, NMH $\geq$ 2V
- Large noise margin.....
- Wide operating frequency range.....DC to 100KHz.
- Wide operating temperature range..... -20°C to +75°C.



ABSOLUTE MAXIMUM RATINGS at 25°C ambient temperature

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	-V _T	-0.3~30	V
Operating Temperature	Topr	-20~75	°C
Storage Temperature	Tstg	-55~150	°C

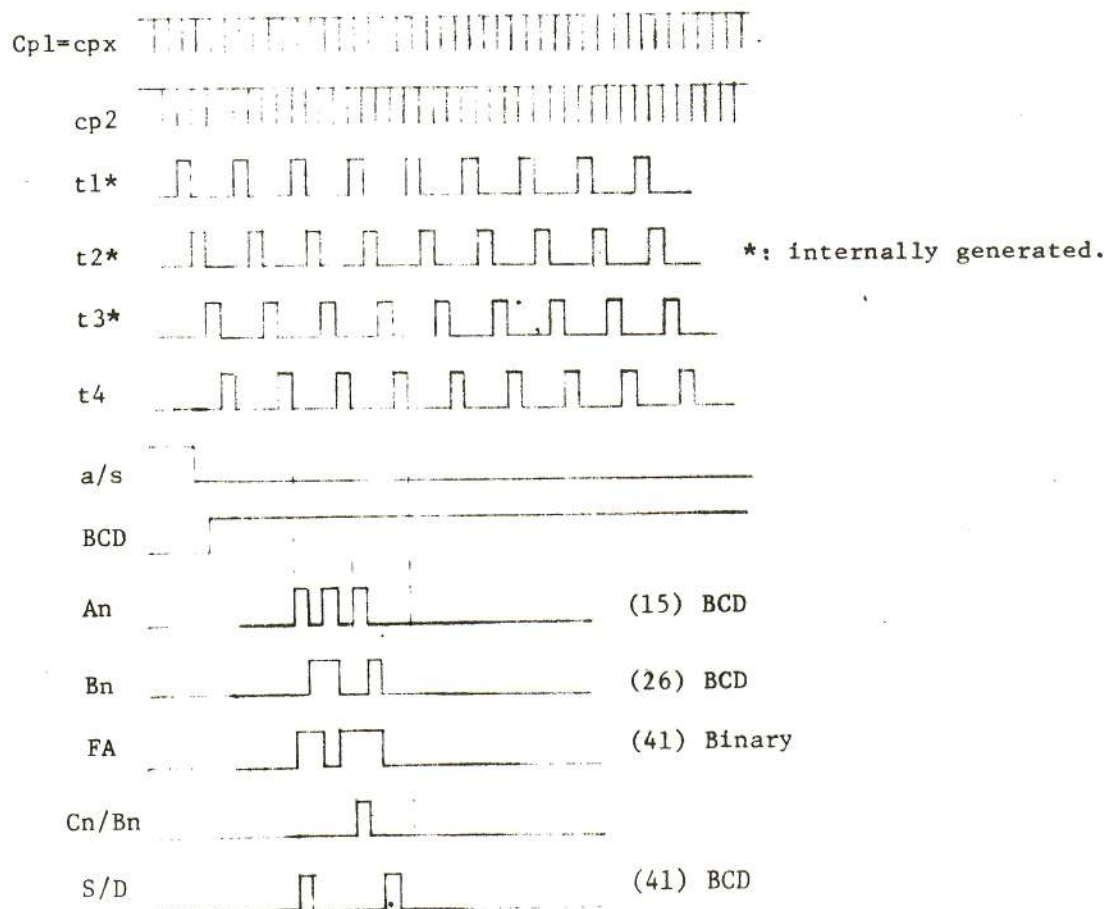
DEFINITION OF SYMBOLS

Input	A _n	BCD or Binary DATA
	B _n	BCD or Binary DATA
	X _{in}	X-Register Input
	C _R	Carry or Borrow Flip-flop Reset
Output	F _A	Sum or Difference (Binary)
	X ₂	X-Register Output 2
	X ₄	X-Register Output 4
	X ₈	X-Register Output 8
	C _n /B _n	Carry or Borrow
Control	S/D	Sum or Difference (BCD)
	a/s	ADD/SUB control
	BCD	Binary/BCD control
	t ₄	Bit Time t ₄
	cp1	clock pulse
	cp2	clock pulse
Power Source	V _{DD}	
	V _{GG}	

a/s	BCD	Function
0	0	Binary Addition
0	1	BCD Addition
1	0	Binary
1	1	BCD Subtraction

TIMING CHART

EXAMPLE : 15+16 in BCD Format.



ELECTRICAL CHARACTERISTICS

($-V_{GG}=24V \pm 10\%$, $-V_{DD}=14V \pm 10\%$, $T_a=25^\circ C$)

ITEMS	SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	0' Level	-V _{IL}	9.0		V	Ta=75°C
	1' Level	-V _{IH}		4.0	V	
Output Voltage	0' Level	-V _{OL}	11		V	RL=100KΩ, Ta=75°C, cpw=2.0μs,
	1' Level	-V _{OH}		2.0	V	RL=30KΩ fcp=10KHz
Clock Voltage	0' Level	-V _{cpL}	19	26.4	V	Ta=75°C, cpw=2μs
	1' Level	-V _{CPH}	0	4.0	V	
Min. Clock Frequency	fcpmin			DC	KHz	Ta=75°C, fcp≥10KHz
Clock Pulse Width	cpw	2.0		10	μs	See Fig.2
Clock Pulse Delay	cpd'	1.0			μs	See Fig.2
Clock Capacitance	Ccp			20	PF	f=1MHz, -Vcp=0V
Input Resistance	Rin	10			MΩ	-Vin=26.4V
Input Capacitance	Cin			10	PF	f=1MHz, -Vin=0V
Output Capacitance	Cout			10	PF	f=1MHz, -Vout=0V
Power Dissipation	Pd			120	mW	cpw=2μs, -VDD=14V, -VGG=24V
Propagation Delay Time	Output except Cn/Bn	tpHL		6.0	μs	Vin=0~12.6V, fcp=10KHz
		tpLH		6.0	μs	
	Cn/Bn	tpHL		7.0	μs	CL=20PF, RL=100KΩ,
		tpLH		7.0	μs	See Fig. 1&2

NOTE: C_{p1} is controllable when c_{p2} is given at from 10KHz to 100KHz repetition rate.

C_{p2} is uncontrollable and always must be given at from 10KHz to 100KHz repetition rate.

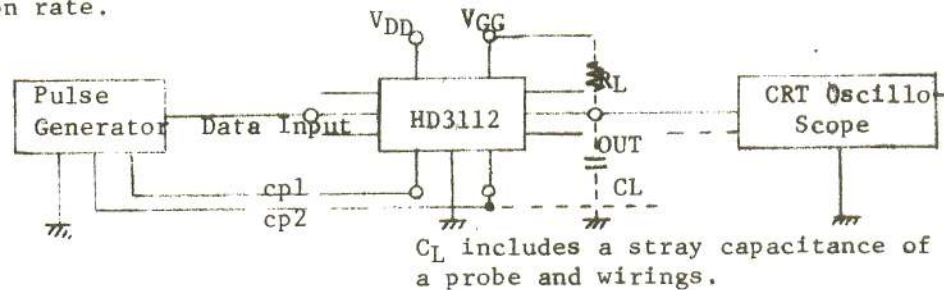


Fig.1. Output Voltage & Propagation Delay Testing Circuit.

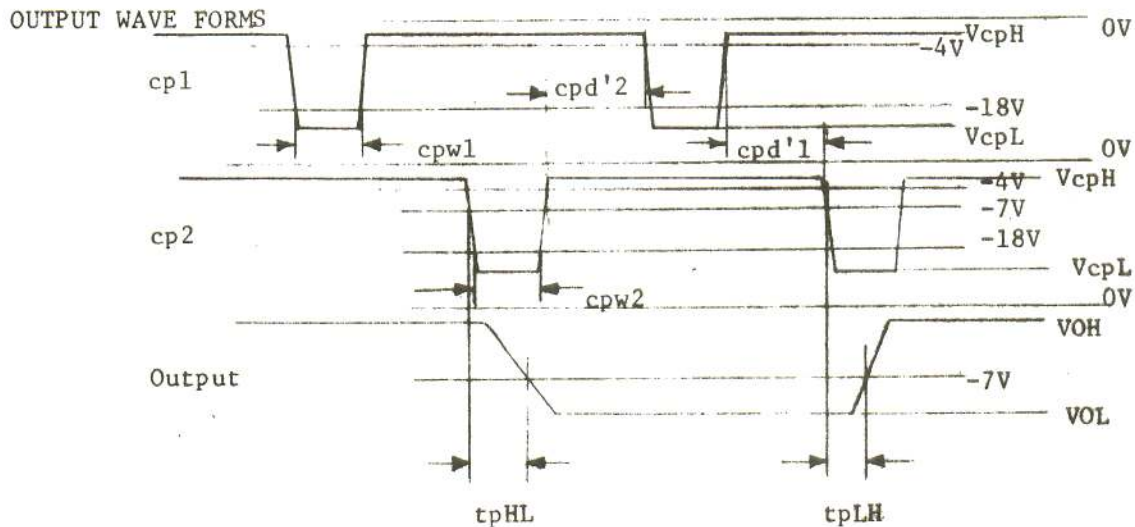


Fig.2. Clock & Output Wave Forms

(to be continued)

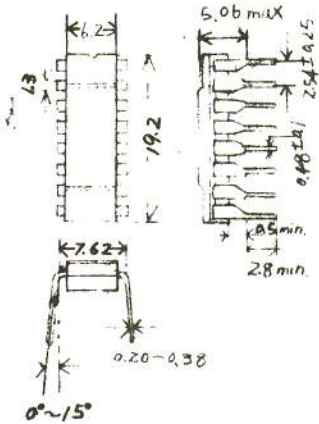
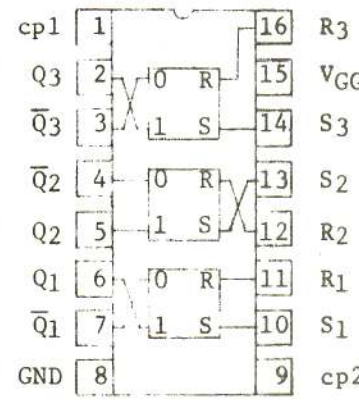
HITACHI MOS INTEGRATED CIRCUIT HD3115

DESCRIPTIONS

The HITACHI MOS (Metal Oxide Semiconductor) Integrated Circuit HD3115 is a triple quasi-static R-S-S flip flop constructed on a silicon monolithic chip utilizing P-channel enhancement mode MOS transistors, belongs to HITACHI MOS IC HD3100 series especially designed for applications in an electronic desk calculator. And HD3115 is available in a dual in line type ceramic package (16 leads).

The HD3115 functions as a R-S-S flip flop, a counter, a memory, and others. The features of HD3115 are as follows:

- Integrated zener clamp protects gates.
- Large noise margin $NM_L = 10.0V$, $NM_H = 2.0 V$
- Wide operating frequency range DC to 100kHz.
- Wide operating temperature range $-20^{\circ}C$ to $+75^{\circ}C$.

DIMENSIONAL OUTLINE	PIN CONNECTION	TRUTH TABLE															
 unit : mm	 (top view)	<table border="1"> <thead> <tr> <th>S_n</th><th>R_n</th><th>Q_{n+1}</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Q_n</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </tbody> </table> $Q_{n+1} = S_n + \bar{R}_n \cdot Q_n$	S_n	R_n	Q_{n+1}	0	0	Q_n	0	1	0	1	0	1	1	1	1
S_n	R_n	Q_{n+1}															
0	0	Q_n															
0	1	0															
1	0	1															
1	1	1															

ABSOLUTE MAXIMUM RATINGS at $25^{\circ}C$ ambient temperature

ITEMS	SYMBOLS	RATINGS	UNITS
Terminal Voltage	$-V_T$	$-0.3 \sim 30$	V
Operating Temperature	T_{opr}	$-20 \sim 75$	$^{\circ}C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^{\circ}C$

(to be continued)

TYPICAL TIMING CHART

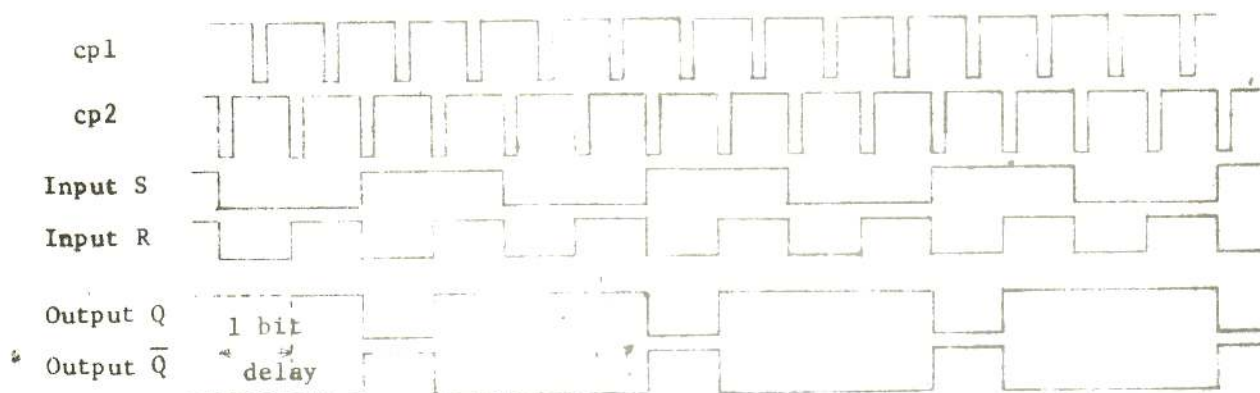


Fig. 3. Timing Chart

CLOCK PULSE GENERATOR BLOCK DIAGRAM

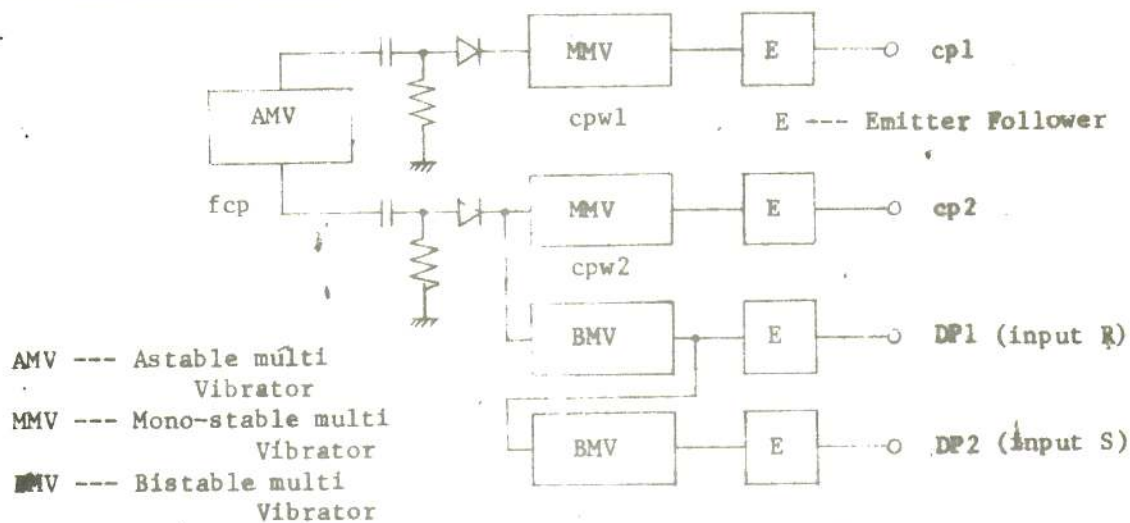


Fig. 4. Clock Pulse Generator Block Diagram

SCHEMATIC DIAGRAM

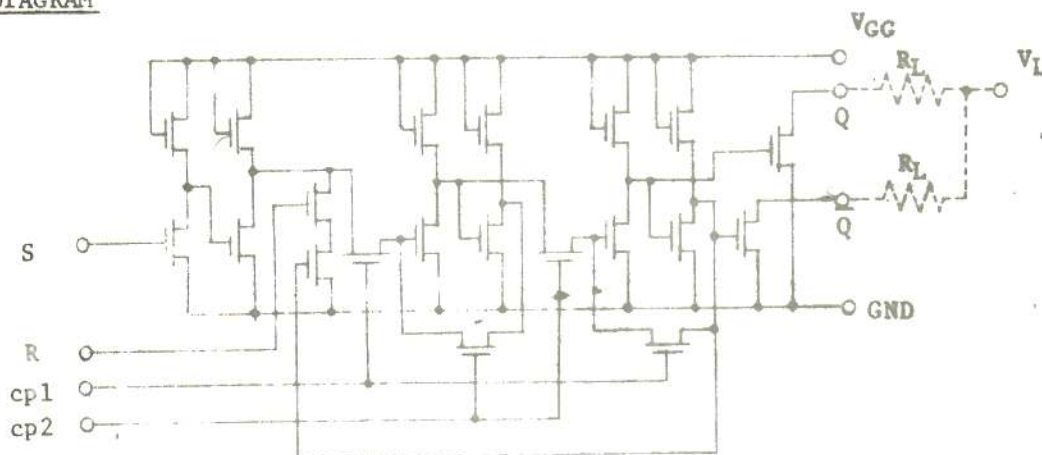


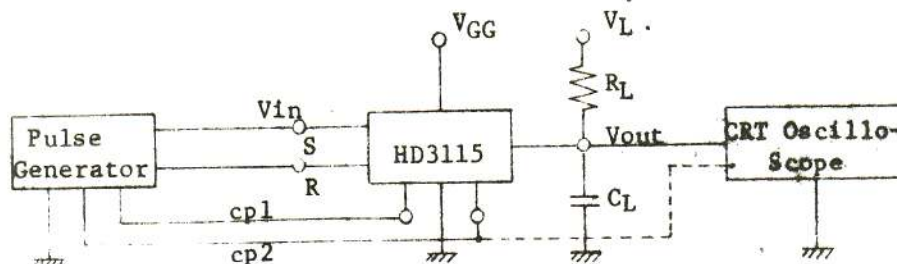
Fig. 5. Schematic Diagram

ELECTRICAL CHARACTERISTICS

($-V_{GG}=24V \pm 10\%$, $T_a=25^\circ C$, $-V_L=-V_{GG}$)

ITEMS	SYMBOLS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Voltage	"0" Level	$-V_{IL}$	9.0		V	$T_a=75^\circ C$
	"1" Level	$-V_{IH}$		4.0	V	
Output Voltage	"0" Level	$-V_{OL}$	19		V	$R_L=200K\Omega$ $T_a=75^\circ C$, $cpw=1.0\mu s$
	"1" Level	$-V_{OH}$		2.0	V	
Clock Voltage	"0" Level	$-V_{cPL}$	19	26.4	V	$T_a=75^\circ C$, $cpw=1\mu s$
	"1" Level	$-V_{cPH}$		4.0	V	
Min. Clock Frequency	Clock 1	f_{cplmin}		0	Hz	$f_{cp2}=5kHz$ $cpw=1.0\mu s$ $T_a=75^\circ C$
	Clock 2	f_{cp2min}		0	Hz	
Clock Pulse Width	cpw	1.0			μs	
Clock Pulse Delay	cpd'	1.0			μs	
Clock Capacitance	C_{cp}			13	pF	$f=1MHz$, $-V_{cp}=0V$
Input Resistance	R_{in}	10			M Ω	$-V_{in}=26.4V$
Input Capacitance	C_{in}			6.0	pF	$f=1MHz$, $-V_{in}=0V$
Output Capacitance	C_{out}			8.0	pF	$f=1MHz$, $-V_{out}=0V$
Power Dissipations	P_d			100	mW	$-V_{GG}=-V_{cp}=24V$, $-V_{in}=14V(S=R)$
Propagation Delay Time	falling	t_{PHL}		2.0	μs	$-V_{in}=0 \sim 12.6V$, $f_{cp}=10kHz$, $R_L=20K\Omega$, $C_L=20pF$, $cpw=1\mu s$
	rising	t_{PLH}		2.0	μs	

NOTE : C_{p1} and C_{p2} are both controllable, and when C_{p1} is controlled, C_{p2} must be given at from 5 kHz to 100kHz repetition rate, and when C_{p2} is controlled, C_{p1} must be given at from 5 kHz to 100kHz repetition rate.



C_L includes a stray capacitance of a probe and wirings.

Fig. 1. Output Voltage and Propagation Delay Testing Circuit

OUTPUT WAVE FORMS

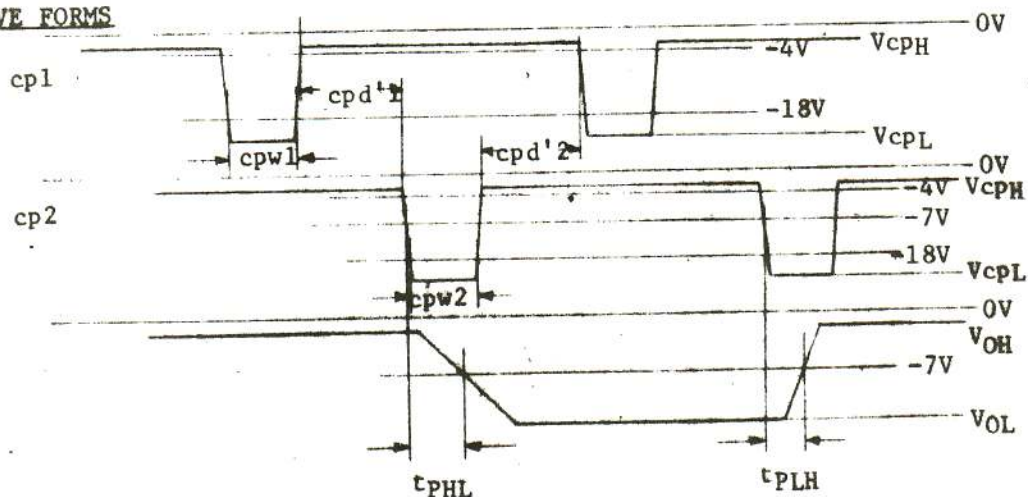


Fig. 2. Clock & Output Wave Forms

(to be continued)