# 1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON DATA I/O



- **Organization 256 Words by 4 Bits**
- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Access Time: 0.65 to 1 μsec Max.**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2112 is a 256 word by 4-bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

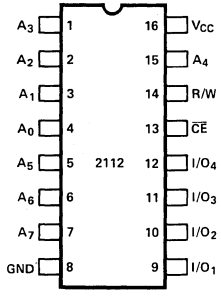
The 2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

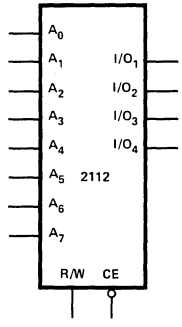
The Intel® 2112 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

## PIN CONFIGURATION



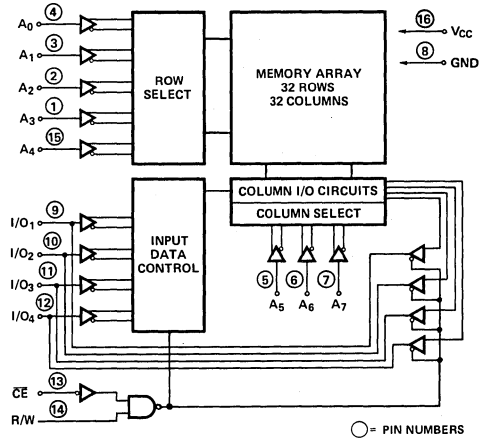

## LOGIC SYMBOL




## PIN NAMES

| | |
|---|---|
| $A_0$-$A_7$ | ADDRESS INPUTS |
| R/W | READ/WRITE INPUT |
| $\overline{CE}$ | CHIP ENABLE INPUT |
| $I/O_1$-$I/O_4$ | DATA INPUT/OUTPUT |
| $V_{CC}$ | POWER (+5V) |

## BLOCK DIAGRAM



## Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70° C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. and Operating Characteristics for 2112, 2112-2

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5% unless otherwise specified.

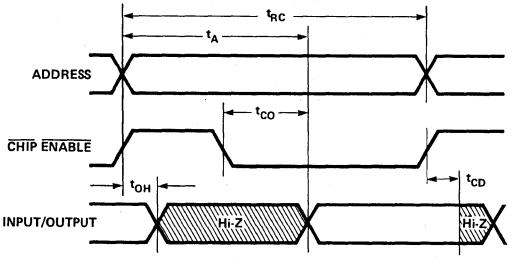
| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Current | | | 10 | µA | $V_{IN}$ = 0 to 5.25V |
| $I_{LOH}$ | I/O Leakage Current | | | 15 | µA | $\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V |
| $I_{LOL}$ | I/O Leakage Current | | | -50 | µA | $\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V |
| $I_{CC1}$ | Power Supply Current | | 30 | 60 | mA | $V_{IN}$ = 5.25V, $I_{I/O}$ = 0mA, $T_A$ = 25°C |
| $I_{CC2}$ | Power Supply Current | | | 70 | mA | $V_{IN}$ = 5.25V, $I_{I/O}$ = 0mA, $T_A$ = 0°C |
| $V_{IL}$ | Input "Low" Voltage | -0.5 | | +0.65 | V | |
| $V_{IH}$ | Input "High" Voltage | 2.2 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output "Low" Voltage | | | +0.45 | V | $I_{OL}$ = 2mA |
| $V_{OH}$ | Output "High" Voltage | 2.2 | | | V | $I_{OH}$ = -150µA |

## A.C. Characteristics for 2112

**READ CYCLE** $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5% unless otherwise specified.

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle | 1,000 | | | ns | $t_r$, $t_f$ = 20ns |
| $t_A$ | Access Time | | | 1,000 | ns | $V_{IN}$ = +0.65V to +2.2V |
| $t_{CO}$ | Chip Enable To Output Time | | | 800 | ns | Timing Reference = 1.5V |
| $t_{CD}$ | Chip Enable To Output Disable Time | 0 | | 200 | ns | Load = 1 TTL Gate |
| $t_{OH}$ | Previous Read Data Valid After Change of Address | 40 | | | ns | and $C_L$ = 100pF. |

**READ CYCLE WAVEFORMS**




## Capacitance[2] $T_A$ = 25°C, f = 1 MHz

| Symbol | Test | Limits (pF) | |
|---|---|---|---|
| | | Typ.[1] | Max. |
| $C_{IN}$ | Input Capacitance (All Input Pins) $V_{IN}$ = 0V | 4 | 8 |
| $C_{I/O}$ | I/O Capacitance $V_{I/O}$ = 0V | 10 | 15 |

NOTES:
1. Typical values are for $T_A$ = 25° C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

## A.C. Characteristics for 2112 (Continued)

**WRITE CYCLE #1** $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%

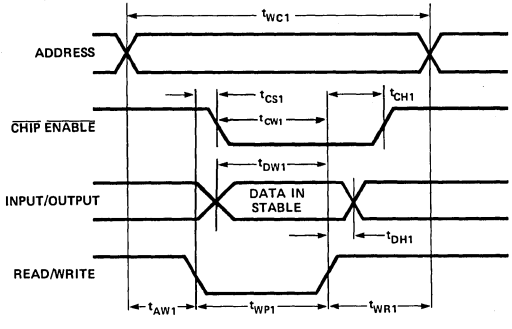
| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{WC1}$ | Write Cycle | 850 | | | ns | $t_r$, $t_f$ = 20ns |
| $t_{AW1}$ | Address To Write Setup Time | 150 | | | ns | $V_{IN}$ = +0.65V to +2.2V |
| $t_{DW1}$ | Write Setup Time | 650 | | | ns | Timing Reference = 1.5V |
| $t_{WP1}$ | Write Pulse Width | 650 | | | ns | Load = 1 TTL Gate |
| $t_{CS1}$ | Chip Enable Setup Time | 0 | | | ns | and $C_L$ = 100pF. |
| $t_{CH1}$ | Chip Enable Hold Time | 0 | | | ns | |
| $t_{WR1}$ | Write Recovery Time | 50 | | | ns | |
| $t_{DH1}$ | Data Hold Time | 100 | | | ns | |
| $t_{CW1}$ | Chip Enable To Write Setup Time | 650 | | | ns | |

**WRITE CYCLE #2** $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%

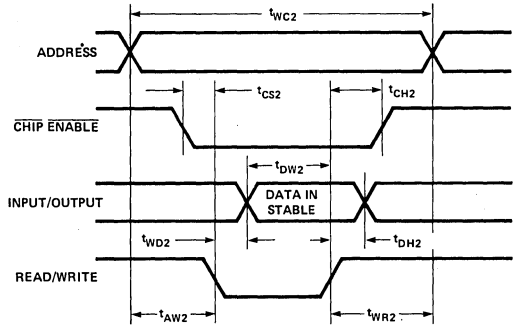
| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{WC2}$ | Write Cycle | 1050 | | | ns | $t_r$, $t_f$ = 20ns |
| $t_{AW2}$ | Address To Write Setup Time | 150 | | | ns | $V_{IN}$ = +0.65V to +2.2V |
| $t_{DW2}$ | Write Setup Time | 650 | | | ns | Timing Reference = 1.5V |
| $t_{WD2}$ | Write To Output Disable Time | 200 | | | ns | Load = 1 TTL Gate |
| $t_{CS2}$ | Chip Enable Setup Time | 0 | | | ns | and $C_L$ = 100pF. |
| $t_{CH2}$ | Chip Enable Hold Time | 0 | | | ns | |
| $t_{WR2}$ | Write Recovery Time | 50 | | | ns | |
| $t_{DH2}$ | Data Hold Time | 100 | | | ns | |

## Write Cycle Waveforms

**WRITE CYCLE #1**




**WRITE CYCLE #2**




NOTE: 1. Typical values are for $T_A$ = 25° C and nominal supply voltage.

# 2112-2 (650 ns Access Time)

## A.C. Characteristics for 2112-2

**READ CYCLE** $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle | 650 | | | ns | $t_r, t_f = 20ns$ |
| $t_A$ | Access Time | | | 650 | ns | $V_{IN} = +0.65V$ to $+2.2V$ |
| $t_{CO}$ | Chip Enable To Output Time | | | 500 | ns | Timing Reference = 1.5V |
| $t_{CD}$ | Chip Enable To Output Disable Time | 0 | | 150 | ns | Load = 1 TTL Gate |
| $t_{OH}$ | Previous Read Data Valid After Change of Address | 40 | | | ns | and $C_L = 100pF$. |

**WRITE CYCLE #1** $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{WC1}$ | Write Cycle | 500 | | | ns | $t_r, t_f = 20ns$ |
| $t_{AW1}$ | Address To Write Setup Time | 100 | | | ns | $V_{IN} = +0.65V$ to $+2.2V$ |
| $t_{DW1}$ | Write Setup Time | 280 | | | ns | Timing Reference = 1.5V |
| $t_{WP1}$ | Write Pulse Width | 350 | | | ns | Load = 1 TTL Gate |
| $t_{CS1}$ | Chip Enable Setup Time | 0 | | | ns | and $C_L = 100pF$. |
| $t_{CH1}$ | Chip Enable Hold Time | 0 | | | ns | |
| $t_{WR1}$ | Write Recovery Time | 50 | | | ns | |
| $t_{DH1}$ | Data Hold Time | 50 | | | ns | |
| $t_{CW1}$ | Chip Enable to Write Setup Time | 350 | | | ns | |

**WRITE CYCLE #2** $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{WC2}$ | Write Cycle | 650 | | | ns | $t_r, t_f = 20ns$ |
| $t_{AW2}$ | Address To Write Setup Time | 100 | | | ns | $V_{IN} = +0.65V$ to $+2.2V$ |
| $t_{DW2}$ | Write Setup Time | 280 | | | ns | Timing Reference = 1.5V |
| $t_{WD2}$ | Write To Output Disable Time | 200 | | | ns | Load = 1 TTL Gate |
| $t_{CS2}$ | Chip Enable Setup Time | 0 | | | ns | and $C_L = 100pF$. |
| $t_{CH2}$ | Chip Enable Hold Time | 0 | | | ns | |
| $t_{WR2}$ | Write Recovery Time | 50 | | | ns | |
| $t_{DH2}$ | Data Hold Time | 50 | | | ns | |

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.