2112A
256 X 4 BIT STATIC RAM

2112A-2	250 ns Max.
2112A	350 ns Max.
2112A-4	450 ns Max.

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

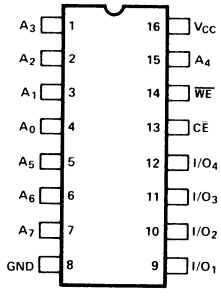
The Intel® 2112A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2112A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

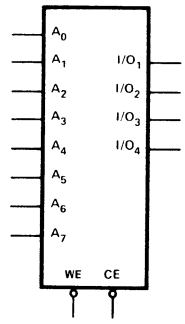
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2112A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



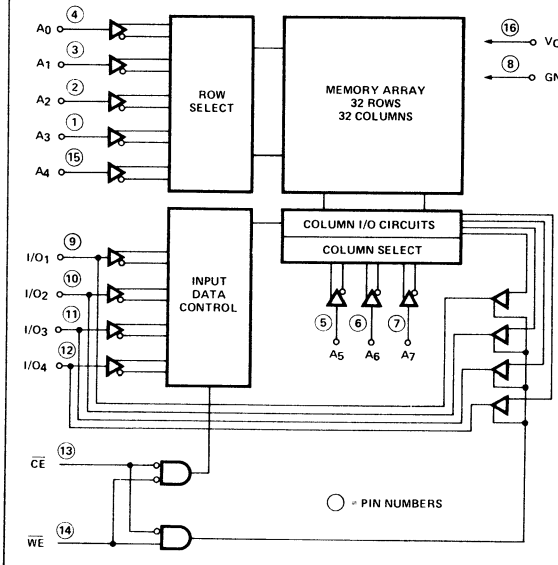
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

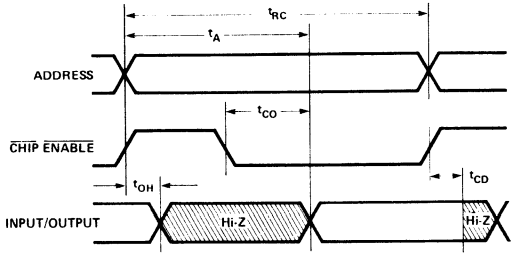
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			1	10	µA	Output Disabled, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current	2112A, 2112A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
		2112A-2		45	65		
I_{CC2}	Power Supply Current	2112A, 2112A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
		2112A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2112A, 2112A-2	2.4			V	I_{OH} = -200µA
		2112A-4	2.4			V	I_{OH} = -150µA

A.C. CHARACTERISTICS FOR 2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output Time			180	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		120	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



CAPACITANCE[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF) Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS FOR 2112A-2 (Continued)

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

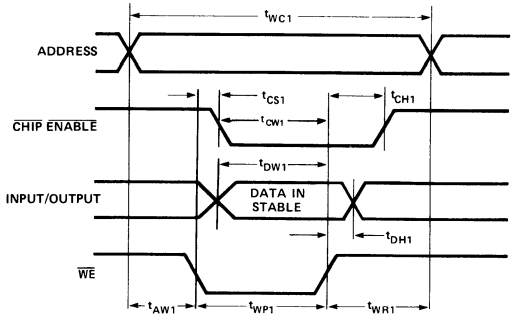
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	200			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	180			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable To Write Setup Time	180			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

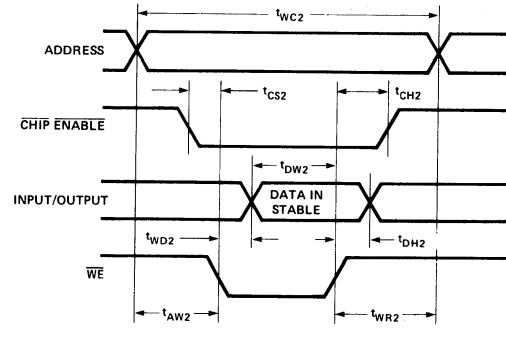
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	120			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

WRITE CYCLE WAVEFORMS

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A-4

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns
t_A	Access Time			450	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			310	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		260	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	300			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	580			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	260			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.