

MONROE 920

PREFACE

This manual is the guide for service after sales with the main purpose of quality performance of products and is also useful for marketing promotion as well as repair service.

It consists of seven sections, i. e. , General; Basic Circuit; Operation Principle; Operation Procedure; How To Repair; Parts Catalog and Service Manual Report.

It is necessary that the operation features and basic circuits of the Monroe 920 should be fully understood in the following sections of General & Basic Circuit, that the principles and the theorem should be also done of Operation Principle and Operation Procedure, and that the proper service should be done by referring to How To Repair and Parts Catalog.

Order repair parts by proper part number from Orange. Part numbers are contained in both the "How To Repair", and "Parts Catalog" sections of this manual.

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HOW TO USE THE SERVICE MANUAL

This manual consists of seven sections, i.e., General; Basic Circuit; Operation Principle; Operation Procedure; How To Repair; Parts Catalog and Service Manual Report.

General

Specifications and operation features are described, and also the manual operations with their precautions are explained details. If this chapter is thoroughly understood, it will be basically in the servicing

Basic Circuit

By using Integrated Circuit, Delay Line, Crystal Oscillator, Nixie Tube and Reed Switch, the electronic circuits are simplified with higher reliability and stability.

It is very important to master these Basic Circuits before understanding Operation Principle and Operation Procedure.

Operation Principle

Principle of operation calculation is classified in addition & subtraction, multiplication, division and square root with detail descriptions concerning about each data, decimal point and sign respectively.

It is necessary to understand the fundamental working operation of these electronic calculations.

Operation Procedure

The actual operation of each calculation is described which is based on Operation Principle, according to Flow Chart and Timing Chart, so that the structural and operational movements can be easily understood.

How To Repair

Operation Check Program; Adjustments; Trouble-Shooting and Wiring Diagrams & Tables necessary for actual repairs and maintenance are explained with important point to localize the faults or defects.

Parts Catalog

Assembly Units are listed in this section and the diagrams should be used in locating the physical defects for repair & maintenance. When parts are ordered, it is important to always to write the complete parts number.

Service Manual Report

Reports of any modifications which should be known by all service personnels and agencies will be issued and forwarded as soon as published.

It is important to keep them, so they should be filed in this section for future reference.

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VII. SERVICE MANUAL REPORT

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GENERAL 1

1. Introduction

Monroe 920 is the most compact type of Monroe series with very simple calculation operations having high reliability and stability.

2. Specifications

2.1 General Specifications

Type: Electronic Desk-top Calculator

Calculation Ability: Addition, Subtraction, Multiplication, Accumulative Multiplication or Division, Constant Multiplication or Division, Square and Powers, Mixed or Applied Calculation.

Indicator: 12 digits

Decimal Point:

Registration: Floating decimal point until it coordinates to the affixed decimal point position.

Result: Fixed decimal point system

Affixed decimal point position: 2, 3 or 4

(The position cannot be changed during calculation.)

Calculation Capacity:

	Operation		Result
Addition or Subtraction:	12 digits	12 digits	12 digits
Multiplication:	12 "	12 "	12 "
Division:	12 "	12 "	12 "

Calculation Time:

Addition or Subtraction: 0.02 sec (max.)

Multiplication: 0.35 sec (max.)

Division: 0.35 sec (max.)

Special Features:

Negative Numeric: When there is negative registration or negative result, a complement numeric is indicated.

Overflow Indicator: When the undermentioned conditions occur, then overflow lamp lights up and all registration stops;

- 1) Registration overflow
- 2) Calculated result overflow

Order Key Correction: When $\boxtimes$ or $\boxplus$ order key has been mistakenly pressed, it can be corrected, if the proper order key is pressed immediately after it.

Key: Reed switch

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Indicator: Nixie tube

Indication system: Dynamic lighting up system

Code: 2'-4-2-1 binary code

Circuit elements: DTL monolithic IC
TTL monolithic IC
Transistors & Diodes

Register Element: Delay line

A register 3 words
B register 1 word

Oscillator: Crystal oscillator 2MHz

Clock Pulse Frequency:
Arithmetic 125 KHz
Delay line 1 MHz

DC Power Supply:

1C:	+5.3V
Read amplifier:	+5.3V, -4.5V
Neon lamp:	+120V
Nixie tube:	+200V

2.2 Ambient Condition

AC allowable voltage fluctuation:	AC voltage, -15% ~ +10%
Ambient temperature:	0 ~ 104° F
Storage temperature:	-40 ~ +158° F
Humidity:	95%
Power:	8W
AC Power:	115, 220 or 240 V

2.3 Physical Features

Dimension:	10.4 (W) x 12.8 (D) x 4.0 (H) in.
Weight:	8.8 lbs

2.4 Keyboard

0 ~ 9	Numeral key:
.	Decimal point key: Affixed decimal point system.
C	Clear key: Clears the indication register, accumulation register and control circuits.
CI	Clear Indicator key: Clears indication register.

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- | | | |
|----------------------------|---------------------|--|
| ☐ X | Multiplication key: | For multiplication |
| ☐ ÷ | Division key: | For division |
| ☐ = | Equal key: | Also used for plus key in addition. |
| ☐ - | Negative equal key: | Also used for entering of negative value in the calculation. |
| ☐ K | Constant key: | Lock key for constant multiplication division. |

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3 Operation**3.1 Special Features****3.1-1 Overflow lamp**

This lamp lights up when a numeral enters the 13th digit position. It can be released by pressing $\boxed{CI}$ or $\boxed{C}$ key.

3.1-2 In multiplication or division, the calculation of 12 digits $\times$ 12 digits can be done and its result is registered in the indicator according to the affixed decimal point position.

3.2 Registration

3.2-1 Entry of registration is freely done until it matches the affixed decimal point position.

Ex. 1-1 4 5 6. 7 8 9 3 with dial at $D\ell = 2$

press	indicator
4	0 0 0 0 0 0 0 0 0 0 0 4.
5	0 0 0 0 0 0 0 0 0 0 0 4 5.
6	0 0 0 0 0 0 0 0 0 0 0 4 5 6.
.	0 0 0 0 0 0 0 0 0 0 0 4 5 6.
7	0 0 0 0 0 0 0 0 0 0 4 5 6. 7
8	0 0 0 0 0 0 0 0 4 5 6. 7 8
Overflow 9	0 0 0 0 0 0 0 4 5 6. 7 8 9
3	0 0 0 0 0 0 0 4 5 6. 7 8 9

Registration stops

Error Correction in Registration

Ex. 1-2 1 2. 4 $\rightarrow$ 1 2 3

press	indicator
$\boxed{C}$	0 0 0 0 0 0 0 0.
$\boxed{1}$	0 0 0 0 0 0 0 1.
$\boxed{2}$	0 0 0 0 0 0 1 2.
$\boxed{3}$	0 0 0 0 0 1 2 3.

In numeral or numeric correction, $\boxed{C}$ or $\boxed{CI}$ key must always be pressed as shown in Ex. 1-2.

3.2-2 Clearing of Indicator

- (1) $\boxed{CI}$ key clears all numerals registered in the indicator.
- (2) After $\boxed{\times}$ or $\boxed{\div}$ key is pressed in multiplication or division and when $\boxed{CI}$ key is pressed before the registration of multiplier or divisor, only numeric are cleared.

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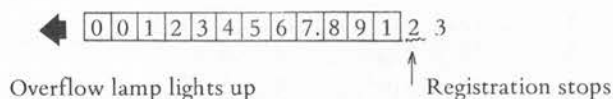
3.2-3 Calculation Overflow

When a numeric is more than 12 digits in the registration cycle, the 13th digit registers with the overflow lamp lighting up and no other digit or digits can be registered.

3.2-4 Decimal point switch and registration

- (1) Decimal point switch always must be set before any calculation is started and cannot be changed during calculation.
- (2) Number of fractional digits of the numeric to be entered must equal to or be less than the affixed decimal point position.
- (3) Decimal point is a floating system until it coordinates to the affixed decimal point position.
- (4) After the decimal point has coordinated, the overflow lamp lights up when the next digit enters in a registration.

Ex. 1-3 1 2 3 4 5 6 7.8 9 1 2 3 (Df= 2)



- (5) However, in the registration of a multiplier or divisor when $\boxed{K}$ key is not locked, the floating system is not concerned to the affixed decimal point position.

3.3 Addition & Subtraction

Ex. 1-4 $a + b + c - d =$

press

$\boxed{C}$	a $\boxed{=}$	a
	b $\boxed{+}$	a+b
	c $\boxed{+}$	a+b+c
	d $\boxed{-}$	a+b+c-d

3.3-1 Negative value

When a negative numeric is registered or there is a negative result, the complement numeric appears in the indicator and it must be converted to its true value by pressing $\boxed{\ominus}$ key.

Ex. 1-5 $-a + b = c$

press

a Floating numerals until numeric coordinates to the affixed decimal position.

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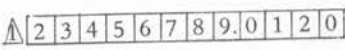
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-  Shifts to the affixed decimal position.
- b Floating numerals until numeric coordinates to the affixed decimal position.
-  Coordinates to the affixed decimal position with the correct answer, but if $-a > b$, the complement answer is indicated.
- $a - (-b) = c$ This equation of calculation also can be done as follows;
press
- a Floating numerals until numeric coordinates to the affixed decimal position.
-  Complement indicated.
- b Floating numerals until numeric coordinates to the affixed decimal position.
-  Complement indicated
-  Converts to true value.

3.3-2 Overflow of Decimal Point Coordination

- (1) In the decimal point coordination cycle, if the number of integral digits of registered numeric is greater than 12 minus the affixed decimal point position, then the overflow lamp lights up.

Ex. 1-6 $Dl = 4$ 1 2 3 4 5 6 7 8 9.0 1 2

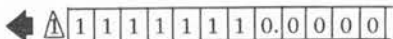
← 

3.3-3 Calculated result enters the 13th digit position.

When the sum of the 12th digit of $a+b$ or $-a-b$ enters the 13th position, then the overflow lamp lights up. Place 1 to the indicated numeric and it will be the correct answer.

Ex. 1-7 $Dl = 4$

	9	8	7	6	5	4	3	2	.	0	0	0	0
+	1	2	3	4	5	6	7	8	.	0	0	0	0

← 

Overflow

3.3-4 Changing Affixed Decimal Point Position During Calculation.

If the affixed decimal point position is changed during calculation, then a mis-calculation will occur.

Ex. 1-8 1. 2 3 (Dℓ = 4) + 1. 2. 3 (Dℓ = 2) mis-calculation

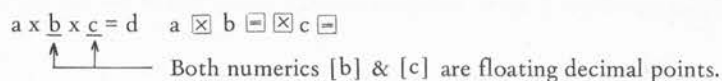
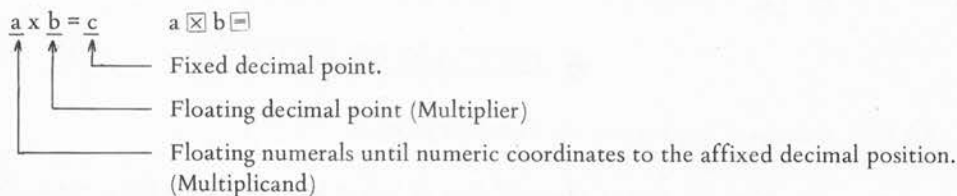
press	indicator												
1. 2 3 (Dℓ = 4)	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td></tr></table>	0	0	0	0	0	0	0	0	0	1	2	3
0	0	0	0	0	0	0	0	0	1	2	3		
$\square$	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	1	2	3	0	0
0	0	0	0	0	0	0	1	2	3	0	0		
1 2. 3 (Dℓ = 2)	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td></tr></table>	0	0	0	0	0	0	0	0	0	1	2	3
0	0	0	0	0	0	0	0	0	1	2	3		
$\square$	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>3</td><td>5</td><td>3</td><td>0</td></tr></table>	0	0	0	0	0	0	0	1	3	5	3	0
0	0	0	0	0	0	0	1	3	5	3	0		

Ex. 1-9 1. 2. 3 (Dℓ = 4) + 1. 2. 3 (Dℓ = 2) mis-calculation

press	indicator												
1. 2. 3 (Dℓ = 4)	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td></tr></table>	0	0	0	0	0	0	0	0	0	1	2	3
0	0	0	0	0	0	0	0	0	1	2	3		
	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	1	2	3	0	0
0	0	0	0	0	0	0	1	2	3	0	0		
1. 2 3 (Dℓ = 2)	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td></tr></table>	0	0	0	0	0	0	0	0	0	1	2	3
0	0	0	0	0	0	0	0	0	1	2	3		
	<table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td><td>3</td><td>1</td><td>2</td><td>3</td></tr></table>	0	0	0	0	0	0	1	2	3	1	2	3
0	0	0	0	0	0	1	2	3	1	2	3		

- (1) When $\square$ or $\square$ key is pressed after the addend or subtrahend was registered, the affixed decimal point position can be changed only to an upper position and then $\square$ or $\square$ key must be pressed again; but it cannot be changed to a lower position, because if the affixed decimal point position is changed to a lower position the indicator clears with overflow lamp lighting up when $\square$ or $\square$ key is pressed again.

3.4 Multiplication



In continuous multiplication, $\times$ & $\square$ key must always be pressed for each calculation and the multipliers have always floating decimal points.

3.4-1 Negative value multiplication

Since the negative value is indicated by its complement, then it must be converted to its true value; so a negative sign must always be added to the result by the operator as follows;

Ex. 1-10 $-2 \times 1.23 = -2.46$ (Dℓ = 4)

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press

indicator

2	0	0	0	0	0	0	0	0	0	0	2.
$\ominus$	9	9	9	9	9	9	8.	0	0	0	0
$\otimes$	9	9	9	9	9	9	8.	0	0	0	0
1 2 3	0	0	0	0	0	0	0	0	1	2	3.
$=$	0	0	0	0	0	0	0.	0	0	1	2

... mis-calculation

Even though, it is a mis-calculation, the overflow lamp does not light up; so the complement can be converted to its true value with the calculation continuing.

Correct operation $-2 \times 123 \rightarrow 2 \otimes 123 = 246$ ($D\ell = 4$)

Ex. 1-11

2	0	0	0	0	0	0	0	0	0	0	2.
$\otimes$	0	0	0	0	0	0	2.	0	0	0	0
1 2 3	0	0	0	0	0	0	0	0	1	2	3.
$=$	0	0	0	0	0	2	4	6.	0	0	0

Answer -246 : Place a negative sign to the result.

Therefore, it is to ignore the negative sign in the operation, but place it to the result.

3.4-2 Multiplication Capacity

This calculator can calculate 12 digits x 12 digits at one time, but the sum of the integrals and fractions totalling 12 digits will be registered in the indicator with all other numerals being eliminated; thus, when multiplying large numbers, the position of the decimal point position ($D\ell$) is very important.

When $D\ell = 0$, the total maximum number of the integral digits of the multiplicand and multiplier can only be 12 or a true result will not be shown, and when $D\ell = 4$, the maximum fractional digits can only total 4 as shown in the following examples:

(1) $D\ell = 0$

a	x	b	=	c
$\downarrow$		$\downarrow$		$\downarrow$
				Total
11 digits	x	1 digit	12 digits	$\rightarrow 9999999999 \times 9 = 89999999991$
6 "		6 "	12 "	$\rightarrow 999999 \times 999999 = 999998000001$
1 "		11 "	12 "	$\rightarrow 9 \times 9999999999 = 89999999991$

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(2) $D\ell = 4$

a	x	b	= c	
↓		↓		
7+4*		1+4*		
		16 digits	Indicator	
			12 digits	* the number of fractional digits.

Ex. 1-9

1 2 3 4 5 6 7. 8 9 8 7 x 9. 9 9 9 9

= 1 2 3 4 5 5 5 5.5 3 0 2 1 0 1 3

cut off

The total digits of the calculation figures are 16, but the upper 12 digits of the result are indicated due to the decimal point coordination with the lower 4 digits being cut off.

(3) Large Numeric Multiplication

When the integral figures of the multiplicand and multiplier are both 12 digits each; first, set the switch at 0, then enter the numerics and calculate. Record the result which is the least significant 12 digits of the correct answer.

Then, set the switch at any position; but, be sure that a decimal point is entered into the multiplicand and multiplier, so that the sum of the integral figures will total to the amount of the difference between the switch set position to 12 and the maximum total digits is 23 digits as follows:

Ex. 1-12 1 2 3 4 5 6 7 8 9 8 7 6 x 9 9 9 9 9 9 9 9 9 9 9 9 9 9
 = 1 2 3 4.5 6 7 8 9 8 7 4 7 6 5 4 3 2 1 0 1 2 4

$$(1) \quad D\ell = 0$$

1 2 3 4 5 6 7 8 9 8 7 6 x 9 9 9 9 9 9 9 9 9 9 9
 = 1 2 3 4 5 6 7 8 9 8 7 | 4 7 6 5 4 3 2 1 0 1 2 4

↙ Overflow and cut off ↗ Overlaps

(2) $D\ell = 4$

$$\begin{array}{ccccccccccccccccc}
 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & .9 & 8 & 7 & 6 & x & 0. & 9 & 9 & 9 & 9 & 9 & 9 & 9 & 9 & 9 \\
 = & \boxed{1} & \boxed{2} & \boxed{3} & \boxed{4} & \boxed{5} & \boxed{6} & \boxed{7} & \boxed{8} & \boxed{9} & \boxed{8} & \boxed{7} & \boxed{4} & & 7 & 6 & 5 & 4 & 3 & 2 & 1 & 0 & 1 & 2 & 4 \\
 & & & & & & & & & & & & \underbrace{}_{\text{Overlaps}} & & & & & & & & & & &
 \end{array}$$

Connect the overlapping numeral for the correct answer, so the method to calculate large numerics is:

- (1) First, set the decimal point switch at 0, so that the lower 12 digits of the calculation will be indicated.

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- (2) Then set the decimal point switch at 4 and place a decimal point in the multiplier (4), so that the upper 12 digits will appear in the indicator. Then connect the overlapping numeral or numerals.

Ex. 1-13 1 2 3 4 5 6 7 8 9 8 7 x 9 9 9 9 9 9 9 9 9 9
 = 1 2 3 4 5 6 7 8 9 8 6 8 7 6 5 4 3 2 1 0 1 3

- (1) $D\ell = 0$

- (2) $D\ell = 4$

3.4-3 Correction of the order key

- 1) In multiplication, if $\oplus$ key was pressed by mistake, it can be corrected by immediately pressing the correct key $\otimes$ as follows:

Ex. 1-14 $a \times b = c$

(Correction method is the same for division.)

Ex. 1-15 $a \times b \times c = d$

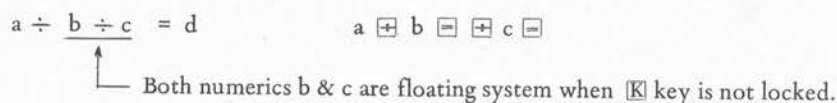
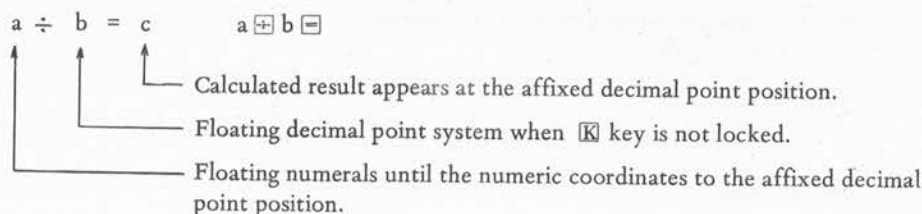
- 2) Clearing registration or order key

- i) $a \text{ [CI]}$ Clears a
- ii) $a \otimes \text{ [CI]}$ Clears a
- iii) $a \otimes b \text{ [CI]}$ Clears only b

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3.5 Divison



In continuous division, [=] key must be pressed every time before a division takes place.

3.5-1 Negative Division

The negative sign principle is exactly the same as in negative multiplication where the operator calculates with both as positive values and then attaches the negative sign to the result, because when negative [-] key is pressed after the numeric, it is instantly converted to its complement, giving an incorrect answer;

Ex. 1-16 $-144 \div 12 = -12$ (Dl=4)

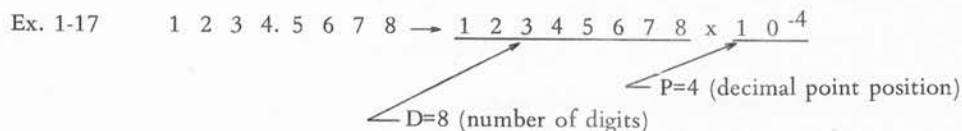
If pressed accordingly to the equation, there will be a wrong answer.

144	0	0	0	0	0	0	0	0	0	1	4	4
[-]	9	9	9	9	9	8	5	6	0	0	0	0
[+]	9	9	9	9	9	8	5	6	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	1	2
[=]	3	3	3	3	3	3	2	1	3	3	3	3

(mis-calculation)

3.5-2 Calculation Capacity

In division calculation, the calculation capacity is decided by the black region of the Vector Chart as follows; for instance,



so the above equation can expressed as follows;

$$N = D \times 10^{-P}$$

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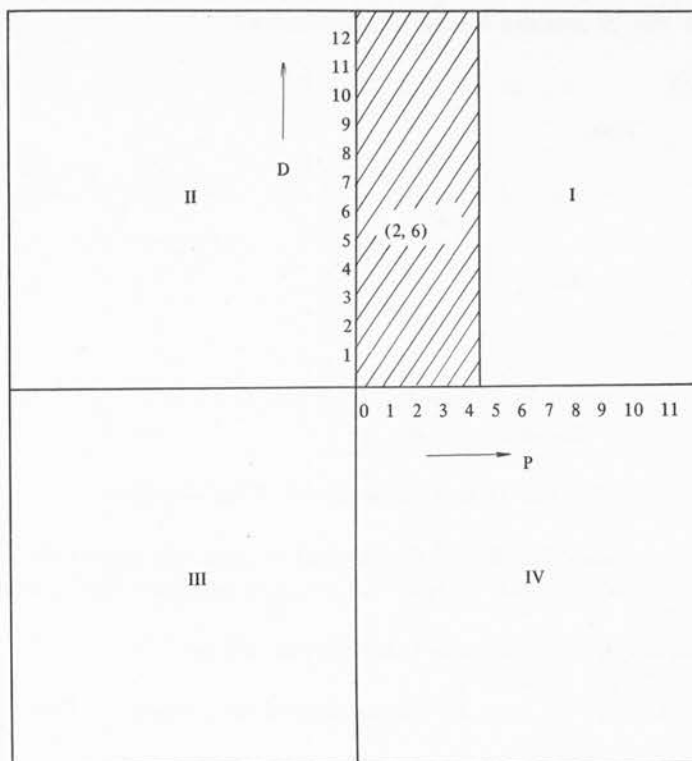
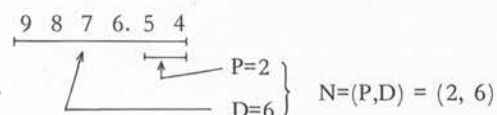


Fig. 1-1 Registration Allowance Region

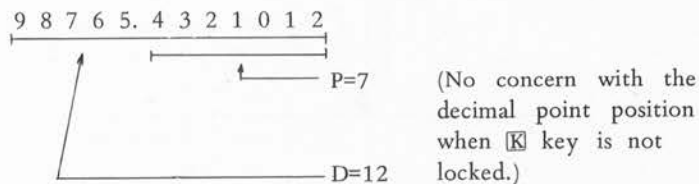
- (a) In registration of dividend, it must be within the black region of the first quadrant

Ex. 1-18



- (b) In registration of divisor, since the decimal point is a floating system when $\boxed{K}$ key is not locked, then it must be within the region of (0, 0), (11, 0), (11, 12) and (0, 12) as shown in Fig. 1-1.

Ex. 1-19



(c) In case of quotient, it is the same as dividend.

Ex. 1-20 $536.1625 \div 234.3$

Thus,

$$\frac{5361625 \times 10^{-4}}{a} \div \frac{2343 \times 10^{-1}}{b} = 22883 \times 10^{-4} \quad (Dl = 4)$$

Therefore,

$$a = (4, 7)$$

$$b = (1, 4)$$

So, calculation capacity is;

$$= (\text{Number of digits of dividend}) - (\text{That of divisor}) + 1$$

When the value of the dividend is larger than that of the divisor, which is the same number of digits from the most significant digit, 1 must be added.

This can be calculated as Vector Calculation as follows:

$$\begin{aligned} 7 - 4 + (1) &= 4 \dots \dots \text{Number of digits of the quotient} \dots D=4 \\ (-4) - (-1) &= -3 \dots \dots \text{Decimal point position of the quotient} \quad P=3 \end{aligned}$$

However, the quotient coordinates to the affixed decimal point position as follows:

$$N = (3, 4) \rightarrow (4, 5) \quad \text{Shifts one digit to the left.}$$

It is shown in following figure.

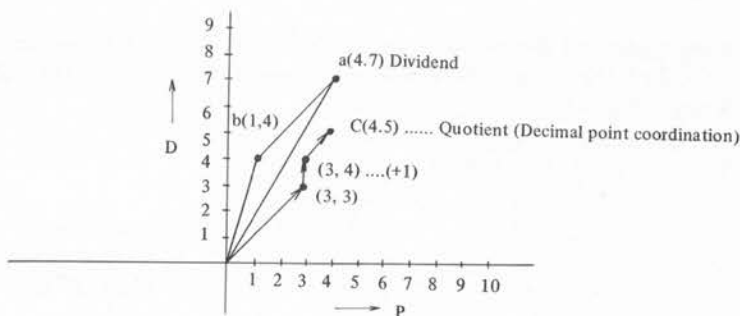


Fig. 1-2 Vector Calculation of Quotient

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Calculation capacity can be obtained as follows;

- I (a) Calculate the simple vector calculation.
- (b) If the value of the dividend is larger than that of divisor which is the comparison of the value of the same number of digits from the most significant digit except 0, then 1 is added to D.
- (c) It shifts to the decimal point position.
- (d) After the operation of (a), (b) & (c), if the result is outside the black region in the first quadrant, then the calculation overflows.

3.5-3 Correction of Order key

This is exactly the same as that of multiplication.

3.6 Constant Multiplication or Division

Simple constant calculation is operated by using $\boxed{K}$ key.

3.6-1 Constant Multiplication

$$\begin{array}{ll} K \times a = & \boxed{K} \text{ lock } K \boxed{\times} a \boxed{=} \\ K \times b = & b \boxed{=} \\ K \times c = & c \boxed{=} \end{array}$$

K: Multiplicand (Constant)

a, b & c: Multiplier

- 1) Multiplicand is the constant
- 2) When there is a negative multiplication, calculate it as a positive value and then the operator should write the minus sign to it.

3.6-2 Constant Division

$$\begin{array}{ll} a \div K = & \boxed{K} \text{ lock } a \boxed{\div} K \boxed{=} \\ b \div K = & b \boxed{=} \\ c \div K = & c \boxed{=} \end{array}$$

K: Divisor (Constant)

a, b & c: Dividend

- 1) Divisor is the constant.
- 2) Negative division calculation is the same as that of multiplication.

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3.6-3 $\boxed{L}$ key

- 1) $\boxed{L}$ key can be locked any time before $\boxed{=}$ or $\boxed{\div}$ key is pressed.
- 2) Ordinary calculation can be done as soon as $\boxed{L}$ key is released.
- 3) Individual addition, subtraction, multiplication or division can be done even though $\boxed{L}$ key is locked.

3.7 Square Calculation

3.7-1 Square Calculation

$$a^2 \rightarrow a \boxed{\times} \boxed{=}$$

- 1) In square calculation, it does not matter whether $\boxed{L}$ key is locked or not.
- 2) "a" can be either an entered numeric or a calculated result indicated in the indicator.

3.7-2 Powers

a^n $\boxed{L}$ key locked

n=2	$\boxed{\times} \boxed{=}$... a^2
n=3	$\boxed{=}$... a^3
n=4	$\boxed{=}$... a^4
n=5	$\boxed{=}$... a^5
⋮	⋮
n=i	$\boxed{=}$ a^i

a^{2^n} $\boxed{L}$ key locked or not

n=1	$\boxed{\times} \boxed{=}$ a^2
n=2	$\boxed{\times} \boxed{=}$ a^4
n=3	⋮ a^8
n=4	⋮ a^{16}
⋮	⋮
n=i	$\boxed{\times} \boxed{=}$ a^{2^i}

a^{-n} $\boxed{L}$ key locked

n=0	$\boxed{+} \boxed{=}$ a^0
n=1	$\boxed{=}$ a^{-1}
n=2	$\boxed{=}$ a^{-2}
n=3	$\boxed{=}$ a^{-3}
⋮	⋮
n=i	$\boxed{=}$ a^{-i}

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3.8 Summary of Overflow

3.8-1 Registration

- 1) When a numeral enters the 13th digit position in registration the lamp lights up and registration stops.
- 2) When the decimal point position of multiplicand or dividend is more than the affixed decimal point position the lamp lights up.

3.8-2 Decimal Point Coordination

When the resultant numeric of the result overflows during the decimal point coordination, the overflow lamp lights up.

3.8-3 Calculation Overflow

- 1) Since the calculated result is a fixed decimal point system, so when it enters into the 13th digit, the lamp lights up and all calculation stops.

3.8-4 Decimal Point Overflow

- 1) In registration of addition, subtraction, multiplicand or dividend, when the decimal point position of the numeric is larger than Dℓ position, the overflow lamp lights up.

3.8-5 Overflow by changing the affixed decimal point position during calculation.

- 1) If the affixed decimal point position is changed to an upper position, then the decimal point coordination can be **done, when any order key is depressed.**
- 2) If the affixed decimal point position is changed to a lower position, then the overflow lamp lights up when any order key is pressed.

3.8-6 Overflow Release

- 1) When  or  key is pressed, then indicator clears with the **overflow lamp being extinguished.**

3.9 Summary of the function key

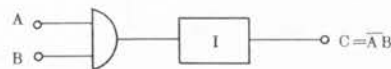
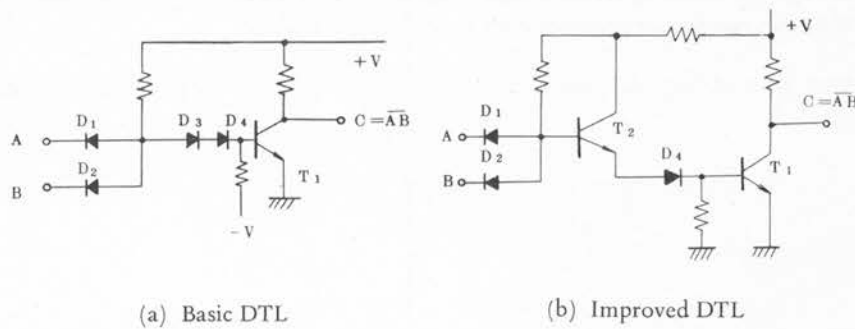
- 1)  or  Clears the indicator or all other circuits.
- 2)  or  For completion of the calculation; but when these keys are pressed again, the calculation will not continue except for power calculation.
- 3)  or  If  and  keys are pressed continuously, then only the latter order key will be in effect.

MONROE 920**BASIC CIRCUITS 1****1. Integrated Circuit****1.1 Types of Integrated Circuit****1.1-1 DTL (Diode Transistor Logic)**

In Fig. 2-1(a), diode D1 & D2 which is the AND gate that makes the transistor T1 operate to invert and amplify the given signals, so the equivalent logic is as shown in Fig. 2-1(c) which is a positive logic. The diode D3 & D4 in Fig. 2-1(a) is the Level Shift Diode which makes the Noise Margin larger by lowering the signal about 0.6V lower by each diode.

The circuit of Fig. 2-1(b) is an improved one to that of 2-1(a), where one level-shift diode is replaced by a transistor which operates not only as level-shift diode but also as an Emitter Follower. The advantages are that a large output is obtained and operates at a higher speed.

Since DTL has a larger Noise Margin and Fan-Out (number of output loads at one time) than that of RTL, so it was adopted in Monroe 950 or 990.



(c) Equivalent Circuit

Fig. 2-1 DTL Circuit

1.1-2 TTL (Transistor Transistor Logic)

Recently TTL is been used in the place of DTL because it has a smaller output impedance and a larger noise margin.

The difference between DTL and TTL is that the diodes are replaced by a transistor with an emitter follower T2 attached to the circuit.

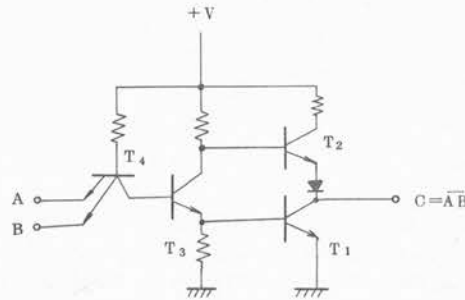


Fig. 2-2 TTL Circuit

1.1-3 MOS (Metal Oxide Semiconductor)

In MOS integrated circuit, FET (Field Effect Transistor) is used which has a large input impedance while epitaxial transistor is used for DTL & TTL.

Though the switching speed in MOS integrated circuit is a little lower than that of DTL & TTL, the noise margin and integration are much larger than them.

Even now, 100-bit shift registers have been developed and are put into practical usage.

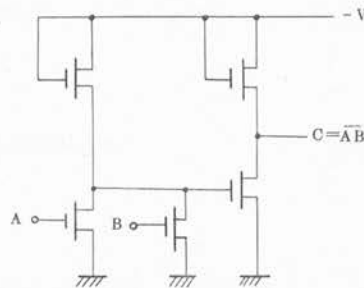


Fig. 2-3 MOS Circuit

1.1-4 Others

Extra-high-speed integrated circuits such as CTL (Complementary Transistor Logic) & CML (Current Mode Logic) which are improved circuits of TTL, have been developed to meet the requirements for extra-high-speed computers.

1.2 DTL Circuits and Its Characteristics

1.2-1 Improved DTL

The improved DTL, mentioned in 1.1-1(b) is adopted in Monroe 990. DTL is divided into two main circuits NAND gate and Master-Slave flip-flop. NAND gate is divided into three groups according to the number of input of diode, i.e. 2-input, 3-input and 4-input NAND gates. There are two types of 4-input NAND gate, general NAND gate and Buffer gate which is able to drive heavy loads.

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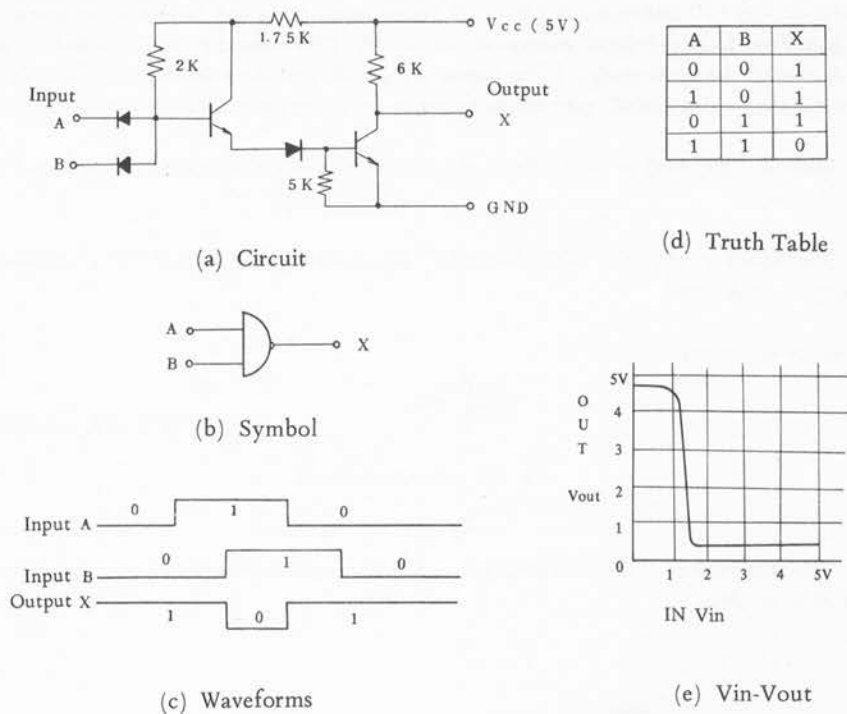


Fig. 2-4 NAND Circuit

Fig. 2-4(a) ~ (e) shows the typical 2-input NAND gate. Generally this integrated circuit is a positive logic circuit as shown in Fig. 2-4(c).

high level (5V) "1"
low level (0V) "0"

Fig. 2-4(a) is the circuit diagram of 2-input NAND gate. Input is given to A and B, and output is emitted from X. Input-output logic $X = \overline{A \cdot B} = \overline{A} + \overline{B}$.

As shown in Fig. 2-4(c) and 2-4(d), output X becomes "0" only when both inputs of A and B are 1", and in all other cases the output is "1". In other words, when either input of A or B is "0", the output X is 1".

As shown in Fig. 2-4(e) when input voltage V_{in} is less than 1.2V with a standard load, the output transistor is OFF and the output voltage V_{out} is nearly V_{cc} (5V). When input voltage is over 1.6V the output transistor is ON and the output voltage is under 0.5V. The holding voltages for the different input and output conditions are:

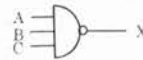
V_{out} "0" = 0.25V max.
 V_{out} "1" = 2.6V min.
 V_{in} "0" = 0.5V max.
 V_{in} "1" = 2.6V min.

Since V_{out} "0" maximum is 0.25V & V_{out} "1" minimum is 2.6V, then V_{in} "0" maximum is 0.5V & V_{in} "1" minimum is 2.6V. So when considering any change in temperature, both V_{in} and V_{out} have a voltage leeway of over 0.5V. This voltage leeway is called Noise Margin and the larger the noise margin is the higher the stability of the calculator will be. The number of outputs from this NAND gate which operates the other gates is called Fan-Out.

Monroe 990, 950 & 920 adopts the NAND gate of Full-Fan-Out (F.O=8) and Half-Fan-Out (F.O=4).

The switching speed of about 20ns (10^{-9} sec) is lower than that of TTL, but it operates at a relatively high speed.

1.2-2 3-Input NAND Gate

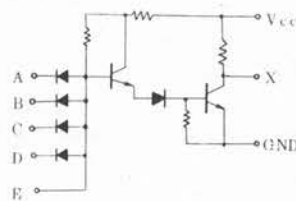


$$X = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

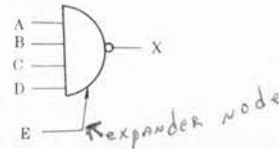
Fig. 2-5 3-Input NAND

The structure of 3-input NAND gate is the same as 2-input NAND gate, except it consists of 3-input diodes.

1.2-3 4-Input NAND Gate



(a) Circuit



(b) Symbol

Fig. 2-6 4-Input NAND

4-input NAND gate consists of 4 input diodes and an expander node to which an expander diode is attached when the inputs are over 4.

1.2-4 Buffer Gate

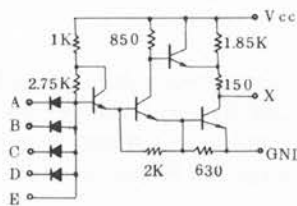


Fig. 2-7 Buffer Gate

The operation of buffer gate without the emitter follower is exactly the same as 4-input NAND gate, but if the emitter follower is attached to it, it drives a heavier load of a Fan-Out of 25.

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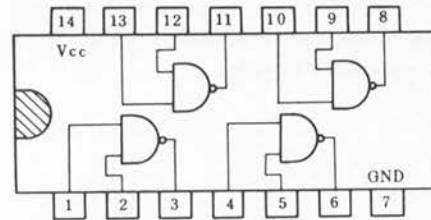
1.2-5 Integrated Circuit

a) Quadruple 2-Input Gate

SN3925 (F.O=4)

SN4554 (F.O=8)

SN7400 TTL



b) Triple 3-Input Gate

SN3931 (F.O=4)

SN4556 (F.O=8)

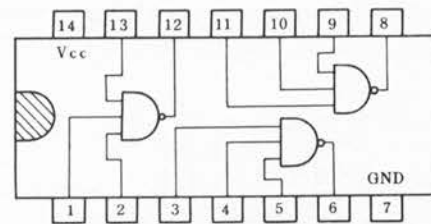


Fig. 2-8 Internal Connection

1.3 Logic of Integrated Circuit

1.3-1 NAND & NOR

All logic are constructed by the NAND gate because the positive logic AND and negative logic OR are the same. Similarly the positive logic NAND and negative logic NOR are the same. The logic of Fig. 2-9(a) is positive logic NAND and Fig. 2-9(b) is the negative logic NOR.

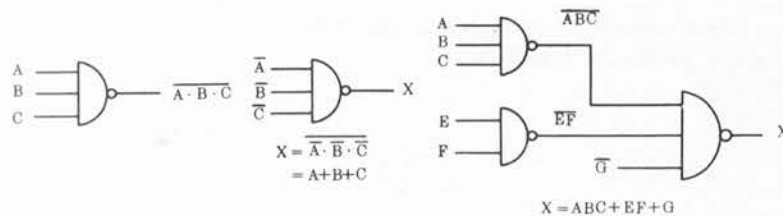


Fig. 2.9(a) NAND

(b) NOR

(c) NAND & NOR

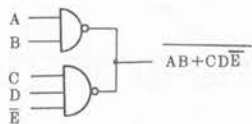
Generally the I.C logic is composed of NAND-NOR as shown in Fig. 2-9(c). The first stage has a function of NAND and the second stage has a function of NOR. In every stage the signal is converted from positive to negative or vice versa. It is important to understand the following Boolean algebra.

$$\overline{AB} = \overline{A} + \overline{B}$$

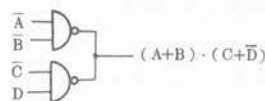
$$\overline{A + B} = \overline{A} \overline{B}$$

1.3-2 Wired OR & AND

In DTL, the outputs of more than two gates are connected and this is called "Wired". Wired OR and wired AND are the same function but their difference is only whether the input is positive or negative.

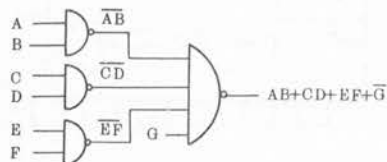


(e) Wired OR

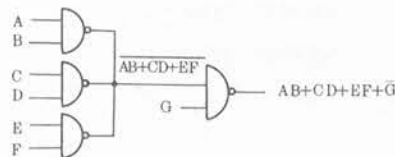


(d) Wired AND

The circuit of 2-9(f) has the same function as 2-9(g) which is the wired OR. However by wiring the outputs of each AND gates together simplifies OR gate which stabilizes the circuit.

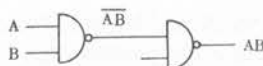


(f) NOR



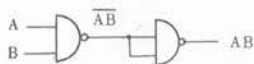
(g) Wired OR

NAND gate is used as an inverter in the circuit by wiring any one terminal of it directly to the output of a gate to convert the signal as shown in Fig. 2-9(h).



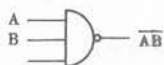
(h) Inverter 1

Even when wired as shown in Fig. 2-9(i), since $A \cdot A = A$ and $\bar{A} \cdot \bar{A} = \bar{A}$, the latter gate of Fig. 2-9(i) functions as an inverter.



(i) Inverter 2

In some cases the input node is not wired since there is no need for it in the circuit as shown in Fig. 2-9(j). Thus, this 3-input gate.

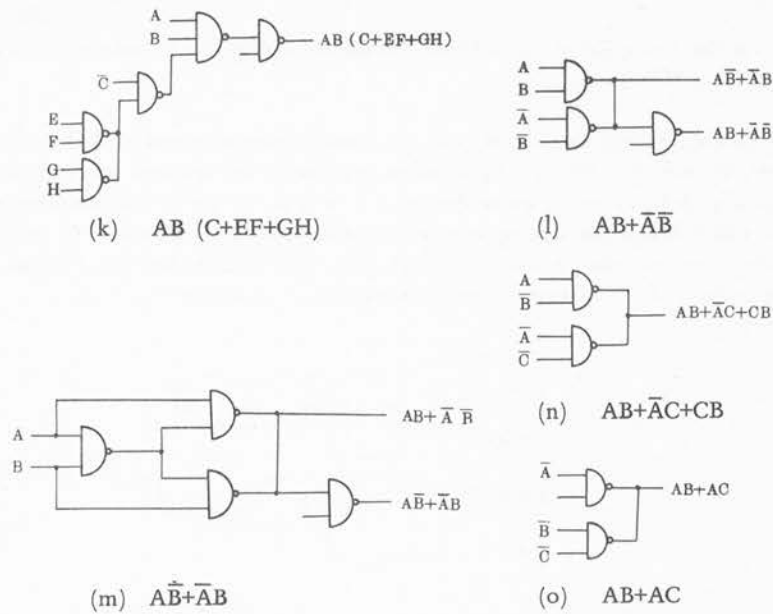


(j) 2-Input Gate

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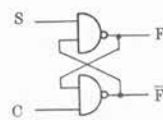
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There are other combinations of NAND & NOR to make other circuits as shown in Fig. 2-9(k) ~ (o).



1.4 Reset-Set Flip-flop Attached Resistors & Condensers

Many R-S.FF attached RC whose circuit is composed of two gates, resistors and condensers are used in the Monroe 990 & 920.

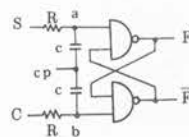


(a) FF

S	C	F
1	1	NC
0	1	1
1	0	0
0	0	UN

(b) Truth Table

1 ... Logical "1"
 0 ... Logical "0"
 NC ... No Change
 UN ... Undetermined



(c) R-S FF Attached RC

	T _n	T _{n+1}
S	C	F _{n+1}
1	1	F _n
0	1	1
1	0	0
0	0	UN

(d) Truth Table

Fig. 2-10 R-S.FF Attached RC

Fig. 2-10(a) is the fundamental diagram. Each output of two NAND gates is connected to the other input node and the flip-flop is only set or reset when the setting signal S is "0" or resetting signal C is "0".

In the Truth Table Fig. 2-10(b), the output of flip-flop is undetermined when both signal S and C are "0".

In Fig. 2-10(c), resistor (R) and condenser (C) are attached to the flip-flop of Fig. 2-10(a) to set or reset the flip-flop by synchronizing with the fall time of clock pulse (CP). Truth Table Fig. 2-10(d) shows when the signal S or C is "0" or "1" synchronizing with the CP fall time which delays the setting or resetting of flip-flop by 1-bit time. In order to stabilize this flip-flop, it is necessary to have the clock pulse (CP) smaller than S or C signal and have the fall time under 50ns. The wave forms of each point are shown in Fig. 2-11.

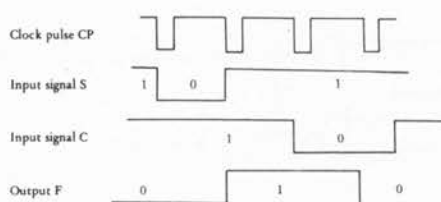


Fig. 2-11 Wave Forms

1.5 Flip-flop (2)

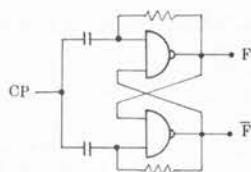
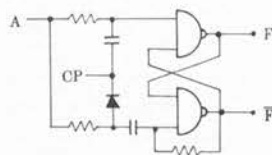


Fig. 2-12 Flip-flop (2)

In Fig. 2-12, the input terminals are controlled by the output signals instead of being controlled by the set or reset signal; so it sets or resets at the fall time of the clock pulses.

1.6 D Type Flip-flop



(a) Circuit

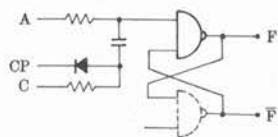
t_n	t_{n+1}	
A	F	$\bar{F}$
1	0	1
0	1	0

(b) Truth Table

Fig. 2-13 D Type Flip-flop

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It sets at the fall time of the clock pulse when A signal is "0" and only resets when F is "0" and A signal is "1", so it can operate by using one input signal which is the set or reset signal. Thus, the output signal changes whenever input signal changes from "0" to "1" or "1" to "0".

1.7 Flip-flop (4)

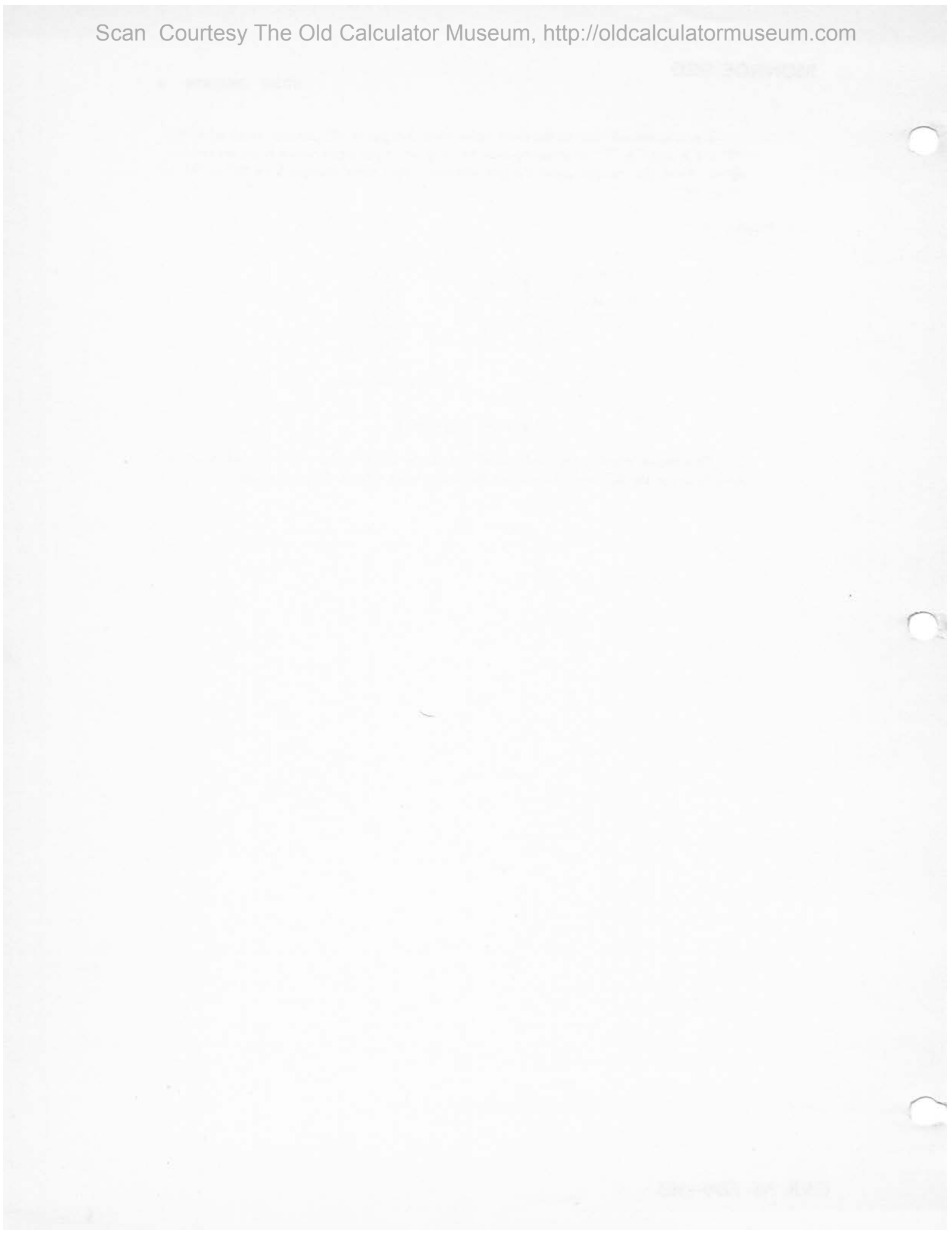
(a) Circuit

t_n		t_{n+1}
A	C	F
0	0	F_n
0	1	1
1	0	F_n
1	1	F_n

(b) Truth Table

Fig. 2-14 Flip-flop (4)

This circuit attaches the condition of $C=1$ to the R-S FF.; therefore, only when $C=1$ & $A=0$, it sets at the fall time of the clock pulse; but when $C=0$, it does not change.



MONROE 920

BASIC CIRCUITS 11

2. Timing Pulse Generators

2.1 Blocks

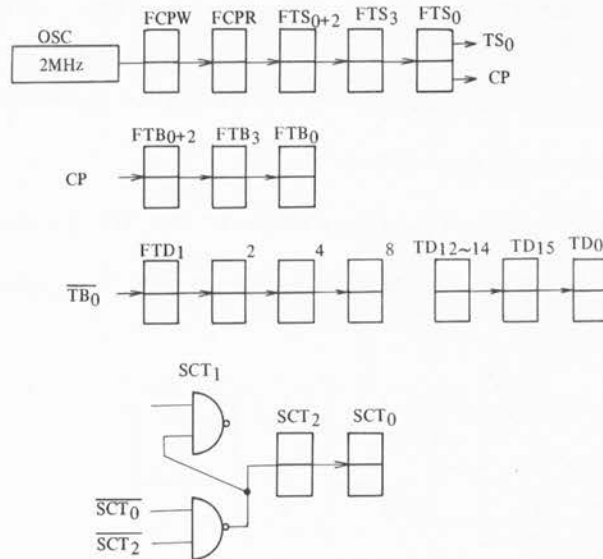


Fig. 2-15 Block Diagrams of Each Signal Generator

2.2 Timing Counters

2.2-1 Bit Counter

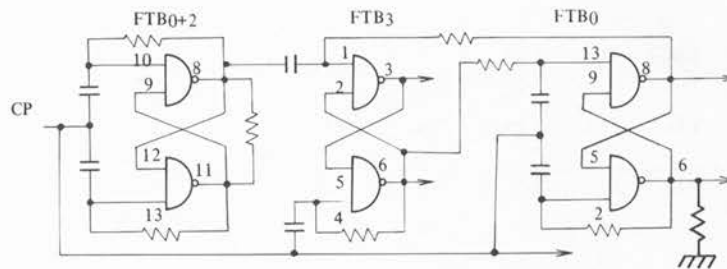


Fig. 2-16 Bit Counter Circuit

TB counter forms the bit pulse and each output has a 1-bit time.

They are formed by a 4:1 counter. Usually these pulse are formed by a feedback counter, but in this method, there are extra small pulses with the bit pulses which may interfere with the other circuit causing an error in the operation, so this bit counter is used as shown in Fig. 2-16 which eliminates these unnecessary pulses.

BASIC CIRCUITS 12

- (1) When all of the output signals of the counter is "0", then $FTB0+2 \cdot 10$ (terminal No.) is "0" by the feedback from 8, so $FTB0+2$ sets at the fall time of $CP1$.
- (2) At this time, $TB0$ & $TB3$ are not effected.
- (3) Since $TB0$ is "0" then $TB3$ is set by $CP2$ at the fall time of $TB0+2$, so $TB3 \cdot 6$ becomes "0" with $TB0$ setting at the $CP3$.
- (4) Since $TB0 \cdot 6$ is "0" and $TB0 \cdot 2$ is also "0", then $TB0$ resets at the fall time of $CP4$.
- (5) Only $TB0+2$ sets at the fall time of $CP \cdot 5$.
- (6) At this time $TB0+2$ resets by $CP4$ and since $TB0$ is "1", then $TB3 \cdot 1$ is not changed.
- (7) $TB0+2$ resets at the fall time of $CP6$ and since $TB0 \cdot 8$ is "0" at this time, then $TB3 \cdot 1$ sets as follows:

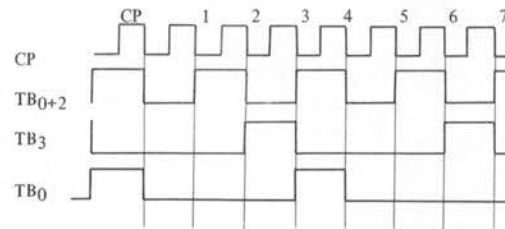


Fig. 2-17 Waveforms of Bit Counter

In this model, 1, 2, 4 & 2' of the 2'421 code of each register are corresponded to the timing of $TB0$, $TB1$, $TB2$ & $TB3$ respectively as follows;

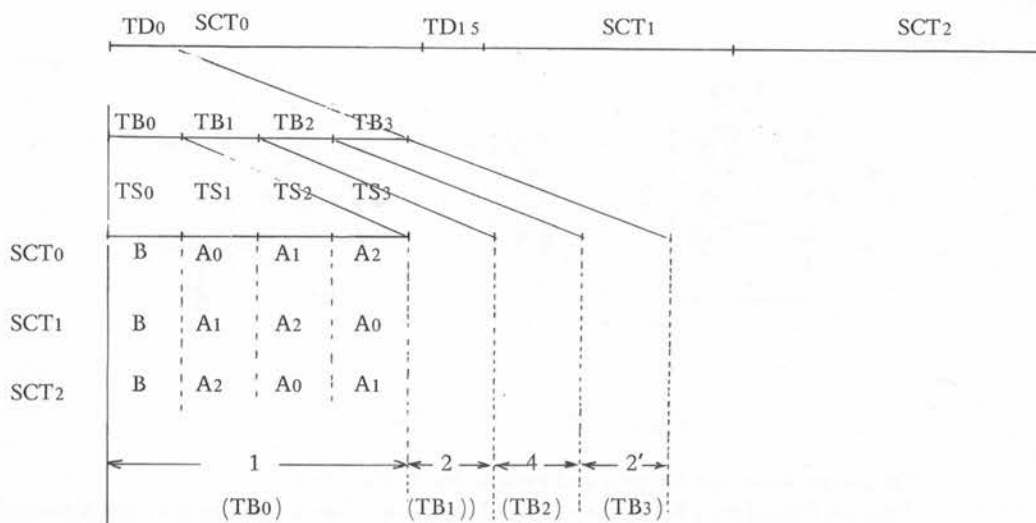


Fig. 2-18 Timing of Each Signal

MONROE 920

BASIC CIRCUITS 13

2.2-2 TS Counter

TS counter circuit is exactly same as that of TB counter and its waveforms are shown below.

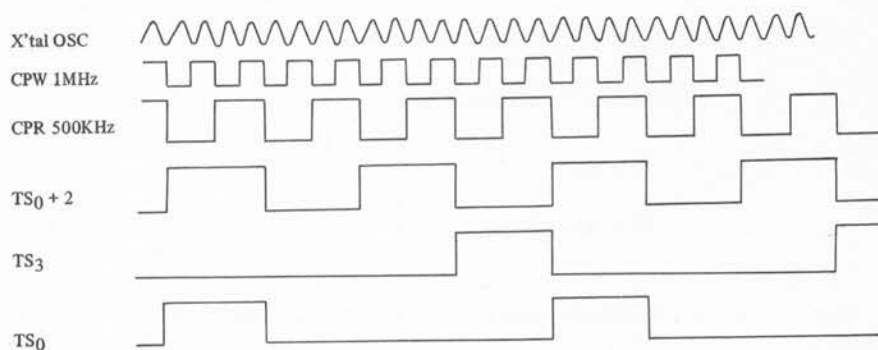


Fig. 2-19 Waveforms of TS Counter

CPW Data is written on the delay line by CPW in $0.4\mu\text{sec}$ which is pulse width of CPW.

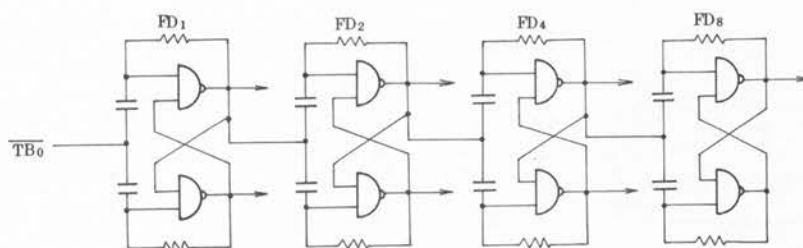
CPR Clock pulse for the delay line.

TS0 Timing when data in B register is written.

TS4 Timing when data in AD4 is written.

CP Clock pulse for arithmetic operation, which is the same as TS0.

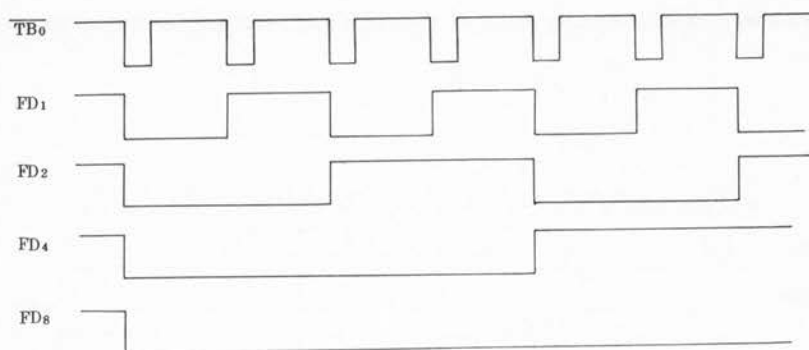
2.2-3 Digit Counter



(a) Digit Counter Circuit

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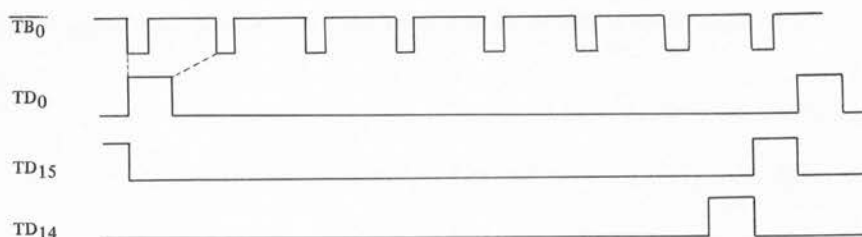
BASIC CIRCUITS 14



(b) Waveforms (1)

Digit counter is the Hexadecimal counter which is also the same as that of the former series.

TD0 ~ TD15 signals are formed by encoding the output signals of this counter.



(c) Waveforms (2)

Fig. 2-20 Digit Counter and its waveforms

2.2-4 Point Counter

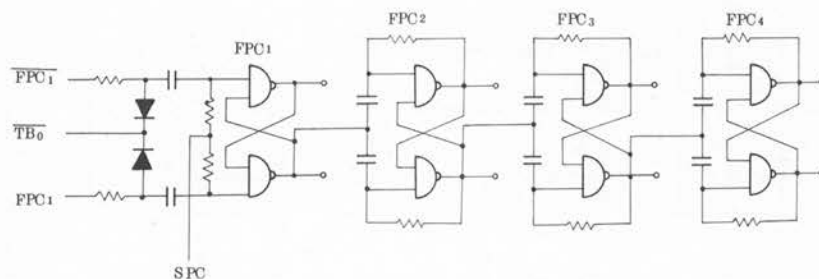


Fig. 2-21 Point Counter Circuit

MONROE 920**BASIC CIRCUITS 15**

Point counter counts one digit shifting at the fall time of TB0 only when SPC signal is "0".

$\overline{PC=D}$ signal is formed by encoding the output signals of FPC1 ~ FPC4.

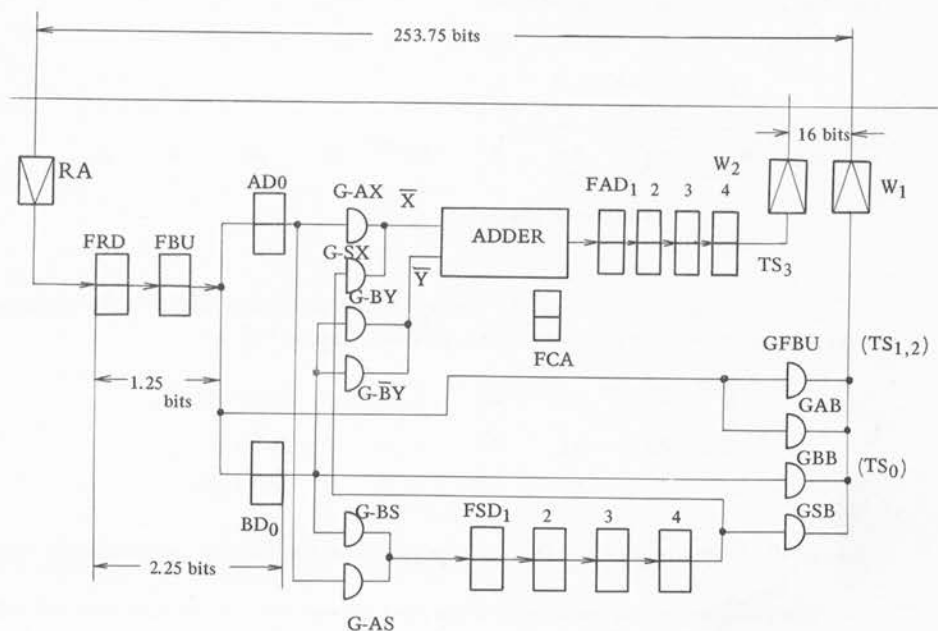
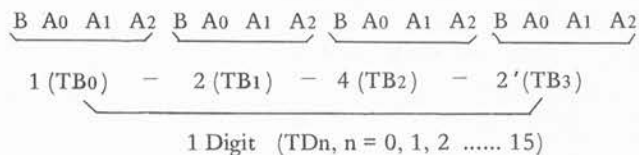
2.3 Delay Line and Circuit

Fig. 2-22 Delay Line Block Diagram

2.3-1 Data Flow

All data is written on the delay line as bit units as follows:

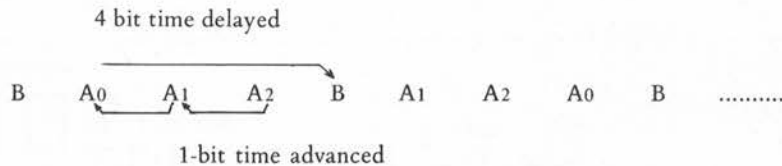


There are 256 bits ($4 \times 4 \times 16$) in the delay line loop, so when data of B register make one complete circulation in the loop of Read amplifier $\rightarrow$ FRD $\rightarrow$ FBU $\rightarrow$ BD0 $\rightarrow$ GBB $\rightarrow$ Write amplifier -1, it passes through 256 bits of this loop.

The next first following data to B register transfers to AD0 and then through AD1, AD2, AD3 & AD4 and is written on the delay line at TS3.

The data of B register in $\overline{\text{FBU}}$ is transferred to BD0 at TS3 and only the next bit (A0 in SCT0) is transferred to AD0 at the timing of CP. Since there are 258 bit time in the loop of Read amplifier $\rightarrow \text{FRD} \rightarrow \text{FBU} \rightarrow \text{AD0} \rightarrow \text{AD4} \rightarrow \text{Write amplifier-2}$; therefore its loop has 2 bit extra time than original loop.

So the data which passes in this loop, is delayed 4-bit time when it circulates for one cycle. All data except B register and the next first following data to B register pass through the loop of Read amplifier $\rightarrow \text{FRD} \rightarrow \text{FBU} \rightarrow \text{GFBU} \rightarrow \text{Write amplifier - 1}$ which has 255 bits, so it is 1-bit less than the original loop; thus these bits are read 1-bit faster than that of original loop when it circulates once in the loop as follows;



Therefore, the sequence or the timing of each A register which is the interchanging of A0 ~ A2 whenever they circulate once through these loop, as follows;

B	A0	A1	A2		SCT0 (1)
B	A1	A2	A0		SCT1 (2)
B	A2	A0	A1		SCT2 (3)

At the timing of SCT0 ~ SCT2, the sequence of the data is respectively (1) ~ (3).

The calculation operation only takes place between B and the next first following data to B; therefore at the timing of SCT0, the calculation operates between B and A0 register.

Transferring and shifting of data is as follows;

B · LSF (Left Shift) : BD0 $\rightarrow$ GBS $\rightarrow$ FSD $\rightarrow$ GSB $\rightarrow$ W1

A · LSF : AD0 $\rightarrow$ G-AS $\rightarrow$ FSD $\rightarrow$ GSX $\rightarrow$ AD $\rightarrow$ W2

B $\rightarrow$ A : BD0 $\rightarrow$ GBY $\rightarrow$ AD $\rightarrow$ W2

A $\rightarrow$ B : FBU $\rightarrow$ GAB $\rightarrow$ W1

2.4 Write Amplifier

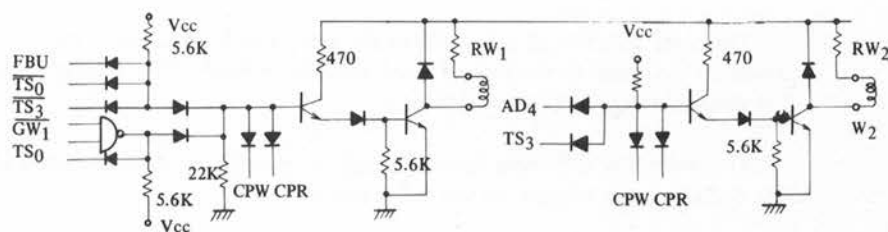


Fig. 2-23 Write Amplifier Circuit

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In Fig. 2-23 RW2 resistor is set at $30\ \Omega$ with the current flowing into the write head W2 at 150mA and the RW1 resistor is adjusted by viewing the signal of read amplifier; so that the data levels of W1 and W2 are equal.

2.5 Read Amplifier

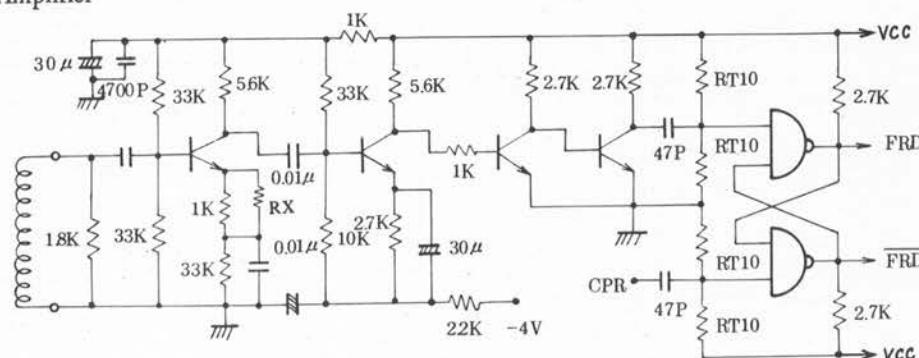


Fig. 2-24 Read Amplifier Circuit

In Fig. 2-24, the variable resistor $1K\Omega$ adjusts the signal level of the collector of 2nd transistor at 2V (p-p) and the position of the read head sets the pulse width of FRD at $1.2\mu\text{sec}$.

MONROE 920**PRINCIPLE 1****1. Outline of Operation Principle****1.1 Special Features of Operation**

Monroe 920 uses the delay line for its register and has one word for the indication register and three words for arithmetic registers, making four words in all.

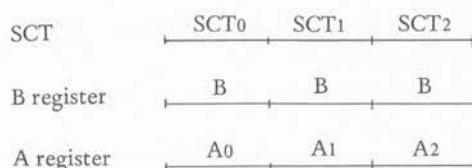


Fig. 3-1 Data in each Registers

The registered numeric or the calculated result are entered in B register and the number of fractional digits of the registering numeric must be less or equal than the affixed decimal point position, except for the multiplier in multiplication and the divisor in division (when $\boxed{K}$ key is not locked) in which it is the floating decimal point system. The decimal point coordination in the B register always takes place before transferring the data from B register to A register. Even though the data is not transferred, the decimal point coordination is done before the operation starts in case of addition and subtraction. Consequently, before the commencement of any calculation operation, the decimal point coordination of all the data are completed; so only one decimal point counter is necessary.

Since the data of each register are written into the same delay line, then the clock frequency (TS) of the delay line is four times higher than the clock frequency (CP) for operation.

To indicate a negative value, the complement indication system is adopted.

1.2 Outline of Addition and Subtraction**1.2-1 General**

When addition or subtraction of two numbers is performed, their decimal point positions should be coordinated to the affixed decimal point position before the operation starts. In addition of the two numbers, the augend and the addend are entered into their respective registers and then the operation is performed. If the augend and the addend are denoted as A.a and B.b respectively, the operation can be performed as follows:

A.	a	A: Integral numeric of an augend
+ B.	b	B: Integral numeric of an addend
		a: Fractional numeric of an augend
Answer:		b: Fractional numeric of an addend

A.a and B.b are entered into the accumulator and B register respectively.

In this calculator, the decimal points of all data are coordinated to the affixed decimal point position before the calculation starts as shown in Fig. 3-2.

MONROE 920

PRINCIPLE 2

Ex. 3-1 1 2 3. 4 5 + 5 4. 3 2 1 Dℓ = 4: Affixed decimal point position

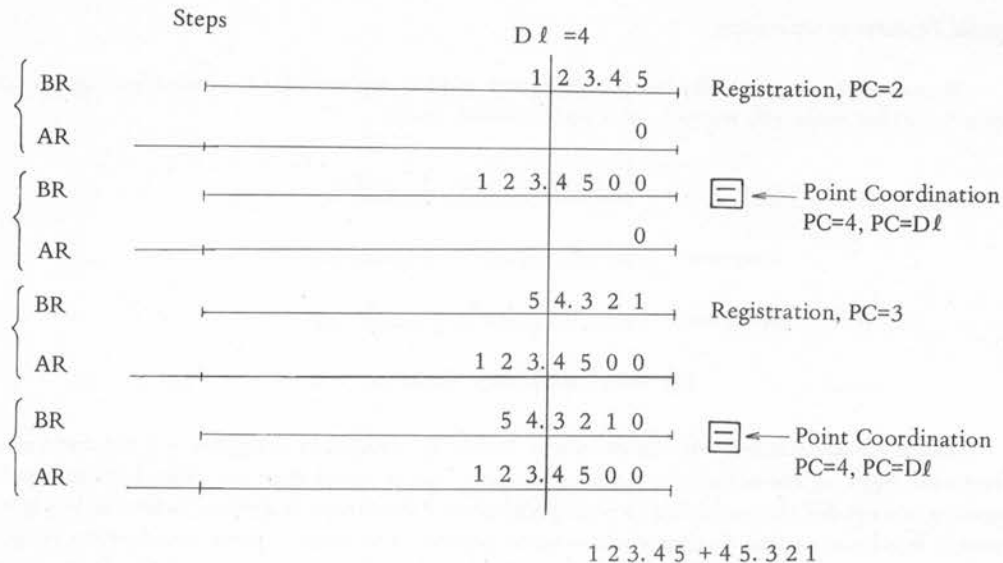


Fig. 3-2 Steps of Addition and Subtraction

1.2-2 Subtraction

Subtraction is performed by adding the complement of it and if the calculated result is a negative value, then the complement is indicated, because after the complement conversion, subtraction is performed by adding the two numbers as in the case of a Monroe 990, and since Monroe 920 is not provided with a negative sign flip-flop; so when the result of subtraction operation is a negative value, it is not converted into its true value but indicated as a complement.

Ex. 3-2 5. 6 - 3. 4 5 = 2. 1 5

5. 6 0		5. 6 0
-3. 4 5	complement	→ 9 9 9 6. 5 5
2. 1 5	conversion	10 0 0 2. 1 5
		↑ omitted

Ex. 3-3 4. 5 6 - 7. 8 = -3. 2 4

4. 5 6		4. 5 6
-7. 8	complement	→ +9 9 . . . 9 2. 2 0
-3. 2 4	conversion	9 9 . . . 9 7. 7 6
		↗ complement

Fig. 3-3 Complement Subtraction

In Ex. 3-2 and Ex. 3-3, when a carry signal to the most significant digit (MSD) is emitted, the result is a true value, but when a carry signal is not emitted, the result is a negative value which is indicated as a complement.

MONROE 920**PRINCIPLE 3****1.3 Outline of Multiplication****1.3-1 General**

The method of multiplication operation is shown in Fig. 3-4: namely, in case of $A \times B = C$, the multiplicand and the multiplier are entered into B and A0 registers respectively at the start of the operation and the product appears in the two series connected registers A1 & A2.

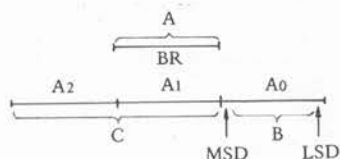


Fig. 3-4 Data in each register in multiplication

If the number of digits of the multiplicand A, the multiplier B and the product C are denoted as [A], [B] and [C] respectively, then $[C] = [A] + [B]$; so the product requires the registers of two words in length, i.e., A1 and A2, so that the calculation digits are 12×12 .

Multiplication operation is performed by transferring the multiplicand A (content of B register) to the accumulator A1 and adding to itself the same number of times as the value of multiplier B (content of A0 register). This procedure is the same as that of Monroe 950.

Thus, the multiplicand is added to A1 register and 1 is subtracted from the MSD of the A0 register. This operation is repeated until the MSD of the A0 register becomes 0. When MSD becomes 0, the multiplier and the partial result of the product shifts to the left one digit, and again the multiplicand is added to A1 register with 1 being subtracted from the MSD of the multiplier every time it is added once.

This continued until there is no subtraction operation, so A1 and A2 are operated as one accumulator. Since the result shifts 16 times to the left to enter the result in A2 register. In this model, multiplication calculation must be finished at the PC=0 and also the decimal point position of the product must be coordinated with D1, so the number of shift S is as follows:

$$S = (15 - P) + 16 = 31 - P$$

P : Decimal point position of multiplier.

In above equation, $15 - P$ is the number of left shifting to calculated the whole numerals in A0 register, then PC must count once (PC+1) before the calculation operation starts so that to obtain the proper result.

PRINCIPLE 4

MONROE 920

Thus, the calculation operation and total left shifting take place for 31 - P times.

Ex. 3-4

$$12 \times 21 = 252$$

multiplicand	multiplier
12	21
+ 12	-1
+ 12	-1
24	01
24	01
+ 12	-1
252	0

Fig. 3-5 Multiplication Operation(1)

1.3-2 Decimal Point in Multiplication

Assuming that the number of digits of the multiplicand A.a; the multiplier B.b and the product C.c as [A]. [a]; [B]. [b] and [C]. [c] respectively, then the following expression is obtained:

$$[C]. [c] = [A] + [B]. [a] + [b]$$

So the decimal point position in multiplication is the sum of the fractional digits of the multiplicand and that of the multiplier.

For instance,

$$1.23 \times 2.1 = 2.583$$

In this model, only the decimal point of the multiplicand is coordinated to the affixed decimal point position in registration cycle; but the decimal point of the multiplier is a floating system, so it does not coordinated to it.

Ex. 3-5

$$A \times B = 4 \times 2.3 = 9.2$$

Multiplicand	Multiplier			
0	0 2 3	8		
+ 0	-1	+ 4	Omit →	+ 1
0	9 2 3	8 4		0 3
0	+ 1	+ 4		- 1
0	Omit →	8 8		2
+ 4	0 2 3	+ 4		- 1
4	-1	9 2		1
+ 4	1 3			- 1
8	-1			9
+ 0	0 3			+ 1
8	-1			Omit →
	9 3			0

Fig. 3-6 Multiplication Operation(2)

MONROE 920**PRINCIPLE 5****1.4 Outline of Division****1.4-1 General**

The operation of division is shown in Fig. 3-7. In $a \div b = c$, the divisor $[b]$ enters in B register and the dividend $[a]$ enters in the two registers A0 & A1 which are connected in series. The quotient $[c]$ enters in register A2.

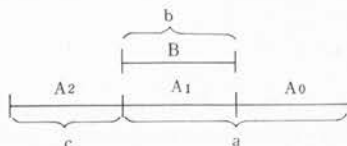


Fig. 3-7 Registration of Numerals in Division

The divisor $[b]$ (data of B register) is subtracted from the dividend $[a]$ (data of A1 register). The number of times of these subtractions which are repeated until just before the dividend goes over 0 and becomes a negative value, is the quotient of that digit and is added to A2.

Therefore, 1 is added to the LSD of A2 register every time the divisor in B register is subtracted once from the dividend in A1 register. This operation is repeated until there is no more subtraction of $A1 - B$. When the partial division has been completed, the dividend and partial quotient are shifted one digit to the left and same operation continues.

When the point counter becomes 0, the calculation operation is completed. If the decimal point position of the divisor is P, then the number of times of left shifting will be as follows:

$$\text{Number of times of left shifting} = 16 + P$$

Therefore, A0 ~ A1 are used as an accumulator of a two-word length. The remainder remains in A1 register at the end of the calculation.

Ex. 3-6 $15129 \div 369 = 41$

1 5 1 2 9	0	
- 3 6 9	+ 1	
1 1 4 3 9	1	
- 3 6 9	+ 1	
7 7 4 9	2	
- 3 6 9	+ 1	
4 0 5 9	3	
- 3 6 9	+ 1	
3 6 9	4	
- 3 6 9	4 0	Left Shift
0	+ 1	
	4 1	Quotient

Fig. 3-8 Division Operation

PRINCIPLE 6**1.4-2 Decimal Point**

Division is performed from the MSD of the dividend and calculated one by one to the right until all digits calculation are completed.

The decimal point in division is generally conformed that if the numbers of digits of the dividend and the divisor are $[A] \cdot [a]$ and $[B] \cdot [b]$ respectively, thus the decimal point of the division $A \cdot a \div B \cdot b$ is obtained as follows:

$$[a] - [b]$$

However, since the decimal point of the quotient is a fixed decimal point, then the quotient must appear at the affixed decimal point position; so the number of times of left shift to coordinate the decimal point of the quotient in the completed calculation is as follows;

$$\text{Number of times of left shifting} = 16 - ([a] - [b]) + D\ell$$

In this equation, $D\ell$ is the affixed decimal point position. Therefore, the calculation is finished when the left shift which is shown in the above equation, is completed.

The above equation can be simplified by the substitution of $[a] = D\ell$ as follows:

$$\begin{aligned} \text{Number of times of left shifting} &= 16 - D\ell + [b] + D\ell \\ &= 16 + b \end{aligned}$$

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PRINCIPLE 7

2. Operation Principle

Control counters are used in order to perform the calculation operation and the operations of each CC are as follows:

Entry cycle	CC0	Indication
	CC3	Shifting for decimal point coordination in registration. Data transfer, registration and left shift.
Operation	CC1	Shifting for the decimal point coordination in addition, subtraction and constant division.
	CC2	Interchanging of $B \leftrightarrow A_0$ in multiplication or constant division. Clearing of A1 & A2 register.
	CC6	Addition or subtraction in multiplication or division.
	CC7	Addition and subtraction. Correction of over-subtraction in multiplication and division.
	CC5	Left shifting of the data in $A_0 \sim A_1$ in multiplication or division.
	CC4	Interchanging of $B \leftrightarrow A_0$ in addition or subtraction. Transferring of $A_2 \rightarrow B, B \rightarrow A_0$.

2.1 Addition and Subtraction

When the calculated result is a negative value, the complement conversion performs and it is indicated as 10's complement.

2.1-1 Binary Code

The adopted binary code 2'-4-2-1 code in which it has self-complementing property, is very convenient in obtaining a complement.

The 2'-4-2-1 code is shown below:

	2' 4 2 1		2' 4 2 1
0	0 0 0 0	1 1 1 1	9 ($\bar{0}$)
1	0 0 0 1	1 1 1 0	8 ($\bar{1}$)
2	0 0 1 0	1 1 0 1	7 ($\bar{2}$)
3	0 0 1 1	1 1 0 0	6 ($\bar{3}$)
4	0 1 0 0	1 0 1 1	5 ($\bar{4}$)
5	1 0 1 1	0 1 0 0	4 ($\bar{5}$)
6	1 1 0 0	0 0 1 1	3 ($\bar{6}$)
7	1 1 0 1	0 0 1 0	2 ($\bar{7}$)
8	1 1 1 0	0 0 0 1	1 ($\bar{8}$)
9	1 1 1 1	0 0 0 0	0 ($\bar{9}$)

Fig. 3-9 2'-4-2-1 Binary Code

PRINCIPLE 8

MONROE 920

Thus, "NOT" signal of each number corresponds respectively to 9's complement of each number.

2.1-2 Discrimination of Signs for Calculated Result

1 $A + B$ $3 + 9 = 12$

$$\begin{array}{r} 0\ 0\ 0\ 0\ 0\ 0\ 0\ 3 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 9 \\ \hline \text{Positive} \rightarrow \boxed{0}\ 0\ 0\ 0\ 0\ 0\ 1\ 2 \end{array}$$

2 $-A + B$ $-5 + 8 = 3$ ($A < B$)

$$\begin{array}{r} 9\ 9\ 9\ 9\ 9\ 9\ 9\ 5 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 8 \\ \hline \text{Omit} \rightarrow \overline{A}\ \boxed{0}\ 0\ 0\ 0\ 0\ 0\ 0\ 3 \\ \text{Positive} \rightarrow \end{array}$$

3 $-A + B$ $-5 + 3 = -2$ ($A > B$)

$$\begin{array}{r} 9\ 9\ 9\ 9\ 9\ 9\ 9\ 5 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 3 \\ \hline \text{Negative} \rightarrow \boxed{9}\ 9\ 9\ 9\ 9\ 9\ 9\ 8 \end{array}$$

4 $-A + B$ $-5 + 5 = 0$ ($A = B$)

$$\begin{array}{r} 9\ 9\ 9\ 9\ 9\ 9\ 9\ 5 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 5 \\ \hline \text{Omit} \rightarrow \overline{A}\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \end{array}$$

5 $A - B$ $5 - 7 = -2$ ($A < B$)

$$\begin{array}{r} 0\ 0\ 0\ 0\ 0\ 0\ 0\ 5 \\ 9\ 9\ 9\ 9\ 9\ 9\ 9\ 2 \leftarrow 9\text{'s complement of } 7 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1 \leftarrow \text{To make } 10\text{'s complement} \\ \hline \text{Negative} \rightarrow \overline{A}\ 9\ 9\ 9\ 9\ 9\ 9\ 9\ 8 \end{array}$$

6 $A - B$ $5 - 2 = 3$ ($A > B$)

$$\begin{array}{r} 0\ 0\ 0\ 0\ 0\ 0\ 0\ 5 \\ 9\ 9\ 9\ 9\ 9\ 9\ 9\ 7 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1 \\ \hline \text{Omit} \rightarrow \overline{A}\ \boxed{0}\ 0\ 0\ 0\ 0\ 0\ 0\ 3 \\ \text{Positive} \rightarrow \end{array}$$

7 $A - B$ $5 - 5 = 0$ ($A = B$)

$$\begin{array}{r} 0\ 0\ 0\ 0\ 0\ 0\ 0\ 5 \\ 9\ 9\ 9\ 9\ 9\ 9\ 9\ 4 \\ +\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1 \\ \hline \text{Omit} \rightarrow \overline{A}\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \end{array}$$

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PRINCIPLE 9

$$\begin{array}{r}
 8 \quad -A - B \quad -5 - 2 = -7 \\
 \begin{array}{r}
 99999995 \\
 99999997 \\
 + 00000001 \\
 \hline
 \text{Omit } \rightarrow \boxed{9}9999993 \\
 \text{Negative} \rightarrow
 \end{array}
 \end{array}$$

	A	B	Ex.	Add or Sub.	Carry	+1	16th Digit	Posi. Nega
1	+	+	3+9=12	A+B	0	—	0	+
2	—	<+	—5+8=3	$\overline{A}+B$	1	—	0	+
3	—	>+	—5+3=—2	$\overline{A}+B$	0	—	9	—
4	—	=+	—5+5=0	$\overline{A}+B$	1	—	0	+
5	+	<—	5—7=—2	A+B	0	○	9	—
6	+	>—	5—2=3	A+B	1	○	0	+
7	+	=—	5—5=0	A+B	1	○	0	+
8	—	—	—5—2=—7	A+B	1	○	9	—

Table 3-1 Sign Discrimination

From the above table, “positive” or “negative” can be discriminated by the content of the MSD of the result. If the MSD is 0, then the result is positive; but if the MSD is 9, the result is negative with the negative value being indicated as a 10's complement. However OF signal must be “0” at the end of the calculation as explained later. When  key is pressed, always 1 is added to the complement to make a 10's complement.

2.1-3 Overflow of calculated result

	14th 15	13th D
a	0	0
OF b	0	1
c	9	9

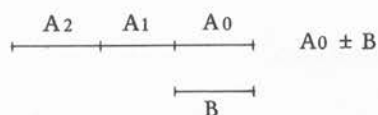
Fig. 3-10 Data in B Register

In this model, the capacity of each register is 16 digits, but since only 12 digits indicator is adopted, the overflow is discriminated by content of the 13th digit. In addition, the maximum value of the numeral that can enter the 13th digit is “1”. Which means that only the other numeral 0 can enter the 13th digit. In subtraction, no other numerals except “9” can enter the 13th ~ 15th digit when the result is a negative value. These three conditions of each case are illustrated in Fig. 3-10. There can be no other conditions beside these for addition or subtraction. In these three conditions, only b is the overflow occurring in the calculated result with OF signal becoming “1”.

2.1-4 Data Flow

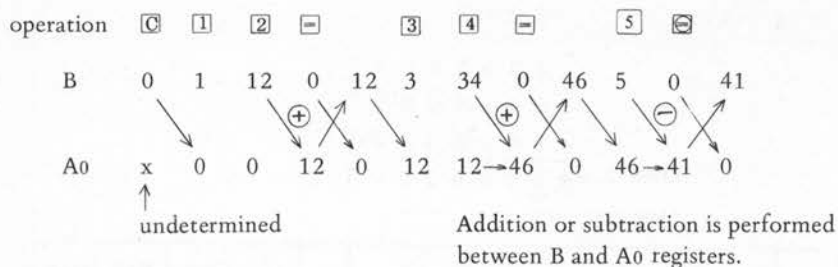
Ex. 3-7

$$12 + 34 - 5 = 41$$



PRINCIPLE 10

MONROE 920



2.1-5 Registration of numerals

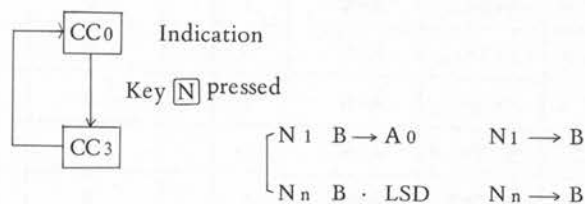


Fig. 3-11 Registration Cycle

CC0 is the indication cycle which indicates the data of B register by a dynamic indication system.

When the first numeral key N_1 is pressed, the cycle proceeds from CC0 to CC3 which transfers the data of B to A0 register and enters the numeral N_1 at the LSD of B register, and then returns to CC0.

Next, each time the second or third numeral key is pressed, the cycle proceeds from CC0 to CC3; so the registered numeric in B register shifts one by one to the left every time there is a registering of N_2 or N_3 into the LSD of B register, and then returns to CC0.

The checking of the overflow in the registration cycle is performed at CC3.

2.1-6 Data Flow of Addition or Subtraction

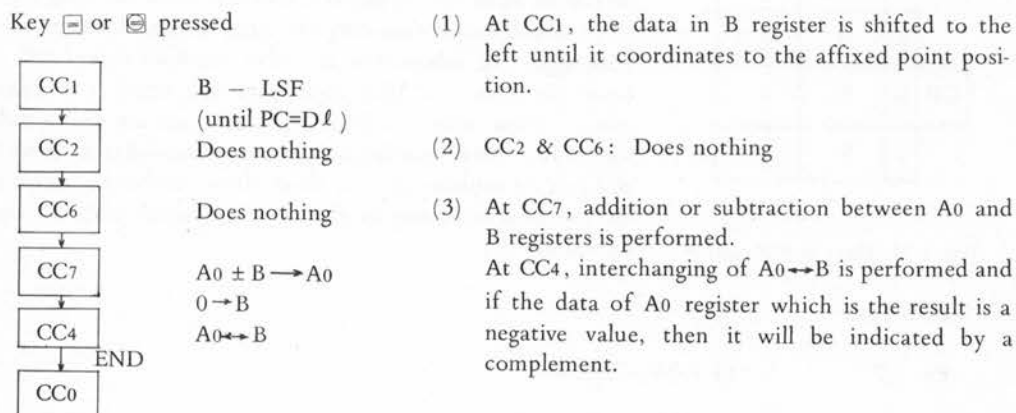


Fig. 3-12 Addition or Subtraction Cycle

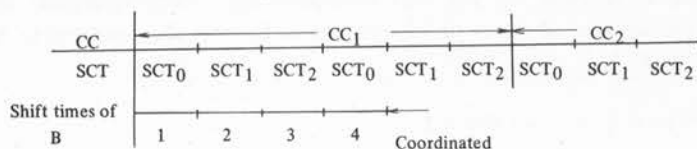
MONROE 920**PRINCIPLE 11****2.1-7 Decimal point coordination in B register**

Fig. 2-13 Decimal Point Coordination

Decimal point coordination is performed at CC1 only. When the coordination ends during CC1 cycle, it proceeds to the next step CC2 from SCT0 of CC1.

Since there is a SCT signal which is a 3 word time in this CC1, then the left shift can be performed three times. Since the affixed decimal point positions are 2~4, so it is possible to obtain the coordination in 2 cycles of CC1. Also, the $\square$ key always starts the cycle from CC1; **provided the decimal point is not coordinated at the start and proceeds to the next step CC2, after coordination. If the decimal point is coordinated CC1 is skipped and the system proceeds immediately to CC2.**

The checking of the overflow caused by LSF to coordinate the decimal point is also performed at CC1.

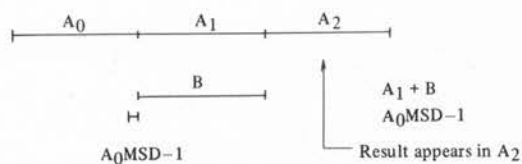
2.1-8 Operation

CC1	CC2	CC6	CC7	CC4	CC0
A0A1A2	A0A1A2	A0A1A2	A0A1A2	A0A1A2	A0A1A2
$A_0 \pm B$			$A_0 \rightarrow B$		
$B \rightarrow 0$			$B(0) \rightarrow A_0$		

The operation of $A_0 \pm B$ is performed at CC7. When the calculated result is a negative value and $\square$ key is pressed, always 1 is added to it to make a 10's complement at the start of the cycle. The operation of $B \rightarrow 0$ is also used for complement conversion by pressing $\square$ key again.

2.2 Multiplication**2.2-1 Outline of operation system**

In the operation system of this calculator, since $A_1 + B$ operation does not performed when the "A0 MSD-1" operation cannot be performed, so the over-subtraction correction is not done. Also since the product appears in A1 register, so it must be shifted 16 times more to enter A2 register.

2.2-2 Data Flow

The multiplicand and the multiplier enter A0 and B register respectively.

PRINCIPLE 12

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When the calculation starts, first the interchanging of $A_0 \leftrightarrow B$ takes place, so that the multiplicand is retained for constant multiplication. Partial products are added to $A_1 \sim A_2$ and the number of times of left shifting to transfer the products to A_2 register is expressed as follows:

$$S = 16 + \{15 - (a + b)\} + D\ell$$

a: Decimal point position of multiplicand.

b: Decimal point position of multiplier.

$D\ell$: Affixed decimal point position.

In this calculator, a always equals $D\ell$.

$$a = D\ell$$

Therefore, the above equation can be simplified by the substitution of $a = D\ell$ as follows:

$$S = 16 + \{15 - D\ell - b\} + D\ell$$

$$= 31 - b$$

The 1st term "16" of the first equation, means the number of times of left shifting to transfer the product from A_1 to A_2 register. The following is the actual data flow:

Ex. 3-8 Multiplication Operation

$$12 \times 21 = 252$$

Press	A ₂	A ₁	A ₀	B
	X	X	X	X
[1]	X	X	X	1
[2]	X	X	X	12
[X]	X	X	12	12
[2]	X	X	12	2
[1]	X	X	12	21
[=]	0	0	21	12
	0	252	0	12
	252	0	0	12
	0	0	12	252

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PRINCIPLE 13

Ex. 3-9 Constant Multiplication

$$12 \times 3 = 36$$

$$12 \times 4 = 48$$

$$12 \times 5 = 60$$

	A 2	A 1	A 0	B
☒ key lock	X	X	X	X
☐ 1	X	X	X	1
☐ 2	X	X	X	12
☒ X	X	X	12	12
☐ 3	X	X	12	3
☐ =	X	X	3	12
	36	0	0	12
	0	0	12	36
☐ 4	36	0	12	4
☐ =	0	0	4	12
	48	0	0	12
	0	0	12	48
☐ 5	48	0	12	5
☐ =	0	0	5	12
	60	0	0	12
	0	0	12	60

When ☒ key is locked and the multiplication is completed once, the transferring of B→A0 is not performed; so the constant is retained in A0 as a multiplicand.

Ex. 3-10 Square

$$4^2 = 16$$

	A 2	A 1	A 0	B
	X	X	X	X
☐ 4	X	X	X	4
☒ X	X	X	4	4
☐ =	0	0	4	4
	16	0	0	4
	0	0	4	16

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Ex. 3-11 Powers

$$2^4 = 16$$

☒ key lock

☐ 2

☒

☐

☐

☐

A2	A1	A0	B
X	X	X	X
X	X	X	2
X	X	2	2
0	0	2	2
4	0	0	2
0	0	2	4 2 ²
0	0	4	2
8	0	0	2
0	0	2	8 2 ³
0	0	8	2
16	0	0	2
0	0	2	16 2 ⁴

2.2-3 Registration

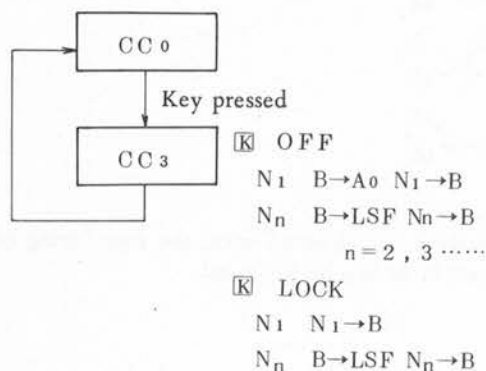


Fig. 3-14 Registration

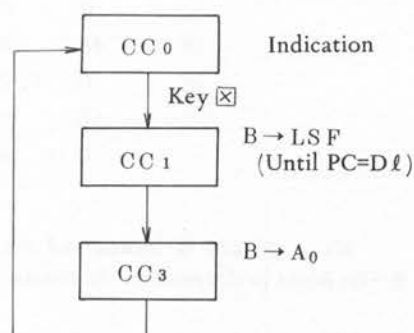


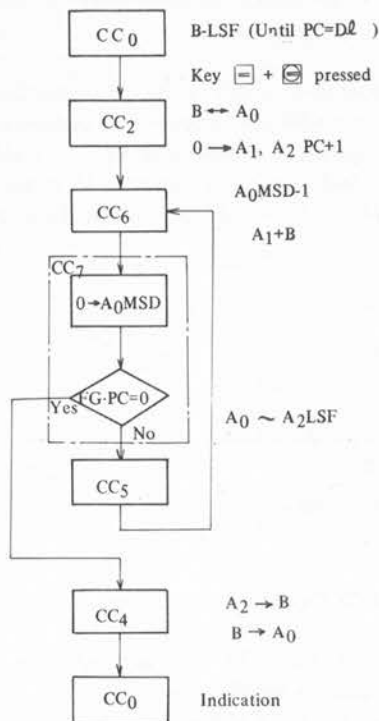
Fig. 3-15 Key operation

The registration cycle in multiplication operation of $a \times b$ is the same as that of addition or subtraction. When ☒ key is pressed, the data shifts to the left until $PC=Dl$ and then the transferring of $B \rightarrow A0$ is performed. In constant multiplication, $B \rightarrow A0$ is not performed when $N1$ which is the first numeral of multiplier. In simple multiplication, the registration cycle of the multiplier is the same as that of the multiplicand.

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PRINCIPLE 15

2.2-4 Multiplication Operation



- (1) At CC2, A1 and A2 registers are cleared and the interchanging of $B \leftrightarrow A0$ and PC+1 are performed.
- (2) At CC6, A0 MSD-1 is performed. If this subtraction can be done, $A1 + B$ is performed and if not, the operation proceeds to CC7.
- (3) At CC7, if FG.PC is not 0, $0 \rightarrow A0$ MSD is performed and the operation proceeds to CC5. If FG.PC is 0, then the operation proceeds to CC4.
- (4) At CC5, left shifting of $A0 \sim A2$ is performed.
- (5) CC4 transfers the result in A2 to B register and transfers the data of B to A0 register.
- (6) CC0 indicates the result of the operation.

Fig. 3-16 Multiplication Operation

(A) CC6 (Addition Cycle)

Ex. 3-12 $4 \times 2 = 8$ $Dl = 2$

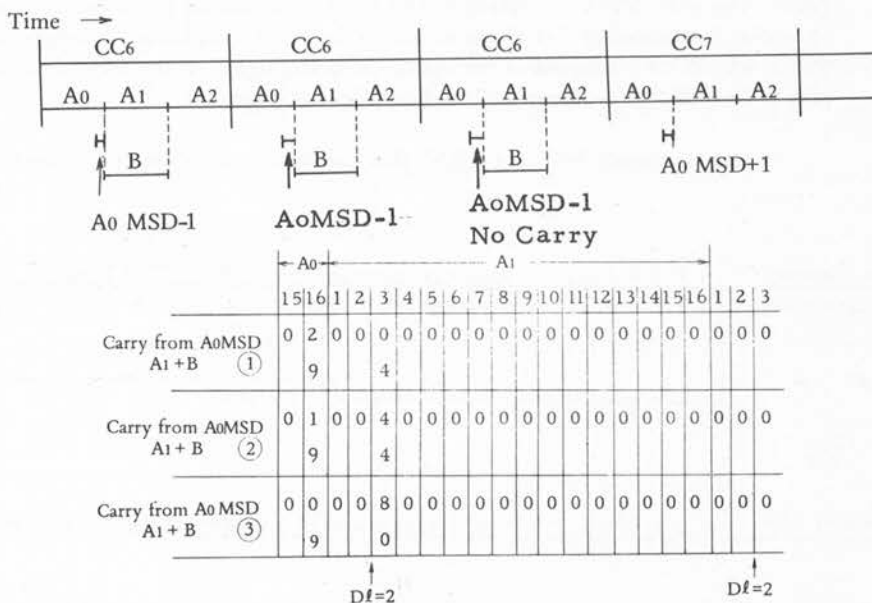


Fig. 3-17 Data Flow

The above diagram shows only a partial of CC6, when $2 \times 4 \rightarrow 2.00 \times 4$ is performed when $D\ell = 2$. Only after the repetition of $CC6 \rightarrow CC7 \rightarrow CC5$ 15 times does "2" enter into A0MSD.

Then the subtraction of A0MSD-1 takes place, so 9 which is the 10's complement of 1 is added to it and a carry is emitted every time the addition of $A_1 + B$ is performed. If a carry is not emitted, " $A_1 + 0$ " is done and the operation proceeds to CC7. In this case, "A0MSD becomes 0 when CC6 is repeated twice, and once more "A0MSD-1" is performed. At this time, since no carry is emitted from A0MSD, " $A_1 + B$ " is not calculated and the operation proceeds to CC7.

(B) CC7 (If $\overline{PC} = 0 \cdot FG$)

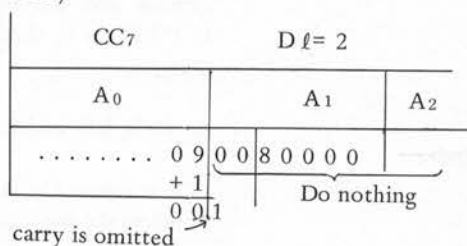


Fig. 3-18 Data at CC7 Cycle

In CC7, the correction of over-subtraction of A0MSD-1 is done, therefore, when "A0MSD-1" is performed when A0MSD=0, "9" remains in A0MSD. So in this model, A0MSD is cleared by closing the gate of $\overline{G-X}$ (223-6).

The data jumps from CC7 of the repetitive $CC6 \rightarrow CC7 \rightarrow CC5$ cycles. Thus, this repetitive operations of $CC6 \rightarrow CC7 \rightarrow CC5$ are performed "31-b" times as mentioned previously. "b" is the decimal point of the multiplier and stored in the point counter when the calculation step is started; therefore, $PC=0$ is the calculation ending condition. So when $PC+1$ is performed each time CC5 is in operation, the first " $PC=0$ " is obtained by counting " $PC+1$ " at "15-b" times. The next " $PC=0$ " is obtained after " $PC+1$ " is counted 16 times. This means that CC5 operation is repeated at "31-b" times before the entire calculation is completed. This is the reason why $PC=0$ is adopted as the operation ending signal. If the decimal point of the multiplier is "0", " $PC=0$ " is obtained at the first CC6, but is ignored.

In this case, since $b=0$ ($A.a \times B.b$), then the number of left shift is $31-0=31$ times.

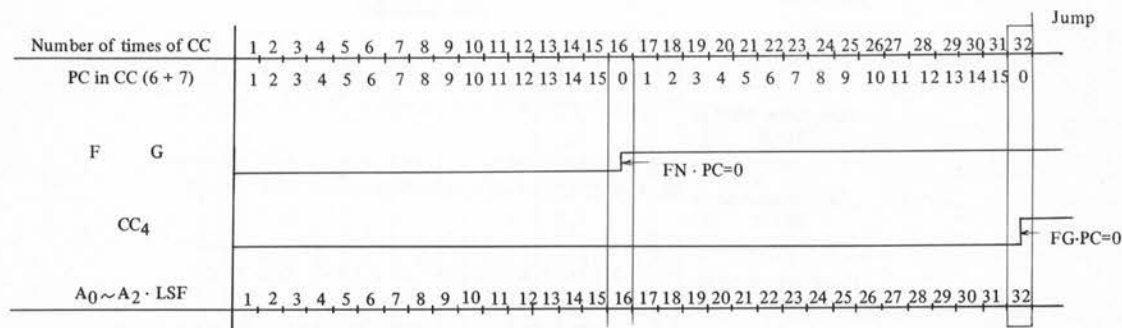


Fig. 3-19 Repetition of $CC6 \rightarrow CC7 \rightarrow CC5$ Cycles (1)

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PRINCIPLE 17

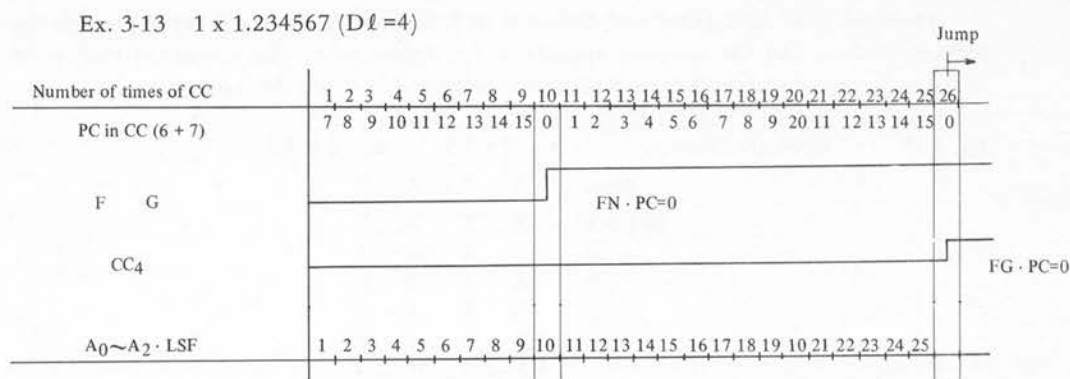


Fig. 3-20 Repetition of CC6 → CC7 → CC5 cycles (2)

In this case, $b = 6$, so left shift times are:

$$S = 31 - 6 = 25$$

(C) CC5 (LSF)

This cycle performs left shifting of partial products which is located in A1 ~ A2 registers where the multiplicand shifts one digit to the left to enter the MSD of A0 register in the 16th digit position and each time the point counter counts one ($PC + 1$).

(D) CC4 (A2 → B RSF)

The final answer obtained at CC7 is transferred to B register and it have its decimal point coordinated with the affixed decimal point. Also the point counter will be equal with the affixed point position in CC4.

2.3 Division

2.3-1 Data Flow

Ex. 3-14

$$30 \div 20 = 1.5$$

press	A 2	A 1	A 0	B
	X	X	X	X
[3]	X	X	X	3
[0]	X	X	X	30
[÷]	X	X	30	30
[2]	X	X	30	2
[0]	X	X	30	20
[=]	0	0	30	20
	1.5	X	0	20
	1.5	X	20	1.5

Fig. 3-21 Data Flow of Simple Division

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Dividend is in A0 register and divisor is in B register. When equal key is pressed, the division is done and the quotient appears in A2 register where the content is then transferred to B register and the data of B register simultaneously enters A0 register.

Ex. 3-15 Constant Division $3 \div 2 = 1.5$ $6 \div 2 = 3.0$

press	A 2	A 1	A 0	B
[K] Lock	X	X	X	X
[3]	X	X	X	3
[÷]	X	X	3	3
[2]	X	X	3	2
[=]	0	0	3	2
	1.5	X	0	2
	1.5	X	2	1.5
[6]	1.5	X	2	6
[=]	1.5	X	6	2
	3	X	0	2
	0	X	2	3

Fig. 3-22 Data Flow of Constant Division

When [K] key is locked the division order is memorized after the first calculation has ended. After the entry for the second calculation is completed, the content of B register does not transfer to A0 register; so, the former division is in A0 register and the new dividend is in B register.

As soon as the equal [=] key is pressed, the interchanging of $A0 \leftrightarrow B$ takes place and then the calculation begins.

2.3-2 Decimal Point Counter and Operation Ending Method

As previously explained, if the left shifting of "16 + b" times had been performed during the calculation.

In this calculator, PC is used as a subtraction counter which differs to that of multiplication. Since this counter adopts a hexadecimal, then the subtraction of PC-1 is done by adding 15 to PC. Then, "PC-1" takes place every time there is a left shifting and when it shifted "b" times which is the number of fractional numerals of the divisor the first "PC=0" is obtained.

After another 16 times of left shifting has been performed, the second PC = 0 will again appear which is used as the calculation ending signal. This means that "16 + b" times of left shifting have been performed. Therefore, the data in the A2 register is calculated completely.

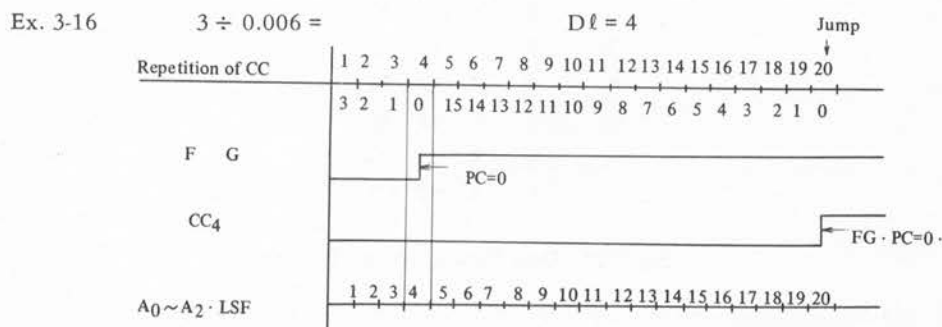


Fig. 3-23 Repetition of CC6 → CC7 → CC5 in Division Calculation

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PRINCIPLE 19

In this example, $b = 3$, then;

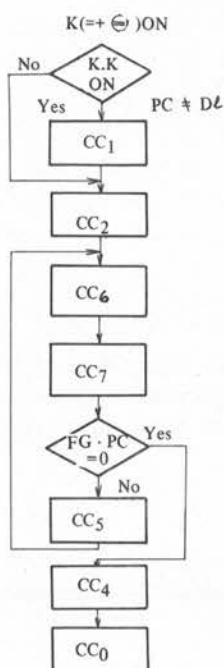
$$S = 16 + 3 = 19$$

The number of left shiftings is 19 times, and the number of times of repetitions of $CC6 \rightarrow CC7$ is $S + 1$, which is 20 times.

2.3-3 Registration System

Exactly the same as multiplication.

2.3-4 Division Operation



- (1) CC1: When $\boxed{K}$ key is locked, the data in B register shifts to the left until it coordinates to the affixed point position. If $PC \neq D\ell$ it repeats to shift in CC1, but if $PC = D\ell$ it advances to CC2.
- (2) CC2: When $\boxed{K}$ key is locked, the interchanging of $A0 \leftrightarrow B$ is done, but when $\boxed{K}$ key is not locked and FG set, then the interchange of $A0 \leftrightarrow B$ **does not take place**.
- (3) CC6: If there is a subtraction of $A1 - B$, then $A2 + 1$ is done; but if not, the operation will proceed to CC7.
- (4) CC7: This cycle performs the correction of over-subtraction at CC6, which is $A1 + B$.
- (5) CC5: It performs left shifting of $A0 \sim A2$.
- (6) CC4: Transferring of $A2 \rightarrow B$ performs and decimal point coordination of $PC = D\ell$ takes place.

Fig. 3-24 Division Operation

(A) CC6 (SUB)

$$5 \div 2 \quad D\ell = 3$$

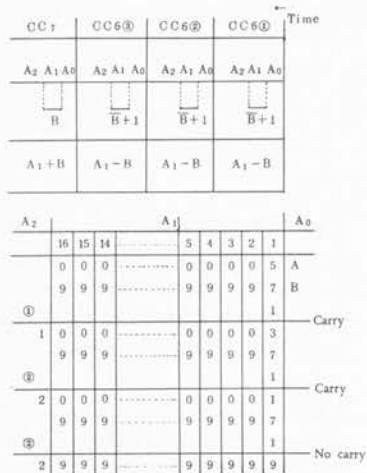


Fig. 3-25 Data Flow

Fig. 3-25 is the operation procedure in CC6 when the cycle of CC6 $\rightarrow$ CC7 $\rightarrow$ CC5 has been repeated 13 times, the dividend in A0 has entered A1 register and a partial quotient has just began.

If the subtraction of $A1 - B$ can be done, then a carry is added from the MSD of A1 to the LSD of A2 register, that is, when a subtraction is performed, "+1" operation takes place automatically. When it over-subtracts, this carry will not be emitted and the operation will proceed to CC7.

(B) CC7 (ADD)

This cycle corrects the over-subtraction of $A1 - B$. This can be done as $A1 + B$, because the numeric in A1 register in over-subtraction is a 10's complement of it and can be calculated by a simple addition. The carry which is generated from A1 to A2 register in this addition is omitted.

(C) CC5 (Left Shifting)

The calculated result in A1 ~ A2 register shifts to the left as that in multiplication.

(D) CC4

It is the same as that of multiplication.

MONROE 920**OPERATION PROCEDURES 1****1. Explanation of Blocks****1.1 Input Blocks****1.1-1 Key Circuit**

Key circuit is the same system as that of Monroe 950. The only difference is that in case of the N + P (numeral keys and decimal point key) or $\overline{CI}$ key, it is not necessary to give an electric potential to them independently from V_{cc} through resistors; therefore, these resistors can be omitted and sometimes an AND resistor is used in their places.

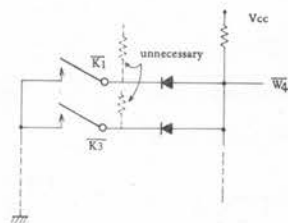


Fig. 4-1 Key Circuit and Logic Diagram

1.1-2 Key OR Circuit

$\overline{W1}$, $\overline{W2}$, $\overline{W3}$ and $\overline{W4}$ are encoded output signals corresponding to each respective digits of the 2'-4-2-1 code:

For instance,

$$\begin{aligned}\overline{W4} &= \overline{K1 \cdot K3 \cdot K5 \cdot K7 \cdot K9} \\ &= \overline{K1 + K3 + K5 + K7 + K9} \\ \therefore W4 &= K1 + K3 + K5 + K7 + K9\end{aligned}$$

Therefore, $\overline{W4}$ corresponds to "1" of the 2'-4-2-1 code which becomes "1", only when an odd numeral key is pressed. Similarly, $\overline{W3}$, $\overline{W2}$ and $\overline{W1}$ correspond to "2", "4" and "2" of 2'-4-2-1 code respectively.

The above equation can be illustrated by a logic circuit as follows:

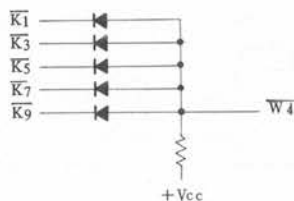


Fig. 4-2 Key AND Circuit

The key start circuit is the same as that of Monroe 950 except double entry prevention circuit memory control key & shift key circuits. For instance, the signal KN+P is emitted when a numeral or a decimal point key is pressed.

Therefore: $KN+P=\overline{W_4} \cdot \overline{W_5}=W_4+W_5=K_0+K_1+K_2+K_3+K_4+K_5+K_6+K_7+K_8+K_9+K_p$

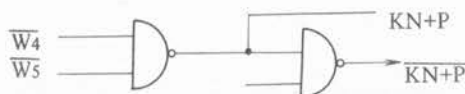


Fig. 4-3

1.1-3 Start Circuit

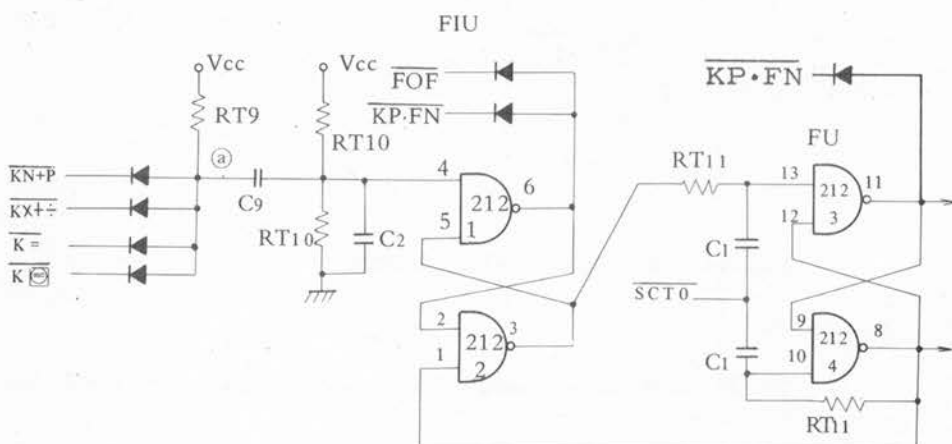


Fig. 4-4 Key Start Circuit

When any numeral or order key except **C**, **CI** or **K** key is pressed, FIU sets when **FOF** and **KP · FN** is 1.

FU sets at the first fall time of $\overline{\text{SCT0}}$ when FIU (212-6) is set, but when FOF or $\overline{\text{KP.FN}}$ is 0, then 212-6 is inhibited, so FU is not changed even though any numeral or order key is pressed, therefore this condition is overflow or point key is pressed.

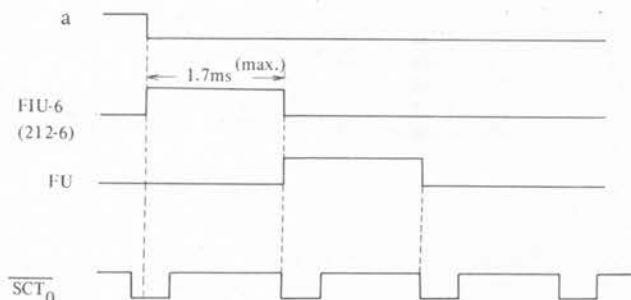


Fig. 4-5 Timing Chart of Start Circuit

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OPERATION PROCEDURES 3

1.1-4 Registration Circuit

The registration circuit encodes the numeral signal into the 2'-4-2-1 code and enters the signal into the SD.

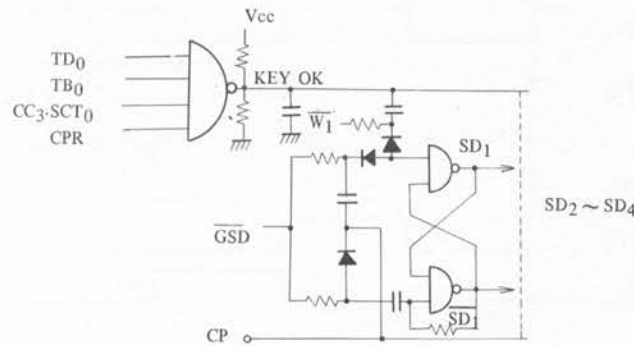


Fig. 4-6 Registration Circuit

In registration cycle, SD1 is set by a clock pulse consisting of $CC3 \cdot SCT0$, $TD0$, $TB0$ and CPR when $\overline{W1}$ is "0". In indication cycle or while the calculation is proceeding, the circuit is operated by CP according to the signals of $\overline{GSD}$.

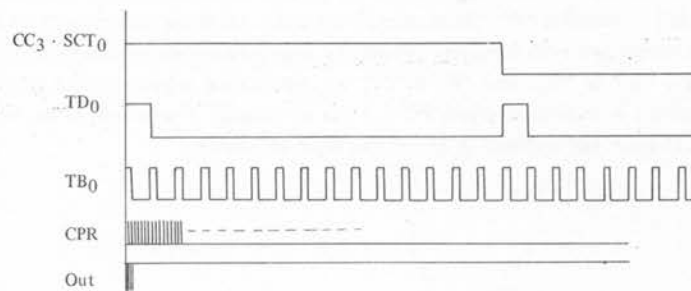


Fig. 4-7 Timing Chart in Registration

Thus, the clock pulses are emitted at the rate of 4 clock pulse at $SCT0$.

1.2 Output Blocks

1.2.1 Digit Selection Circuit

Digit selection is done by selecting the input signal of the primary side of the drive transformer one by one. This digit selection signals $FD1 \sim FD8$ are formed by counting $TB0$.

$\overline{FD4} \cdot \overline{FD8}$ selects the digits of 1~4 digits, $FD4 \cdot \overline{FD8}$ selects 5~8, $\overline{FD4} \cdot FD8$ selects 9~12 digits as follows:

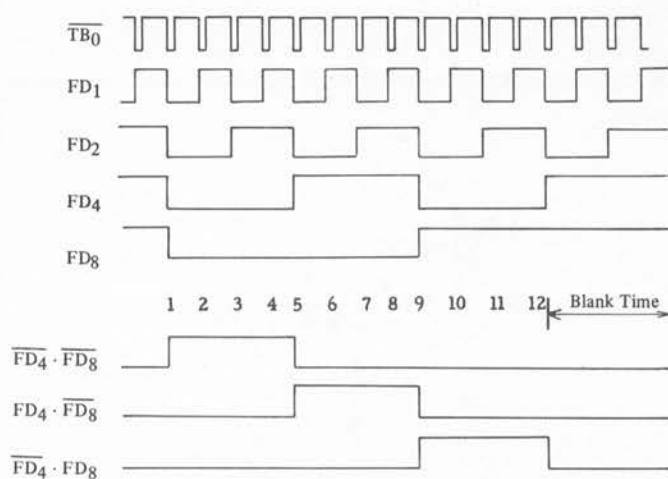


Fig. 4-8 Digit Selection Pulse Timing Chart

1.2-2 Numeral Selection Circuit

First, it is the discrimination of either an odd or even number. If the value of LSD of a 2^4 -4-2-1 coded numeral is "0", the numerals are even numbers including 0; and if the value is "1" the numerals are odd number. Then the discriminations between "0" & "1", "2" & "3", "4", "5", "6" & "7", and "8" & "9" are performed which selects all the numerals. The decimal point is indicated when PC = 15 is obtained. Therefore, if PC becomes 15 at the selected TD time, the decimal point of the digit will be lit.

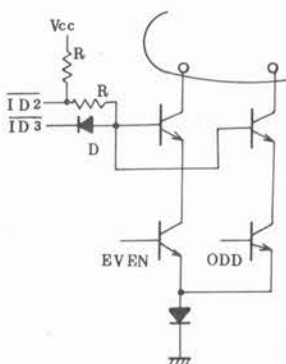


Fig. 4-9 Numeral Selection Circuit

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OPERATION PROCEDURES 5

		ID1	ID2	ID3	ID4		
		2'	4	2	1		
EVEN	0	0	0	0	0	A	} $\overline{4} \cdot \overline{2}$
ODD	1	0	0	0	1	A	
E	2	0	0	1	0	B	} $\overline{2}' \cdot 2$
O	3	0	0	1	1	B	
E	4	0	1	0	0	C	} $\overline{2}' \cdot 4$
O	5	1	0	1	1	D	
E	6	1	1	0	0	E	} $2' \cdot \overline{4}$
O	7	1	1	0	1	E	
E	8	1	1	1	0	F	} $4 \cdot 2$
O	9	1	1	1	1	F	

ODD = 1
 EVEN = 0

Table 4-1 Numeral Selection Table

OPERATION PROCEDURES 6**1.3 Operation Block****1.3-1 Registers****(1) A Register**

This register consists of 5 flip-flops (AD1, AD2, AD3, AD4 & AD0) and the delay line which circulates once at one SCT time. The sequence of signals A0, A1 & A2 are always changing, so that each of these signals may be able to appear in AD0 according to each SCT time respectively. This register operates as an accumulator and performs calculation operation together with the B register and the result remains in A2 register.

(2) B Register

This register consists of BD0 and a delay line which has one SCT time. Since data are always read in BD0 regardless of each SCT time, this register can be paired with any of the registers A0, A1 & A2. Not only does it register the numerics, but also the calculated result enters B register.

(3) S Register

This register is used for one digit memory in the registration cycle and the left shifting of A and B registers. The registration is performed by a clock pulse for only this register and at other times it is triggered by CP.

(4) I Register

This is an indication register which stores for 4-bit time for indication. The data are transferred from the S register and BD0 to this register in parallel of four bits.

1.3-2 Data Gates**(1) $\overline{G-X}$: X-side of the adder.**

G-AX: The data of the A register usually circulates through this gate. This gate closes when ☐ key is pressed and when A1 & A2 are cleared at CC2 before the calculation starts, and also for left shifting, transferring and interchanging of the A register.

G-SX: Opens when the A register shifts to the left in multiplication and division.

The logic and circuit of $\overline{G-X}$ are illustrated in Fig. 4-10.

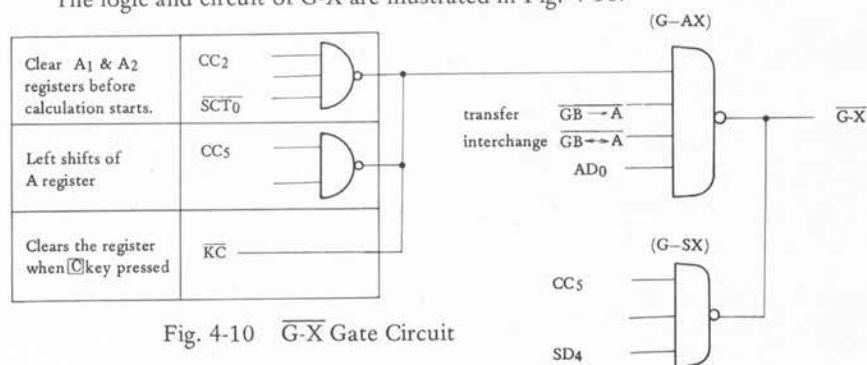


Fig. 4-10 $\overline{G-X}$ Gate Circuit

MONROE 920

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- (2) $\overline{G-Y}$: This is the input gate of the Y-side of the adder and illustrated in the logic diagram as follows:

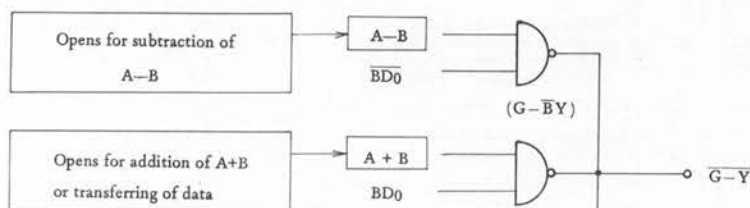


Fig. 4-11 $\overline{G-Y}$ Gate Circuit

$\overline{G-BY}$: Opens when the data of B register is added to A register or the data of B register is transferred to A register in addition, multiplication or division. It is illustrated in the following logical diagram:

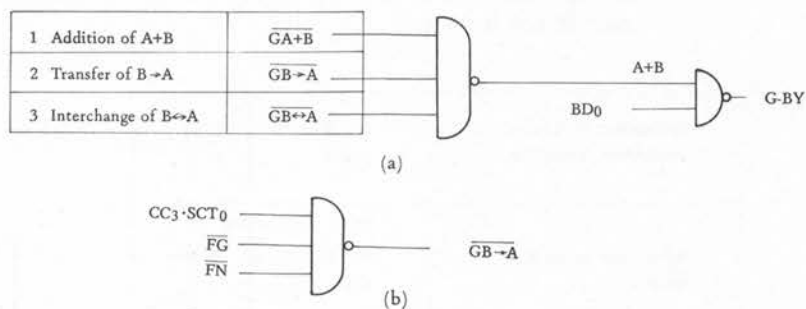


Fig. 4-12 G-BY Gate Circuits

Input gates of G-BY are as follows;

$\overline{GB-A}$: Fig. 4-12 (b) is the transferring of N1 from B to A register in the registration cycle. FG discriminates whether it is a constant multiplication (or division) or not.

$\overline{GB-A}$ Interchanging of $B \leftrightarrow A0$.

It opens when any interchanging operation of $B \leftrightarrow A0$ ①~③ is performed.

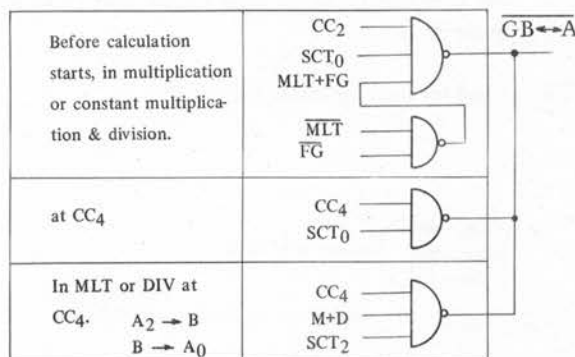


Fig. 4-13 $\overline{GB-A}$ Gate Circuit

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$\overline{GA+B}$: Opens when any of the following operations of ① ~ ③ is performed.

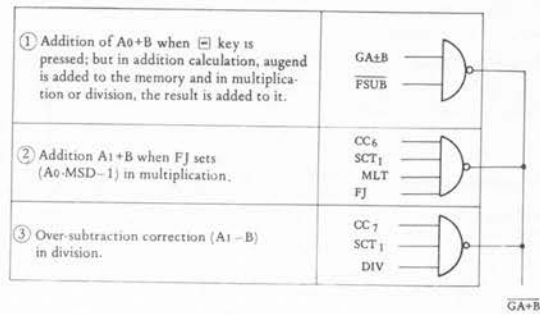


Fig. 4-14 $\overline{GA+B}$ Gate Circuit

(4) $G-\overline{BY}$: Opens when there is any subtraction of A_0-B in subtraction; $A_0 \cdot MSD-1$ in multiplication; A_1-B in division, or $M-B$ in multiplication or division when the $\square$ key is pressed.

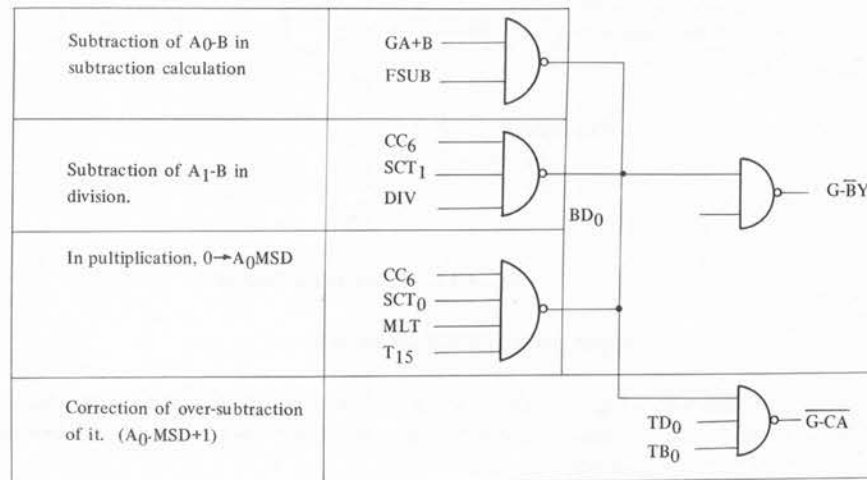


Fig. 4-15 $G-\overline{BY}$ Gate Circuit

(5) $\overline{G-CA}$: Used for complement correction; therefore, since the result of $A+\overline{B}$ ($A < \overline{B}$) is the complement of 9, then 1 must always be added to make it the complement of 10.

(6) $\overline{G-FCA}$: Used for discriminating the carry.

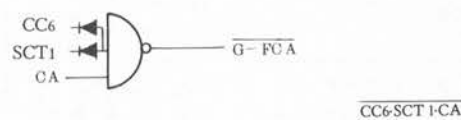


Fig. 4-16 $\overline{G-FCA}$ Gate Circuit

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- (7) $\overline{G-SD}$: Used for the indication of the data in B register and left shifting of B or A register.
- (8) $\overline{GW1}$: Input side gate of the write amplifier where all of the data of the registers are written.

1.3-3 Full Adder

This adder is used for addition, subtraction, multiplication and division and sequent addition is performed.

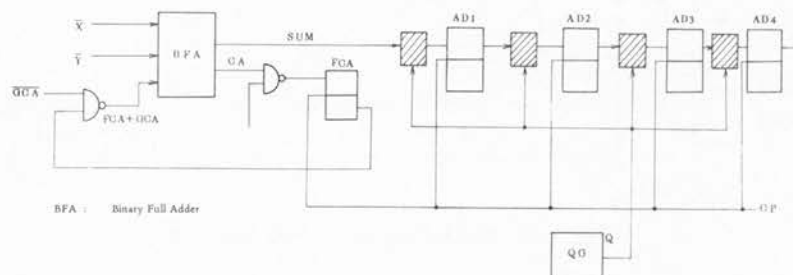


Fig. 4-17 Block Diagram of Full Adder (1)

This model adopts the same decimal correction method as that of Monroe 950.

To make correction for the conversion to 10's complement in subtraction, it is performed by a forced "+1" operation prior at the starting of calculation. $\overline{GCA}$ is a gate to perform this operation.

© Binary Full Adder

The logical equation of binary addition is as follows:

$$\begin{aligned} \text{SUM} &= X \cdot Y (FCA + GCA) + \bar{X} \cdot \bar{Y} (FCA + GCA) + \bar{X} \cdot Y \cdot \overline{GCA} \cdot \overline{FCA} + \overline{GCA} \cdot \overline{FCA} (X \cdot \bar{Y} + \bar{X} \cdot Y) \\ &= (X \cdot Y + \bar{X} \cdot \bar{Y}) (GCA + FCA) + (\bar{X} \cdot Y + X \cdot \bar{Y}) \cdot (\overline{GCA} + \overline{FCA}) \\ &= [(GCA + FCA)(X \cdot Y + \bar{X} \cdot \bar{Y}) + (\bar{X} \cdot Y + X \cdot \bar{Y})] [(GCA + FCA)(X \cdot Y + \bar{X} \cdot \bar{Y}) + \overline{GCA} + \overline{FCA}] \end{aligned}$$

This can be illustrated by the following logic diagram:

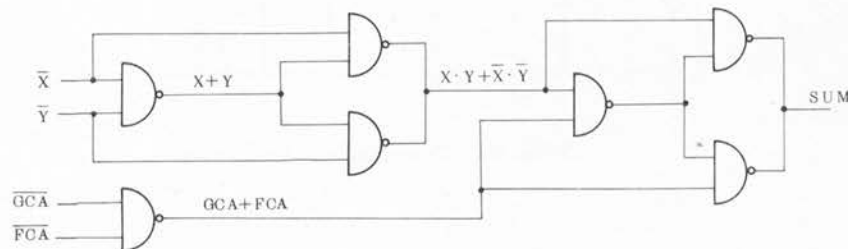


Fig. 4-18 Block Diagram of Full Adder (2)

$$\begin{aligned}
 CA &= X \cdot Y + X(FCA + GCA) + Y(FCA + GCA) \\
 &= \overline{X \cdot Y + (GCA + FCA)(\overline{X \cdot Y + X \cdot \overline{Y}})} \cdot (\overline{X \cdot Y + \overline{X \cdot \overline{Y}}})
 \end{aligned}$$

If the above is superimposed in the logic diagram of SUM, the following logic diagram is obtained:

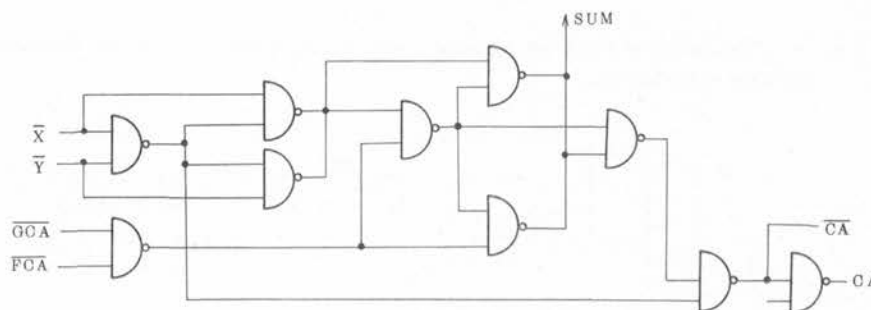


Fig. 4-19 Block Diagram of Full Adder (3)

The truth table of the binary full adder (BFA) is as follows:

X	Y	GCA	FCA	GCA+FCA	SUM	CA
0	0	0	0	0	0	0
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

Table 4-2 Truth Table of Full Adder

MONROE 920**OPERATION PROCEDURES 11****1.3-4 Decimal Point Counter (P counter)**

It is the hexadecimal subtraction counter which counts the decimal point positions and detects the ending time of multiplication or division calculation.

- (1) Memorizes the decimal point position for B register and discriminates the decimal point coordination.
- (2) Discriminates the ending time of the multiplication.
- (3) Discriminates the ending time of the division.

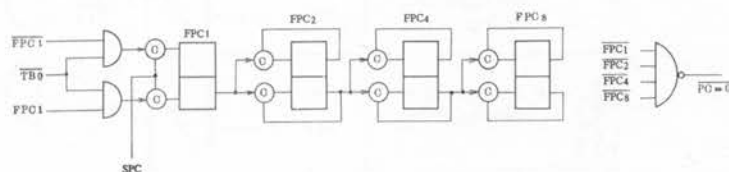


Fig. 4-20 Block Diagram of Hexadecimal Subtraction Counter

This timing chart is shown in the Fig. 4-23.

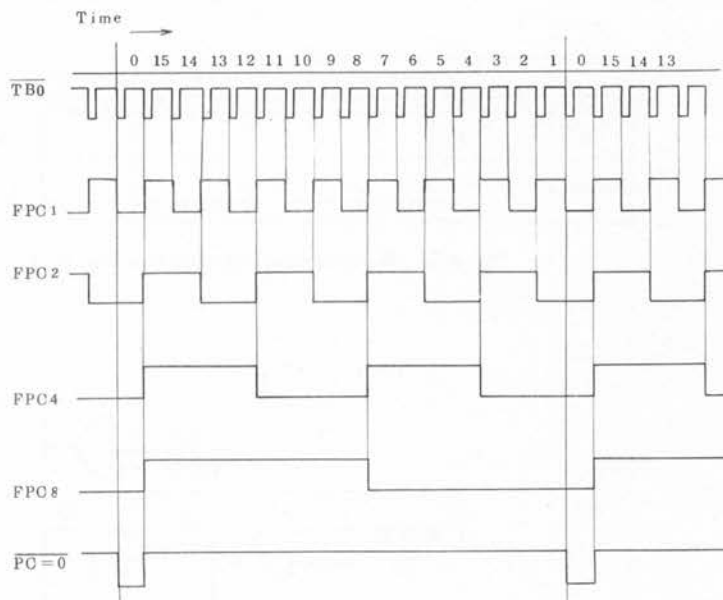


Fig. 4-21 Timing chart of Hexadecimal Subtraction Counter

- (1) Operation Gate: SPC

Since the P counter is a subtraction counter, then the addition of PC+1 is done by counting 15 times and the subtraction of PC-1 is done by counting 1 time.

“+1” . . . It counts during $\overline{\text{TD15}}$ (TD0 ~ TD14). (-15)

“-1” . . . It counts once at the time of TD15. (-1)

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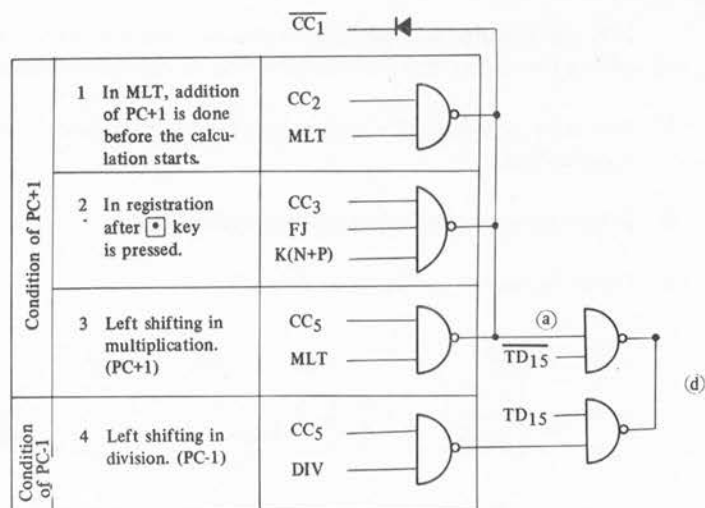


Fig. 4-22 Logic Gate of Point Counter

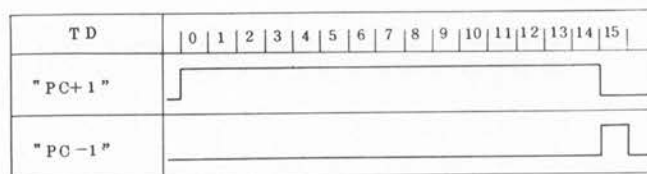


Fig. 4-23 Waveforms of (d) point in Fig. 4-24

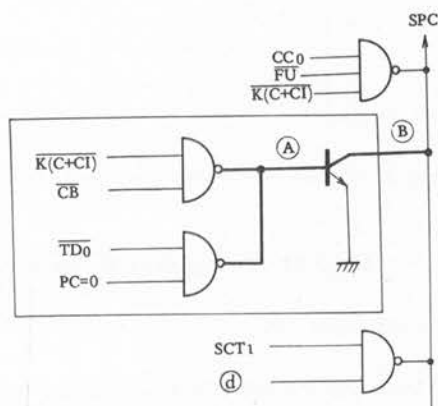


Fig. 4-24 PC Clear gate when $\square$ or $\square$ key is pressed

PC counts when the point ⑧ which is SPC in the timing chart is the condition of “0” (SPC=0).

$$PC = D \ell$$

This is a signal which discriminates the coordination of the point counter with the affixed dial position by means of a direct current.

Decimal point coordination signal of $PC=Dl$ is emitted when each output signal of PC coordinates to the affixed dial position.

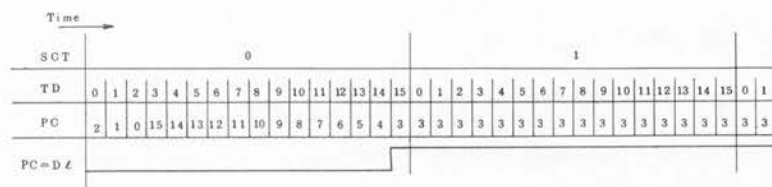


Fig. 4-26 Operation of PC when PC+1 takes place at SCT0 (Dl = 3)

1.4-1 Order Flip-flop

FMLT : It sets when  key is pressed.
FDIV : It sets when  key is pressed.
FSUB : It sets when  key is pressed.
FN : It discriminates whether it is the first numeral registration (N1) or not.

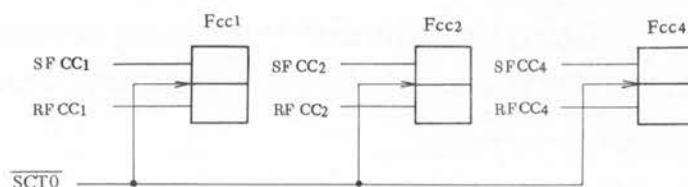


Fig. 4-27 Control Counter Block Diagram

Control counter consists of 3-bit counter which forms digit conditions and each signal which is encoded by the output signals of FCC is called "CC" with the trigger pulse for FCC being TS0. There are 7 CC's from CC0 ~ CC7.

1.4-2 Discrimination Flip-flops

These flip-flops discriminate and memorize various conditions and are used for controlling the "CC" or gate circuits.

(1) FJ

- 1 Sets when decimal point key is pressed during registration cycle.
- 2 Sets when a carry is emitted during subtraction of A0MSD-1 in multiplication.
- 3 Sets when subtraction of A1-B is completed in division.

(2) FG

- 1 Sets when $\boxed{K}$ key is locked;
- 2 Sets when the first "PC=0" signal is emitted during multiplication or division.

(3) FOF

- 1 Sets when a decimal point coordination overflow occurs except registration of multiplier or divisor when $\boxed{K}$ key is not locked.
- 2 Sets when any numeral enter into 13 ~ 15th digit position of B register except 0 and 9.

In the above 2 conditions, FOF sets and the overflow lamp lights up. So, FU is inhibited by FOF signal and all registration stops.

FOF resets when $\boxed{C}$ or $\boxed{CI}$ is pressed.

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2. Explanation of Operation Procedure

This chapter explains in detail the operation procedure of calculation.

2.1 Entry of Numeric

2.1-1 Numeral Keys ($\boxed{0} \sim \boxed{9}$ numeral keys & $\boxed{\cdot}$ key)

The entry of a number is performed at CC0 & CC3. The procedure of entry for this model is the same as that of Monroe 990 except that FN sets at the end of CC3.

(1) Registration Cycle

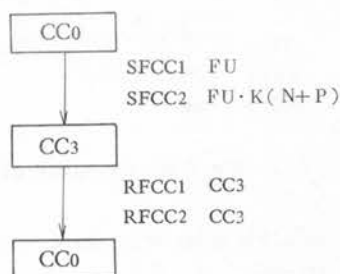


Fig. 4-28 Flow Chart of Registration Cycle

(2) Data Flow when $\overline{FN}$

When FN resets, the indicated numeric transfers to A0 register with the indication register clearing and enters N1 in the indication register.

- 1 $0 \rightarrow PC$ $SPC = CB(TD0 + \overline{PC} = 0)$
 $CB = CC3 \cdot SCT0 \cdot \overline{FN} \cdot K(N+P)$
 $SPC = CC3 \cdot SCT0 \cdot \overline{FN} \cdot K(N+P) \cdot (TD0 + \overline{PC} = 0)$
- 2 $B \rightarrow A0$
 $N1 \rightarrow B \cdot LSF$

These gate circuits are shown in Fig. 4-31.

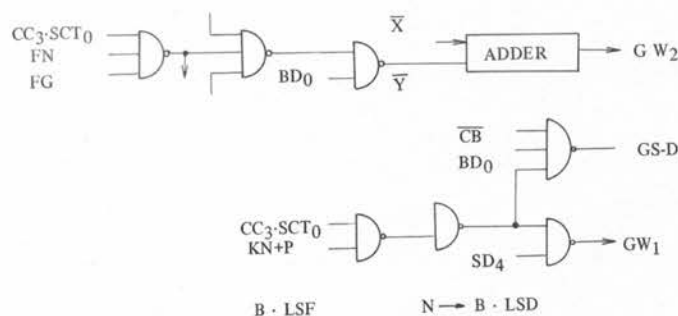


Fig. 4-29 Logic Gates in Registration

At the time of FN, the entered numeral shifts to the left whenever there is a registration one by one.

At this time, since the gate for data shifting of B register opens and the other gate of B register are normal condition.

(3) Setting Condition of FN

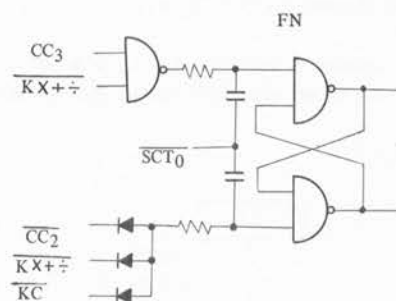


Fig. 4-30 Operation of FN

In the registration cycle, FN is set after the pressing of N1 or KP at the end of CC3 except $\boxed{\times}$ or $\boxed{+}$ key is pressed.

(4) Operation at the Time of FN

$B \rightarrow LSF$

$Nn \rightarrow B \cdot LSD$

The operation at the time of FN only differs from the operation at the time of $\overline{FN}$ is that there is no transferring of $A \rightarrow B$ in the former operation and at the time of FN, B register is not cleared. The gates for the B register are the same for both operations.

When $\boxed{\square}$ key is pressed, the inhibit signal $FN \cdot KP$ is emitted to inhibit FU which sets FJ. When there are any registration of numerals after FJ is set, PC counts 15 times ($PC+1$). Since SPC is emitted at the time of $CC3 \cdot SCT0 \cdot \overline{TD15} \cdot FJ \cdot K(N+P)$, the point counter counts the trigger pulses which are emitted 15 times, thus $PC+1$ is completed.

MONROE 920**HOW TO REPAIR 1****1. Operation Check Program****CHECK PROGRAM No. 1**

No.	SETTING SWITCH	OPERATION KEY	LAMP	INDICATOR	REMARKS
	Df		OF		
1	2	☒ $\uparrow$ ☒ 2 ☒	○	0000000002.00	
2	"	6 ☒ ☒		0000000004.00	
3	"	☒ 123456789 ☒		0123456789.00	
4	"	987654321 ☒		1111111110.00	
5	"	123456789 ☒		0987654321.00	
6	"	☒ 8000 ☒		0000123456.79	
7	"	☒ 9999 ☒		1234444443.21	
8	"	☒ .9999 ☒		1234567900.00	
9	"	☒ 8 ☒		9876543200.00	
10	"	☒ 9 ☒		8888888800.00	
11	4	☒ Lock	○		
12	"	☒ 9 ☒ ☒		00000001.0000	
13	"	☒		00000000.1111	
14	"	☒		00000000.0123	
15	"	☒ 123 ☒		00000001.5129	
16	"	456 ☒		00000005.6088	
17	"	.123000 ☒		00000000.0015	
18	"	.1 ☒		00000000.1000	
19	"	.3 ☒		00000000.3333	
20	"	6 ☒		00000020.0000	
21	"	123 ☒		00000410.0000	
22	"	2 ☒ ☒		00000004.0000	
23	"	☒		00000008.0000	
24	"	☒		00000016.0000	
25	"	☒		00000032.0000	
26	"	☒ ☒		00001024.0000	
27	3	1 $\div$.12345		00000000.1234	
28	"	☒ ☒ OFF .1234 ☒		000000008.103	

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2. Circuits

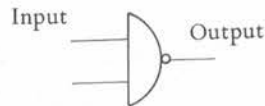
2.1 Precaution

- (1) Be sure that the power source of +200V or +120V is never touched during repairing.
- (2) Use a soldering iron of 30W without any leakage of power.
- (3) Use an oscilloscope which has the most suitable frequency characteristic as possible.
- (4) When the ground is not connected well between the oscilloscope and the machine body, a noise appears in the wave form, especially the ground line to the probe when it is touched to the read amplifier.
- (5) Removing of IC.
Remove the solder from the printed board with a tweezers while removing the solder of the pins of the IC with a soldering iron. Pull off the IC from the printed board after disconnecting of all the pins.

2.2 Integrated Circuit

1. Gates

Input and output voltage fluctuation allowance level of the integrated circuit is shown in the Fig. 5-1 for the logic gate. It is necessary to observe the signal level when checking the circuit.



Input		Output	
		For Gate	For FF
0 Level	0.5V max.	0.5V max.	0.5V max.
1 Level	2.4V min.	2.4V min.	4.0V min.

Fig. 5-1 Gate Signal Levels

Table 5-1

2. Flip-flop

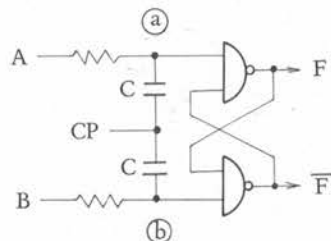


Fig. 5-2 Flip-flop

Input	Voltage
0	1.0 V max.
1	4.0V min.

CP 0 level 3.5~3.8V
Fall time 40ns max.
C = 47 pF
R = 22KΩ

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The flip-flop is set or reset by synchronizing to the clock pulse when the input signal is "0".

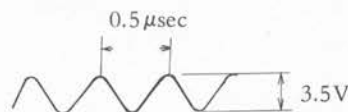
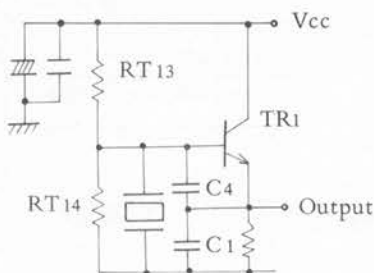
When the input voltage is less than 4V at the "1" signal, then the IC will not operate properly; so when checking the flip-flop, first, check the input levels, clock pulse voltages or wave forms.

Usually the capacity of condenser (C) is 47pF: but in some instance, the capacity must be increased a little according to the operation speed of the IC. In such case, the capacity of the condenser must be less than 100pF, but if larger capacity is required, the IC must be replaced. When the capacity of the probe is too large when observing the wave form with an oscilloscope, some times it interferes with the operation of the flip-flop. Especially when checking the wave forms at point (a) and (b) shown in the Fig. 5-2. Always be sure that a 10K Ω resistor is attached to the probe in series to prevent a mis-operation of the flip-flop. However, when attaching the resistor, sometimes the wave form becomes more or less dull. The input capacity of the probe of the oscilloscope is usually about 10pF.

2.3 Crystal Oscillator

Since the oscillation frequency of the crystal oscillator is decided by the natural oscillation frequency, then if it oscillates at a different frequency than the specified oscillation frequency 2MHz, the crystal is defected or damaged.

When checking the crystal oscillator, always be sure that an oscillation circuit is separated from the other circuits, as shown in the Fig. 5-3, and if it does not oscillate, then check whether the current is flowing to the transistor correctly or not, or whether the condenser C4 and C1 operates properly or not.



Waveform of the crystal oscillator.

RT13 = 56K Ω
 RT14 = 100K Ω
 C1 = 47pF
 C4 = 100pF

Fig. 5-3 Crystal Oscillator Circuit

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2.4 Delay line, Read and Write Amplifier

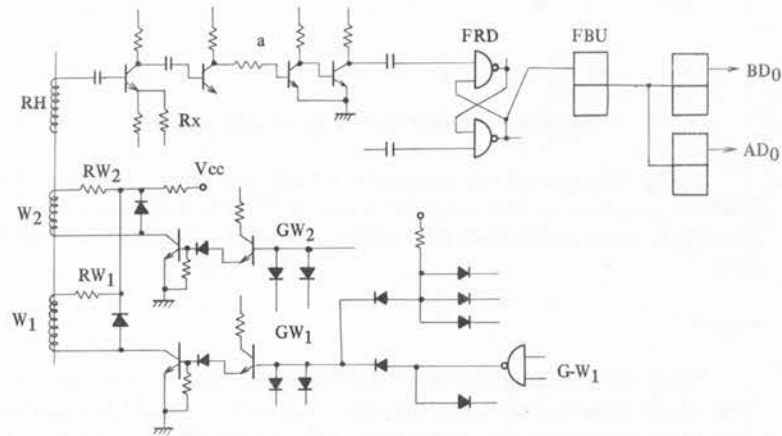


Fig. 5-4 Delay Line Circuit

There are four important points which must be adjusted in the delay line circuit.

1. Selection of the resistor series of RW1 & RW2 of the write head of W1 and W2.

RW1 resistor must be adjusted by viewing the read amplifier; so that the data levels of W1 and W2 are equal.
RW2 is fixed at 30Ω.

2. Gain adjustments of the read amplifier.

In Fig. 5-4, ground the terminal GW1 and disconnect the line of GW2, and then, connect the TS3 to the base of TR1 of W2 by using a diode as shown in Fig. 5-5.



Fig. 5-5 Gain Adjustment of the Read Amplifier

Adjust the parallel resistor (Rx), so that the signal level of point (a) in Fig. 5-4 is at 2V (p-p) while observing the wave form with the oscilloscope.

3. Delay time adjustment between W2 and RH is by setting the read head (RH) position.

Adjust the read head position, so that the pulse width of FRD is 1.0μsec at TS3 without changing the circuit after gain adjustment (2).

4. Delay time adjustment between W1 and RH is by setting the write head W1 position.

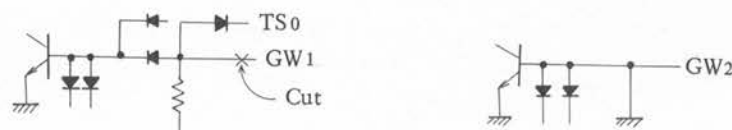


Fig. 5-6 Delay Time Adjustment of GW1

In Fig. 5-4, ground the terminal GW2 and disconnect the GW1. Then, adjust the write head W1 position, so that the pulse width of FRD is $1.2 \mu\text{sec}$ at TS3. If the signal level at point (a) is more or less than 0.3V from 2.0V , then adjust RW1 so that the signal level is just 2.0V .

5. Others

When the crystal or the delay line has been changed, it is necessary to adjust the delay time of all circuits, and when the signal circulates correctly through the delay line circuit, observe to see whether the output pulse width of the FRD is $1.2 \mu\text{sec}$ or not.

2.5 Indication Circuit

The life of a nixie tube is approximately a little more than 30,000 hours, and if it passes its lifetime, it partially indicates the numerals and the tube wall becomes coated which causes a dimmer illumination.

Since the discharge current controls the lifetime of the nixie tube, its flow must be less than 12mA . So, adjust the discharge current in high voltage circuit to be 12mA as specified in the power supply circuit. (The voltage is about 200V .)

Note:

Never change the nixie tubes with a different maker because the illumination and lifetime is different according to the discharge current.

Be careful not to touch the high voltage circuit or to short-circuit with other power supply.

2.6 Power Supply Circuits

The following four power supply are used in this calculator.

Main power	+5.3V	1.0A
Auxiliary power	-4.5V	
Nixie tube	+200V	12mA

1. +5.3V

This voltage is mainly used for the arithmetic circuit and it is regulated by constant voltage circuit. So, its voltage fluctuation allowance is within $5.3\text{V} \pm 0.1\text{V}$ for the AC rated input voltage. When the input voltage changes by $\pm 10\%$ for more than AC 200V rated voltage and by $+10 \sim -15\%$ for less than AC 200V rated voltage, then this voltage must be within $+5.3 \sim \pm 0.4\text{V}$.

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2. -4.5V

This voltage which is stabilized by the zener diode, is also used for the read amplifier and to stabilize the main power. This voltage must be within $-4 \sim -5.4V$ which is the zener voltage.

3. +200V

This voltage is used for the nixie tube circuit and is not regulated, so that the discharge current flows at 12mA.

2.7 Keyboard

1) Key

The reed switch is operated by the movement of the magnets which are attached to the key. Therefore, the positions of the magnets and reed switch are very important.

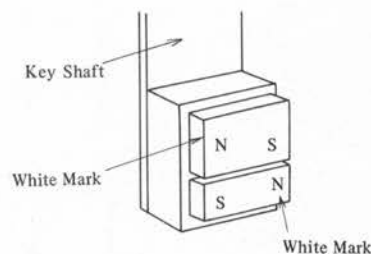
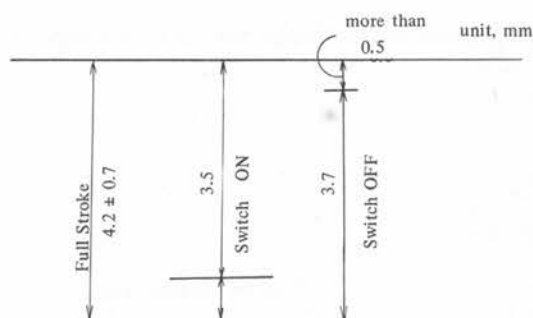


Fig. 5-7 Movement of the Key Switch

It is necessary to adjust the positions of the reed switch and the distance of the magnets, so that they correctly operate as in the above Fig. 5-7. The reed switch must be attached in parallel to the magnets.

2) Magnet

The large and small magnets must be of reverse polarity to each other. The magnets of keys which adjoin each other must be of reverse polarity. This is because if the magnets of each key are installed with the same polarity together, then the magnetic force of them becomes weaker, so the reed switch will not operate properly.

The correct polarity of the magnets is as shown Fig. 5-8.

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HOW TO REPAIR 8

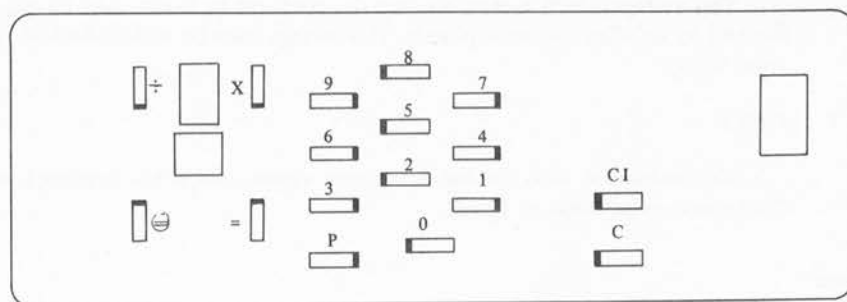


Fig. 5-8 Polarity of Magnets

2 8 Decimal Point Switch

If the affixed point position is desired to be change, then it is necessary to change the terminal circuit of undermentioned IC.

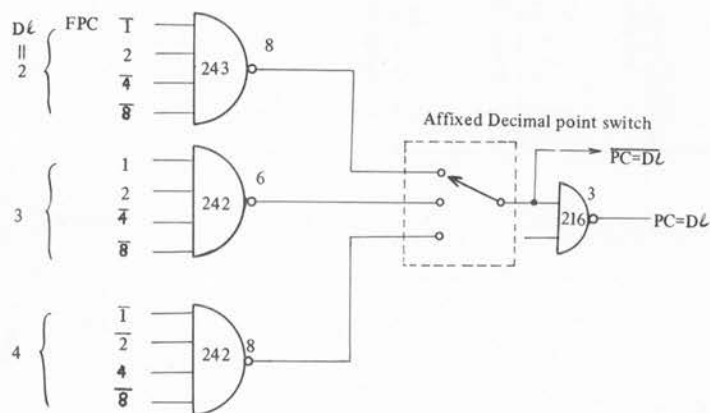


Fig. 5-9 Affixed Decimal Point Dial Circuit

MONROE 920

HOW TO REPAIR 9

3. Trouble-Shooting

3.1 Initial Checking Points

When any fault occurs, it is very important to always carefully examine its symptoms or conditions to find the proper current and the suitable remedial measure for it.

In repairing, it is necessary to confirm at first whether the following items are correct or not.

- 1) Are the AC input of DC output voltages normal?
- 2) Do the timing pulse generators operate properly?
- 3) Is KST signal emitted correctly?

The following are the detailed explanation of the trouble-shooting of the indicator, data, decimal point and sign after all the above mentioned have been examined to be correct.

3.2 Indicator

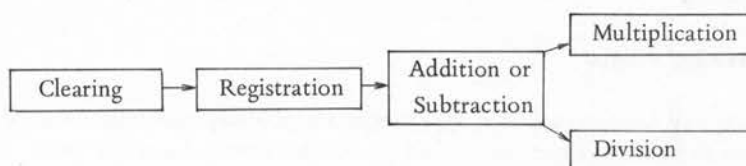
- (1) Digit in indicator does not light up.
 - (a) No digits in indicator light up.
Do the anodes of each digit receive a high voltage pulse?
Are the timing counters operate correctly?
 - (b) No figure of one digit lights up.
Does the anode of the digit receive a high voltage pulse?
Is the drive transistor, transformer or nixie tube normal?
 - (c) Certain figure or figures of the numerals do not light up.
Is indication decoder normal?
Do the cathode or cathodes receive a signal?
 - (d) Certain figure in certain digit or digits do not light up.
Do the cathode or cathodes receive its signal?
 - (e) Decimal point does not light up.
Does the anode receive a high voltage pulse?
Does the cathode of the nixie tube receive a LP pulse?
Is the point light-up transistor normal?
 - (f) Overflow lamp does not light up.
Does the lamp receive a high voltage?
Is FOF normal?
Is the light-up transistor normal?

3.3 Data

In trouble-shooting of the data, it is assumed that the previous calculation or calculations operate properly; therefore in the trouble-shooting of the data for multiplication and division, first confirm whether the operations for indicator clearing, registration, addition or subtraction can be done or not.

HOW TO REPAIR 10

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(1) No clearing indicator

- (a) Pressing **C** or **CI** key does not clear the indicator.
 - Does K ($\overline{C} + \overline{CI}$) signal become "0"?
 - Do GW1 and GSD close?
 - Is FSD or FID reset?

(2) No registration

- (a) No registration of numeric.
 - Is the key ST normal?
 - Is TB0 signal emitted?
 - Is CC normal?
 - Does FSD operate properly and a signal emit from GW1?
- (b) Only 1st digit registers.
 - Does the signal of the 1st digit enter FSD from G-SD?
- (c) Wrong numeral is registered.
 - Are W1, W2, W3 and W4 normal?
 - Is the numeral selection circuit or signal normal?
- (d) Figure appears in all digits when entering the first digit.
 - Are the trigger circuits or signals of W1 ~ W4 normal?

(3) No addition or subtraction

- (a) Answer is always 0.
 - Is CC normal?
 - Does the answer enter A0 register at CC4?
 - Is the addition of A0+B done at CC7 correctly?
 - Where does the data of B register disappear in the circuit?

(4) No multiplication

- (a) No answer is indicated.
 - Is CC normal?
 - Is there an answer in A2 register at CC4?
 - Does the subtraction of A0MSD-1 operate correctly?
 - Does the addition of A1+B operate at SCT1 of CC6?
 - Are FN and FG normal?
 - Does PC count at CC5?

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- (b) Erroneous multiplication.
 - Is FMLT normal?
 - Do the decimal points coordinate correctly?
 - Is CC normal?
- (c) No constant multiplication.
 - Is there a $\boxed{K}$ key signal?
 - Are FG and M + D "1" when the first calculation finishes?
- (d) Constant multiplicand changes.
 - Does $\overline{G-Y}$ close after the registration of the second multiplier?
- (5) No division
 - (a) Data does not shift to the affixed dial position.
 - Is CC1 signal emitted at the proper timing?
 - Is $\overline{G-SD}$ open at CC1?
 - (b) Erroneous division.
 - Is CC normal?
 - Is there an answer in A2 register at CC4?
 - Do FN and FG operate properly?
 - Does PC count at CCs?
 - Do the operations (A1-B) & (A2+1) operate correctly?
- (6) Decimal point
 - (a) No decimal point coordination.
 - Does the signal of FPC come to the dial?
 - Is the signal of PC=D1 normal?

RECEIVED 250

THE OLD CALCULATOR MUSEUM

1000 1000 1000

1000 1000 1000

1000 1000 1000

1000 1000 1000

1000 1000

1000 1000 1000

1000 1000 1000

1000 1000

1000 1000

1000

1000 1000 1000

1000 1000 1000

1000 1000

1000 1000 1000

1000 1000

1000 1000 1000

1000 1000 1000

1000 1000

RECEIVED 250

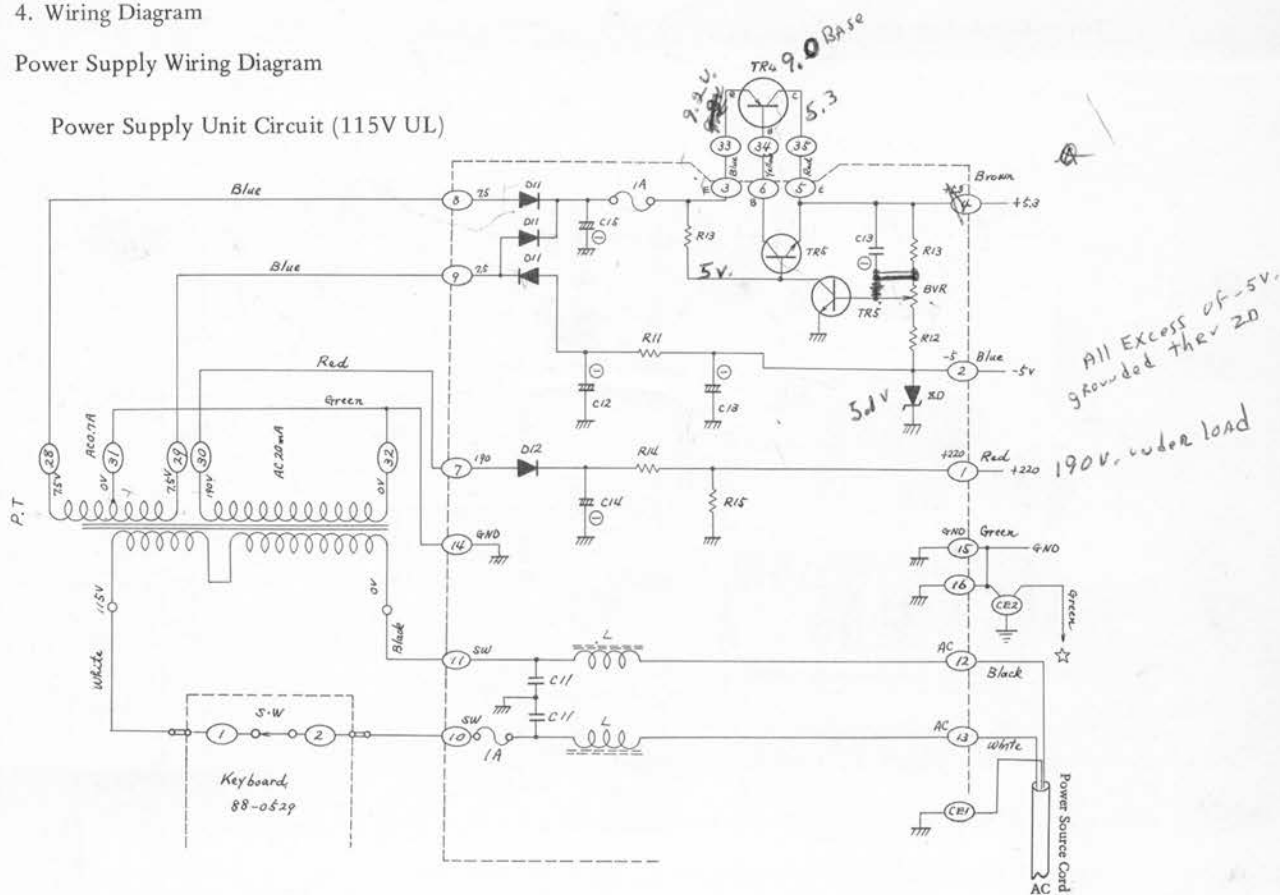
MONROE 920

HOW TO REPAIR 13

4. Wiring Diagram

Power Supply Wiring Diagram

Power Supply Unit Circuit (115V UL)

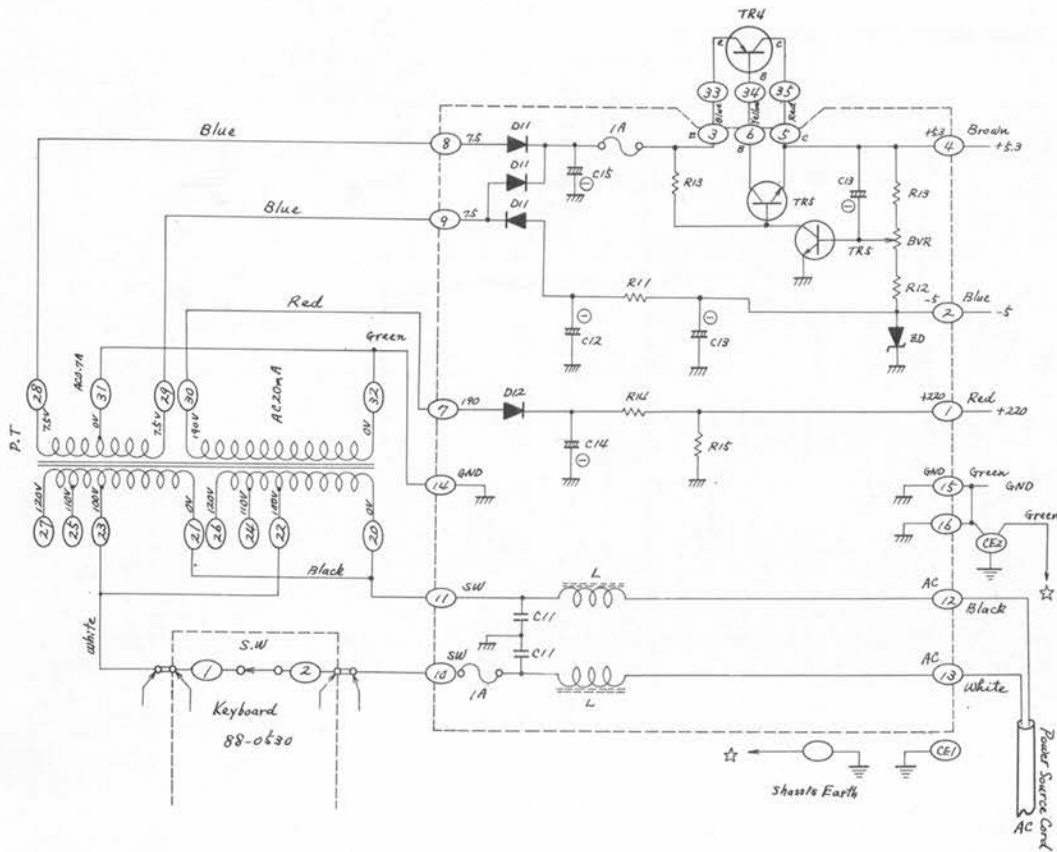


No.	Nomen.	Element	Q'ty	Part No.	Except UL
1	R11	27Ω 2W	1	X64-2116	UL
2	R12	470Ω ¼W	1	X64-0268	Except UL
3	R13	1KΩ ¼W	2	X64-0386	UL
4	R14	3.9KΩ 2W	1	X64-2314	Except UL
5	R15	200KΩ ¼W	1	X64-0585	UL
6	C12	220μF 15V	1	X63-3571	Except UL
7	C13	33μF 10V	2	X63-3089	UL
8	C14	5μF 350V	1	X63-3099	Except UL
9	C15	2000μF 10V	1	X63-3083	UL
10	C11	1000pF 220V	2	X63-2018	Except UL
11	D11	V0-3C	3	X65-5542	UL
12	D12	V0-6G	1	X65-5044	Except UL
13	ZD	AW01-05	1	X65-5544	UL
14	TR4	2SB337	1	X65-6043	Except UL
15	TR5	2SD77	2	X65-6525	UL
16	BVR	1KΩ (B)	1	X64-4353	Except UL
17	L	1.2mH	2	X62-1502	UL
18	1A	1A	2	X62-6797	Except UL
19	P.T.	Power Trans.	1	X61-1104	UL
20	SW	Power Switch	1	X62-0415	Except UL
21		Fuse Holder	1	X62-6796	UL
22	C11	Ceramic C	1	X63-2011	UL
23	P.T.	Power Trans-	2	X61-1117	Except UL
24	*1A	Fuse		X62-6606	UL

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HOW TO REPAIR 14

Power Supply Unit Circuit (Except UL) *Export only*

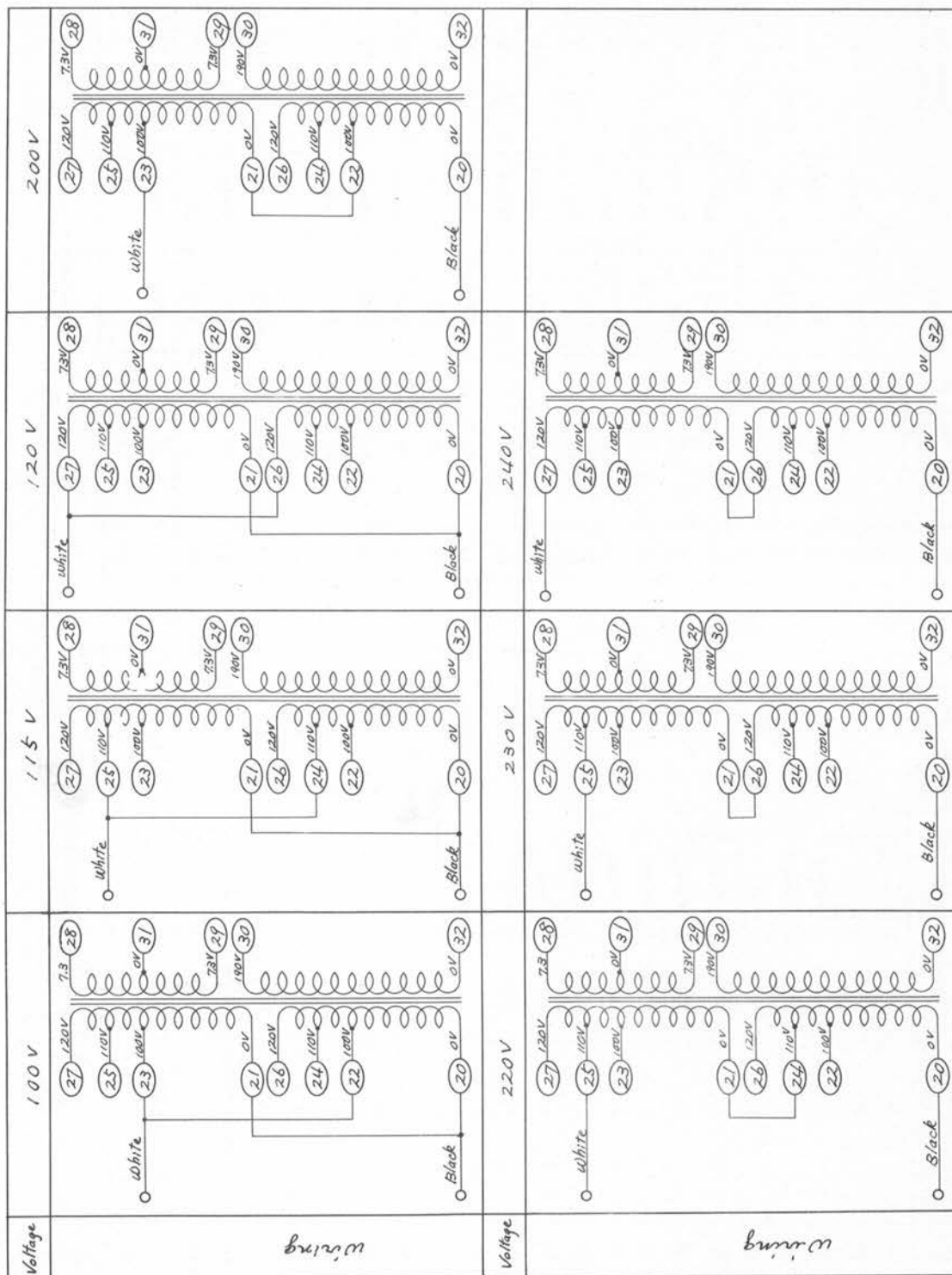


No.	Nomen.	Element	Q'ty	Part No.	Notes
1	R11	Resistor	1	X64-2116	Except UL
2	R12	"	1	X64-0268	UL
3	R13	"	2	X64-0386	Except UL
4	R14	"	1	X64-2314	UL
5	R15	"	1	X64-0585	UL
6	C12	Condenser	1	X63-3571	Except UL
7	C13	"	2	X63-3089	UL
8	C14	"	1	X63-3099	UL
9	C15	"	1	X63-3083	Except UL
10	C11	"	2	X63-2018	UL
11	D11	Diode	3	X65-5542	Except UL
12	D12	"	1	X65-5044	UL
13	ZD	Zener Diode	1	AW01-05	Except UL
14	TR4	Transistor	1	X65-5544	UL
15	TR5	"	2	X65-6043	UL
16	BVR	V.R.	1	X65-6525	Except UL
17	L	Fitter Choke	1	X64-4353	UL
18	1A	Fuse	2	X62-1502	UL
19	P.T.	Power Trans.	1	X62-6797	Except UL
20	SW	Power Switch	1	X61-1104	UL
21			1	X62-0415	UL
22	C11	Fuse Holder	1	X62-6796	Except UL
23	P.T.	Ceramic C	2	X63-2011	UL
24	*1A	Power Trans-former	1	X61-1117	UL
		Fuse		X62-6606	Except UL

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HOW TO REPAIR 15

Power Transformer Terminal Diagram *Export only*



MONROE 920**HOW TO REPAIR 16**

Terminal Destination (Wiring Unit, Arithmetic Card ↔ Indication Card)

No.	Terminal No. of Indication Card	Signal	Color	Destination Arithmetic Card
1				
2	2	$\overline{W4}$	Yellow	4
3	3	$\overline{W2}$	Orange	2
4	4	$\overline{G-SD}$	Pink	9
5	5	M	Purple	C
6	6	$\overline{FCA}$	Grey	10
7	7	CA	Brown	E
8	8	TD15	Yellow	S
9	9	$\overline{G-FCA}$	Blue	V
10	10	LP'	Grey	3
11	11	FOF	Brown	18
12	12	S	White	B
13	13	KEY OK	Blue	6
14	14	$\overline{CA}$	Black	F
15	15	TS3	Orange	H
16	16	$\overline{TB0}$	Purple	12
17	17	TB0	Green	13
18	18			
19	19	CPR	Red	15
20	20	$\overline{FBU}$	White	K
21	21 For Power Supply	+5V	Brown	
22	22 For Power Supply	GND	Green	
23	23			

Indication Card, Parts Side

No.	Terminal No. of Indication Card	Signal	Color	Destination Arithmetic Card
24	A			
25	B			
26	C	$\overline{W3}$	Green	5
27	D	$\overline{W1}$	Pink	1
28	E	N	Red	D
29	F	$\overline{TD0}$	Blue	19
30	H	$\overline{BD0}$	Pink	7
31	J	BD0	Green	M
32	K	CP	Yellow	17
33	L	$\overline{G-W1}$	Orange	8
34	M	TD12~14	Red	R
35	N	SD4	Purple	11
36	P			
37	R			
38	S			
39	T			
40	U			
41	V	TS0	White	J
42	W	FBU	Grey	L
43	X For Power Supply	-4.5V	Blue	
44	Y For 21	+5V		
45	Z For 22	GND		
46				

Indication Card, Printed Side

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HOW TO REPAIR 17

Terminal Destinations Wiring Unit (Arithmetic Card ↔ Keyboard)

No.	Terminal No. of Arithmetic Card	Signal	Color	Destination Keyboard unit
1	1	GND	Green	GND
2	2	$\overline{\text{Key } =}$	Grey	K= -1
3	3	$\overline{\text{Key } \ominus}$	White	K $\ominus$ -1
4	4	$\overline{\text{Key } X}$	Yellow	KX-1
5	5	$\overline{\text{Key } \div}$	Green	K $\div$ -1
6	6	$\overline{\text{Key } C}$	Purple	KC - 1
7	7	$\overline{\text{Key } CI}$	Orange	KCI-1
8	8			
9	9	$\overline{\text{Key } P}$	Blue	KP-1
10	10	$\overline{\text{Key } K}$	Blue	KK-2
11	11			
12	12			
13	13			
14	14			

Arithmetic Card, Parts Side

No.	Terminal No. of Arithmetic Card	Signal	Color	Destination Keyboard unit
15	A	$\overline{\text{Key } 9}$	White	K9-1
16	B	$\overline{\text{Key } 8}$	Grey	K8-2
17	C	$\overline{\text{Key } 7}$	Purple	K7-2
18	D	$\overline{\text{Key } 6}$	Blue	K6-1
19	E	$\overline{\text{Key } 5}$	Green	K5-2
20	F	$\overline{\text{Key } 4}$	Yellow	K4-2
21	H	$\overline{\text{Key } 3}$	Orange	K3-1
22	J	$\overline{\text{Key } 2}$	Red	K2-2
23	K	$\overline{\text{Key } 1}$	Brown	K1-2
24	L	$\overline{\text{Key } 0}$	Black	K0-2
25	M	$\overline{DL=PC}$	Green	PS-2
26	N	DLW1	Black	PS-8
27	P	DLW2	Red	PS-3
28	R	DLW3	Yellow	PS-1

Arithmetic Card, Printed Side

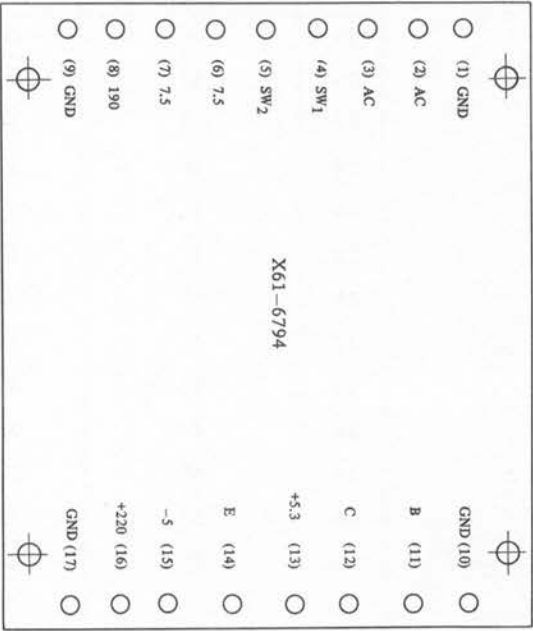
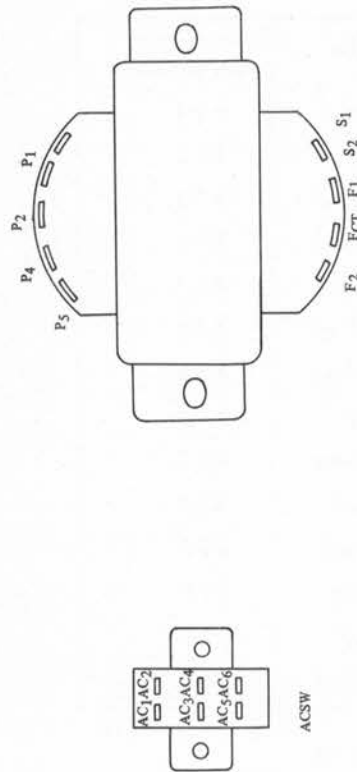
MONROE 920

HOW TO REPAIR 18

Power Supply Assembly

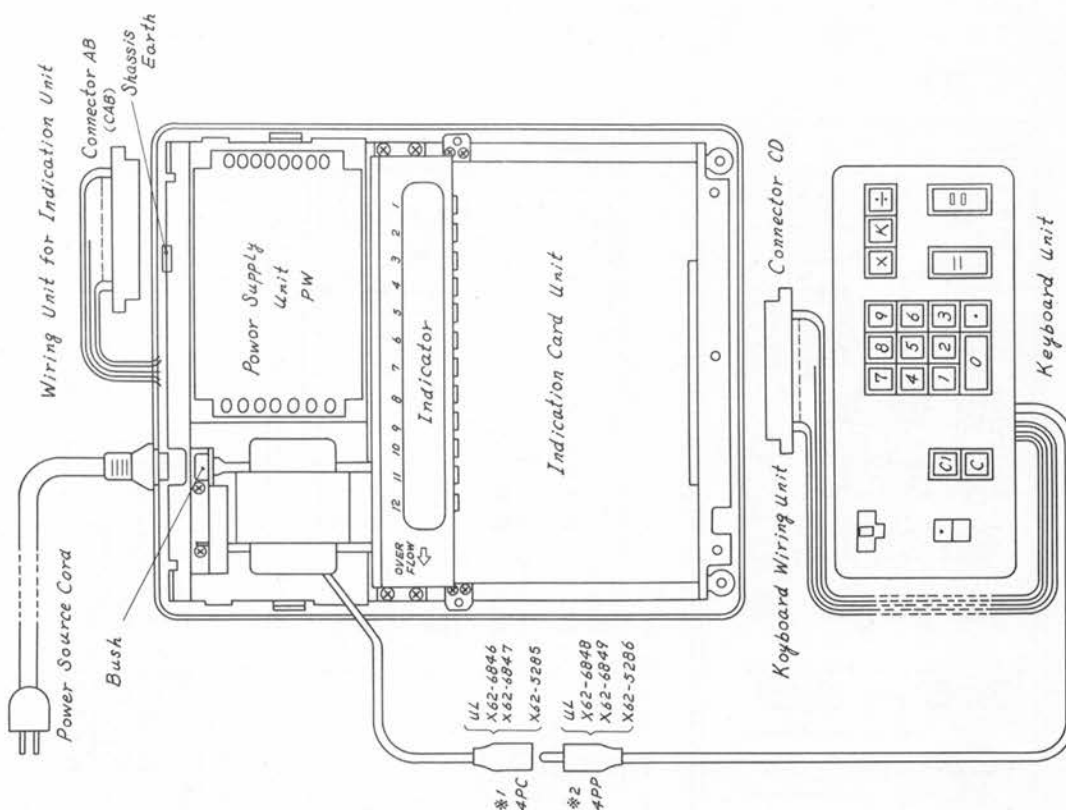
Terminal No.	Signals	Destination	Color
1	AC100V.SW	AC plug	White
2	AC 7.5V	F1	Blue
3	AC 7.5V	F2	"
4	AC190V	S2	Red
5	SW	AC4	White
6	AC100V	AC plug	Black
7	G	P1,S1,FCT	Green
8	G	1-17	Black
9	-Vcc	1-07	Blue
10	E	2SB337-E	Blue
11	+220V	1-01	Red
12	B	2SB337-B	Yellow
13	C	2SB337-C	Red
14	+Vcc	1-19	Brown

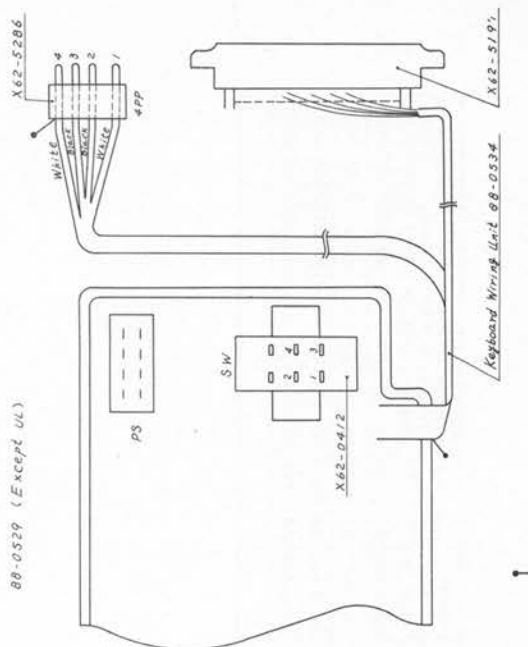
Terminal No.	Signals	Destination	Color
AC3	AC 100V	AC plug 0-1	White
AC4	AC 100V	AC plug	Black
AC5		P2	"
AC6		P1	White



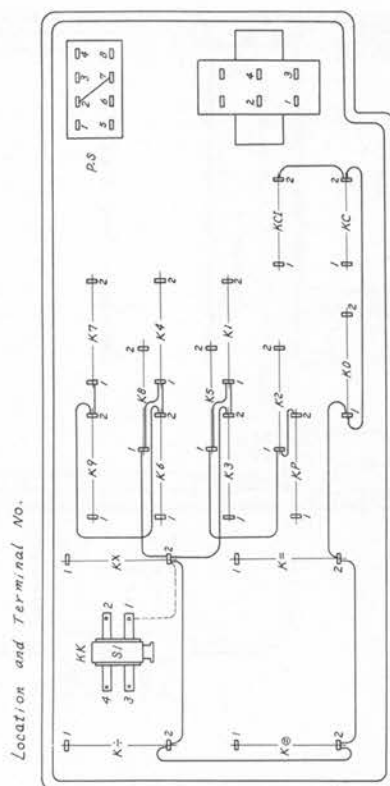
MONROE 920

No.	Voltage	Power Supply Unit No.	Keyboard Unit No.	For Indication Card Wiring Unit No.	Forboard Wiring Unit No.	Arithmetic Card Unit No.	Indication Card Unit No.
1	115V	88-0446	88-0530	88-0533	88-0535	88-0528	88-0527
2	220V	88-0447	88-0529	88-0532	88-0534	88-0528	88-0527
3	240V	88-0448	88-0529	88-0532	88-0534	88-0528	88-0527
4	115V	88-0449	88-0529	88-0532	88-0534	88-0528	88-0527
5							





Keyboard Unit	08-0529 (Except UL)
Keyboard Unit	08-0530 (UL)



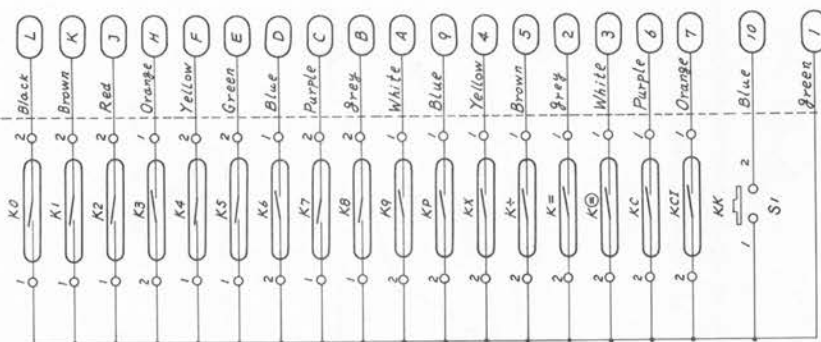
Terminal Wiring

No	Terminal No	Destination
1	KX-2	KX-2, K7-2, K@-2, K=-2, K0-1, KC-2, KC1-2
2	KD-2	KP-2, K2-1, K5-1, K1-1, K3-2, KX-2, K8-1.
3	S1-1	K4-1, K6-2, K9-2, K7-1.
4	DS-2	Keyboard Wiring Unit S1-1, KX-2

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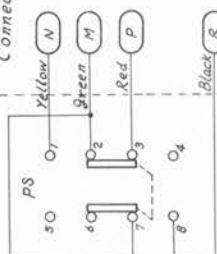
Wiring Unit { 88-0534 (Except ul)
88-0534 For ul

Connector CD

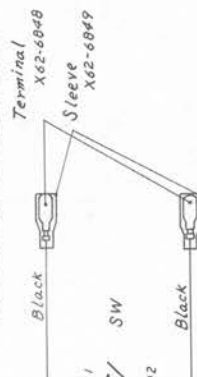


Keyboard Unit Wiring

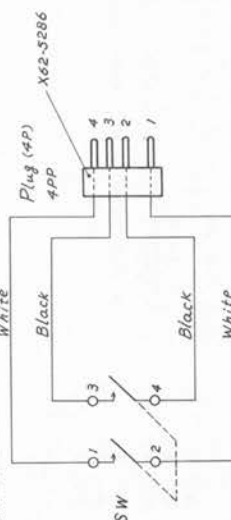
Affixed Decimal Point Switch
Connector CD



UL Power Switch
88-0530
X62-0415



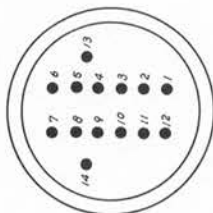
Power Switch (Except ul)
88-0529
X62-0412



Unit No.	
88-0529	220 V
88-0530	240 V
	115 V
	UL 115 V

MONROE 920

View from face

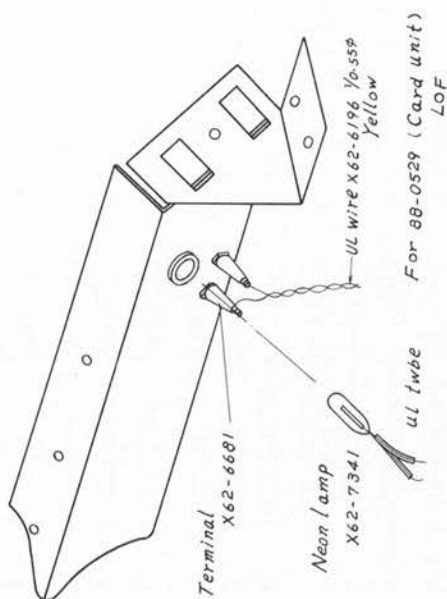
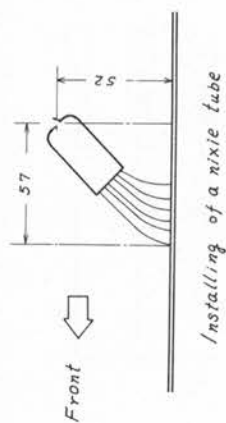
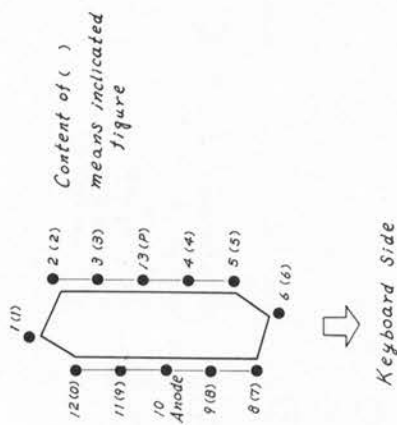


Terminal No. of a nixie tube

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Figure (Numeral)	1	2	3	4	5	6	7	8	9	0	P			

* Pin No. 7 is not used, must cut the Pin

Terminal No. of nixie tube in Printed circuit (Parts 5101e)



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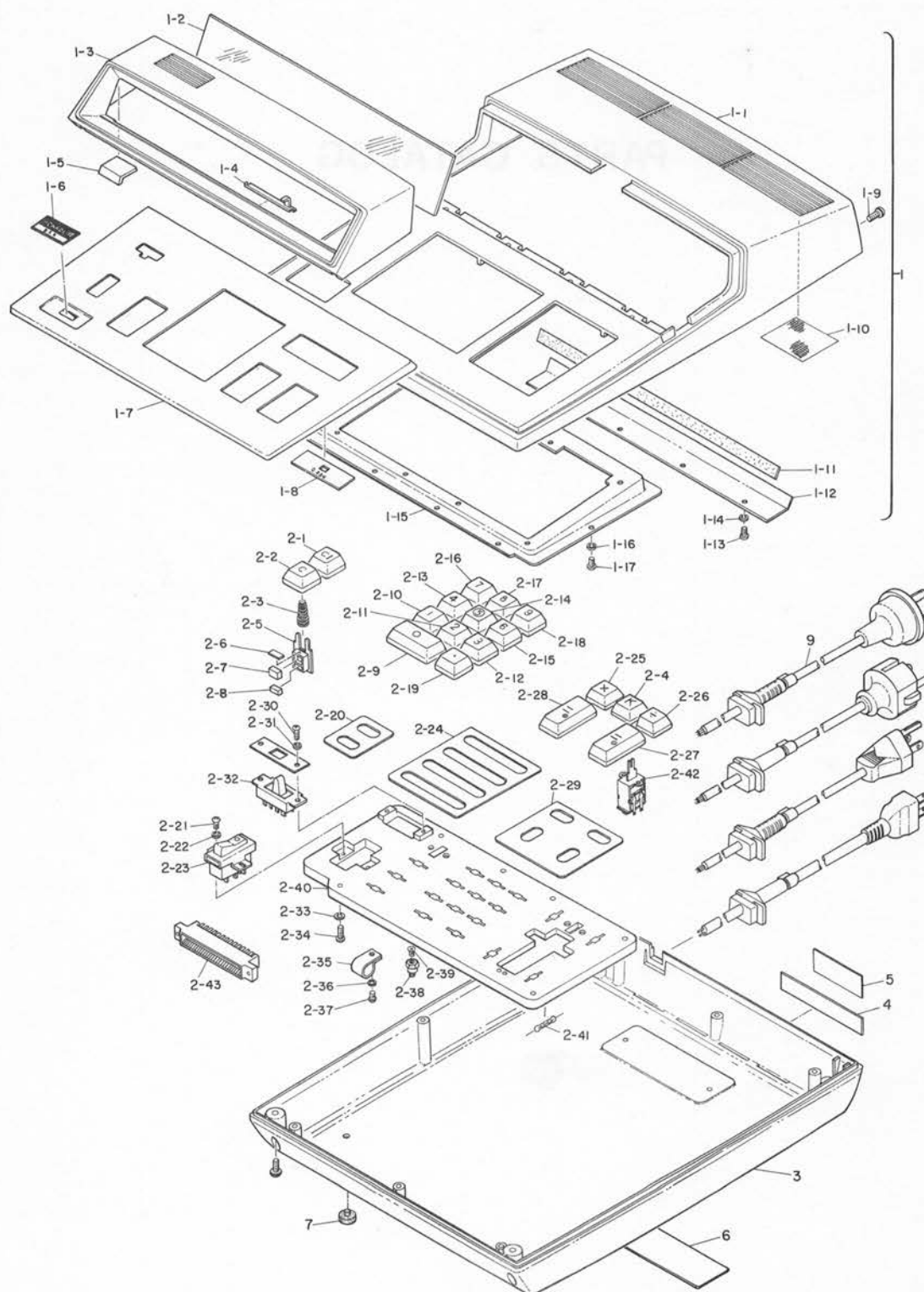
PARTS CATALOG

MONROE 920

PARTS CATALOG 2

1. Casing

CASING

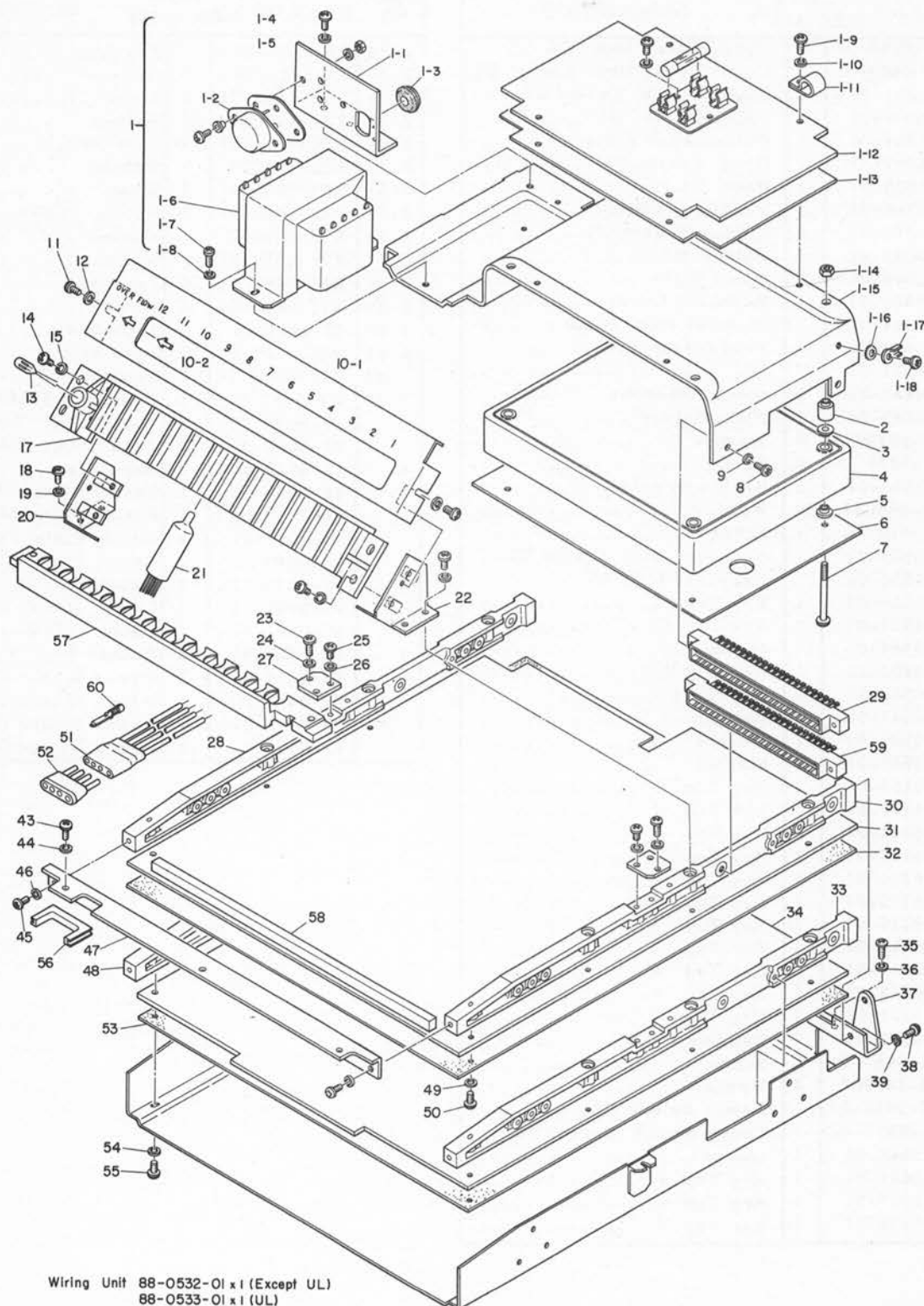


MONROE 920**PARTS CATALOG 3****CASING**

KEY NO.	PART NO.	UNITS PER ASS'Y	DESCRIPTION
1 ..	Y50-0399-01		Upper Cover Unit UL
	Y50-0400-01		Upper Cover Unit Except UL
1-1.	83-6093-01 .	1	Upper Cover Except UL
	83-6094-01 .	1	Upper Cover UL
1-2.	83-5811-02 .	1	Polarization Plate
1-3.	83-6097-01 .	1	Hood Except UL
	83-6098-01 .	1	Hood UL
1-4.	83-5560-04 .	4	3 digits Indicator
1-5.	83-6062-01 .	2	Holder Except UL
	83-6063-01 .	2	Holder UL
1-6.	96-8044-01 .	1	Name Plate
1-7.	83-6480-01 .	1	Keyboard Cover
1-8.	96-8001-01 .	1	Decimal Point Plate
1-9.	X07-400807	4	Bind Screw
1-10.	83-5571-02	7	Net
1-11.	83-5567-02	1	Shock Absorber
1-12.	83-5563-04	1	Plate Holder
1-13.	X32-103027	4	Washer
1-14.	X71-5227 ..	4	Screw
1-15.	83-5562-01 .	1	Keyboard Holder
1-16.	X32-103027	10	Washer
1-17.	X71-5227 ..	4	Screw
2 ..	88-0529-01		Keyboard Unit Except UL ..
	88-0530-01		Keyboard Unit UL
2-1.	83-6120-01 .	1	Key Top CI
2-2.	83-6119-01 .	1	Key Top C
2-3.	83-5648-01 .	17	Spring
2-4.	83-5402-01 .	1	Key Top K
2-5.	89-0542-01 .	17	Key Shaft
2-6.	83-5647-01 .	17	Damper
2-7.	83-5649-01 .	17	Magnet
2-8.	83-5650-01 .	17	Magnet
2-9.	83-6101-01 .	1	Key Top 0
2-10.	83-6111-01 .	1	Key Top 1
2-11.	83-6112-01 .	1	Key Top 2
2-12.	83-6113-01 .	1	Key Top 3
2-13.	83-6114-01 .	1	Key Top 4
2-14.	83-6110-01 .	1	Key Top 5
2-15.	83-6115-01 .	1	Key Top 6
2-16.	83-6116-01 .	1	Key Top 7
2-17.	83-6117-01 .	1	Key Top 8
2-18.	83-6118-01 .	1	Key Top 9
2-19.	83-6121-01 .	1	Key Top
2-20.	83-5646-02 .	1	Damper
2-21.	X71-5567-01	2	Screw
2-22.	X32-103027 .	2	Washer
2-23.	X62-0412-01	1	Power Switch UL
	X62-0415-01	1	Power Switch Except UL
2-24.	83-5645-02 .	1	Damper
2-25.	83-6471-01 .	1	Key Top x
2-26.	83-6107-01 .	1	Key Top ÷
2-27.	83-6106-01 .	1	Key Top ⊖

KEY NO.	PART NO.	UNITS PER ASS'Y	DESCRIPTION
2-28.	83-6102-01 .	1	Key Top = ...
2-29.	83-5644-02 .	1	Damper
2-30.	X71-5217-01	2	Screw
2-31.	X32-103027	2	Washer
2-32.	X62-6411-01	1	Slide Switch
2-33.	X32-103027	7	Washer
2-34.	X07-300807	7	Screw
2-35.	X62-6863-01	1	Wiring Holder
2-36.	X32-103027	1	Washer
2-37.	X71-5567-01	1	Screw
2-38.	X62-6795-01	34	Terminal
2-39.	X71-5240-01	2	Screw
2-40.	83-6471-01	1	Keyboard
2-41.	X62-1104-01	17	Reed Switch
2-42.	X62-0106-01	1	Push Switch
2-43.	X3-5197-01 .	1	Connector (28P)
3 ..	83-6095-01 .	1	Base Cover Except UL ..
	83-6096-01 .	1	Base Cover UL
4 ..	96-8045-01 .	1	Back Plate
5 ..	96-8046-01 .	1	Rating Plate UL
	96-8047-01 .	1	Rating Plate 220V
	96-8048-01 .	1	Rating Plate 240V
	96-8049-01 .	1	Rating Plate 115V
6 ..	97-9039-01 .	1	Label 115V
	97-9040-01 .	1	Label 240V
	97-9041-01 .	1	Label 220V
7 ..	83-5566-01 .	2	Rubber Pad
8 ..	89-0499-01 .	1	Power Source Cord 240V
	89-0498-01 .	1	Power Source Cord 220V
	89-0497-01 .	1	Power Source Cord UL .
	89-0500-01 .	1	Power Source Cord 115V

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Wiring Unit 88-0532-01 x1 (Except UL)
88-0533-01 x1 (UL)

MONROE 920**PARTS CATALOG 5****ARITHMETIC UNIT**

KEY NO.	PART NO.	UNITS PER ASS'Y	DESCRIPTION
1 ..	88-0446-02 ..	...	Power Supply Unit UL.....
	88-0447-02 ..	...	Power Supply Unit 220V.....
	88-0448-02 ..	...	Power Supply Unit 240V.....
	88-0449-02 ..	...	Power Supply Unit 115V.....
1-1.	83-5640-03 ..	1	Transistor Holder
1-2.	X65-6043-01..	1	Transistor 2SB337
1-3.	X62-6816-01..	1	Bush
1-4.	X07-300807 ..	2	Screw
1-5.	X32-103027 ..	2	Washer
1-6.	X61-1104-01..	1	Power Transformer Except UL
	X61-1117-01..	1	Power Transformer UL.....
1-7.	X07-300807 ..	2	Screw
1-8.	X32-103027 ..	2	Washer
1-9.	X07-300807 ..	4	Screw
1-10.	X32-103027 ..	4	Washer
1-11.	X62-6863-01..	1	Wiring Holder
1-12.	88-0423-01 ..	1	Power Supply Card UL
	88-0424-03 ..	1	Power Supply Card Except UL
1-13.	83-5783-02 ..	1	Fiber
1-14.	X31-403357 ..	4	Washer
1-15.	83-5639-01 ..	1	Power Supply Chassis
1-16.	X71-5247-01 ..	1	Washer
1-17.	X62-6741-01 ..	1	Earth Terminal
1-18.	X71-5249-01 ..	1	Screw
2 ..	83-5753-01 ..	4	Collar
3 ..	83-5641-01 ..	4	Collar
4 ..	X61-3020-01..	1	Delay Line
5 ..	83-5641-01 ..	4	Collar
6 ..	83-5799-01 ..	1	Shield Panel
7 ..	83-5669-01 ..	4	Screw
8 ..	X71-5227-01 ..	2	Screw
9 ..	X32-103027-01	2	Washer
10 ..	Y50-0339-01		Indicator Frame
10-1.	83-5633-02 ..	1	Frame
10-2.	83-4957-01 ..	1	Acryl ←
11 ..	X07-300807-01	2	Screw
12 ..	X32-103027-01	2	Washer
13 ..	X62-7341-01 ..	1	Neon Lamp
14 ..	X07-300807-01	4	Screw
15 ..	X32-103027-01	4	Washer
16 ..			
17 ..	83-5782-03 ..	1	Nixie Tube Holder
18 ..	X71-5227-01 ..	4	Screw
19 ..	X32-103027-01	4	Washer
20 ..	83-5636-02 ..	1	Angle
21 ..	X65-4004-01 ..	12	Nixie Tube
22 ..	83-5635-02 ..	1	Angle
23 ..	X71-5564-01 ..	2	Screw
24 ..	X32-103027-01	2	Washer
25 ..	X71-5227-01..	4	Screw
26 ..	X32-103027-01	4	Washer
27 ..	83-5632-01 ..	2	Card Holder

KEY NO.	PART NO.	UNITS PER ASS'Y	DESCRIPTION
28	83-5628-01 ..	1	Card Frame
29	X62-5129-01 ..	1	Connector (44P)
30	83-5628-01 ..	1	Card Frame
31	88-0527-01 ..	1	Indication Card
32	83-5690-01 ..	1	Fiber
33	83-5628-01 ..	1	Card Frame
34	88-0528-01 ..	1	Arithmetic Card
35	X71-5564-01 ..	3	Screw
36	X32-103027-01	3	Washer
37	89-0538-01 ..	1	Shield Panel
38	X71-5227-01 ..	2	Screw
39	X32-103027-01	2	Washer
41	X32-103027-01	4	Washer
42	X71-5227-01 ..	4	Screw
43	X71-5564-01 ..	3	Screw
44	X32-103027-01	3	Washer
45	X71-5564-01 ..	2	Screw
46	X32-103027-01	2	Washer
47	83-5629-04 ..	1	Card Frame
48	83-5628-01 ..	1	Card Frame
49	X32-103027-01	6	Washer
50	X71-5564-01..	6	Screw
51	X62-5285-01..	1	4P Receptacle
52	X62-5286-01..	1	4P Plug
53	83-5800-02 ..	1	Fiber
54	X32-103027-01	2	Washer
55	X71-5227-01 ..	2	Screw
56	83-5821-02 ..	1	Bush
57	83-6104-01 ..	1	Nixie Holder
58	83-6105-01 ..	1	Holder
59	X62-5129-01..	1	Connector (44P)
60	X62-6848-01..	2	Fasten Terminal
* ..	88-0532-01 ..	1	Wiring Unit Except UL
* ..	88-0533-01 ..	1	Wiring Unit UL.....

MONROE 920

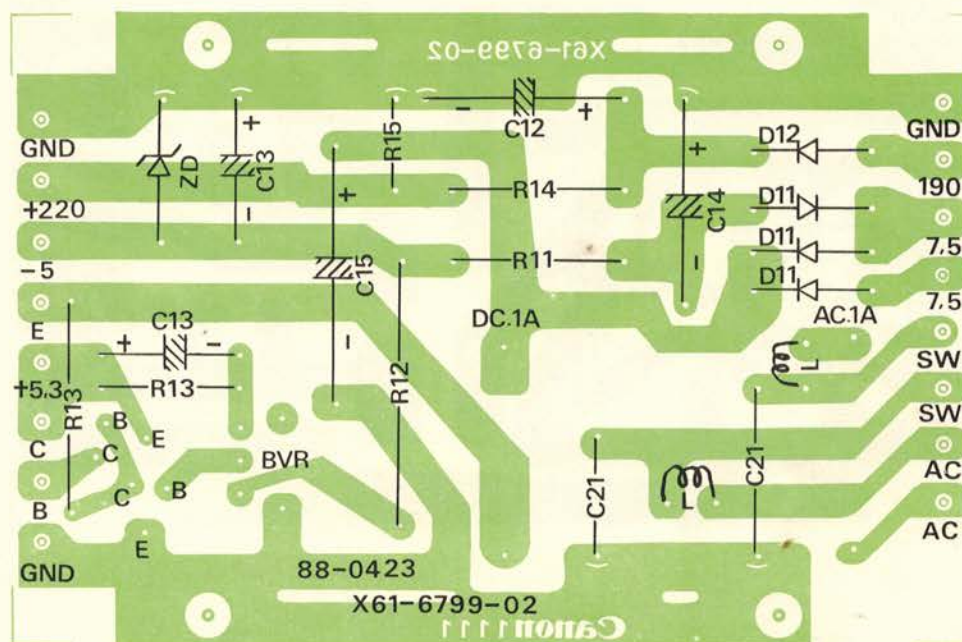
PARTS CATALOG 7

3. Cards

POWER SUPPLY CARD

3.1 Power Supply Card

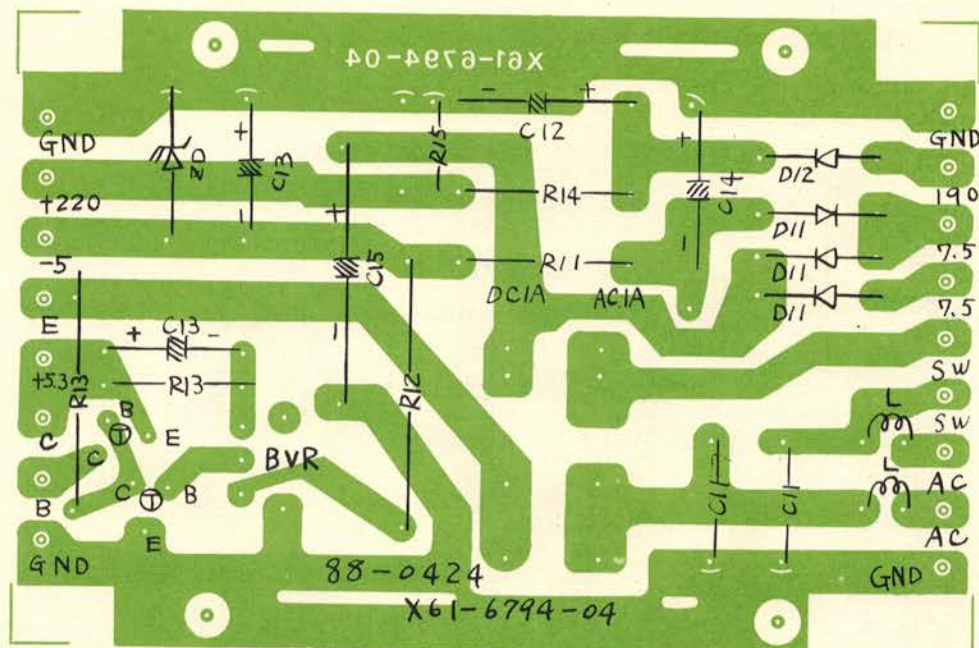
UL 0423



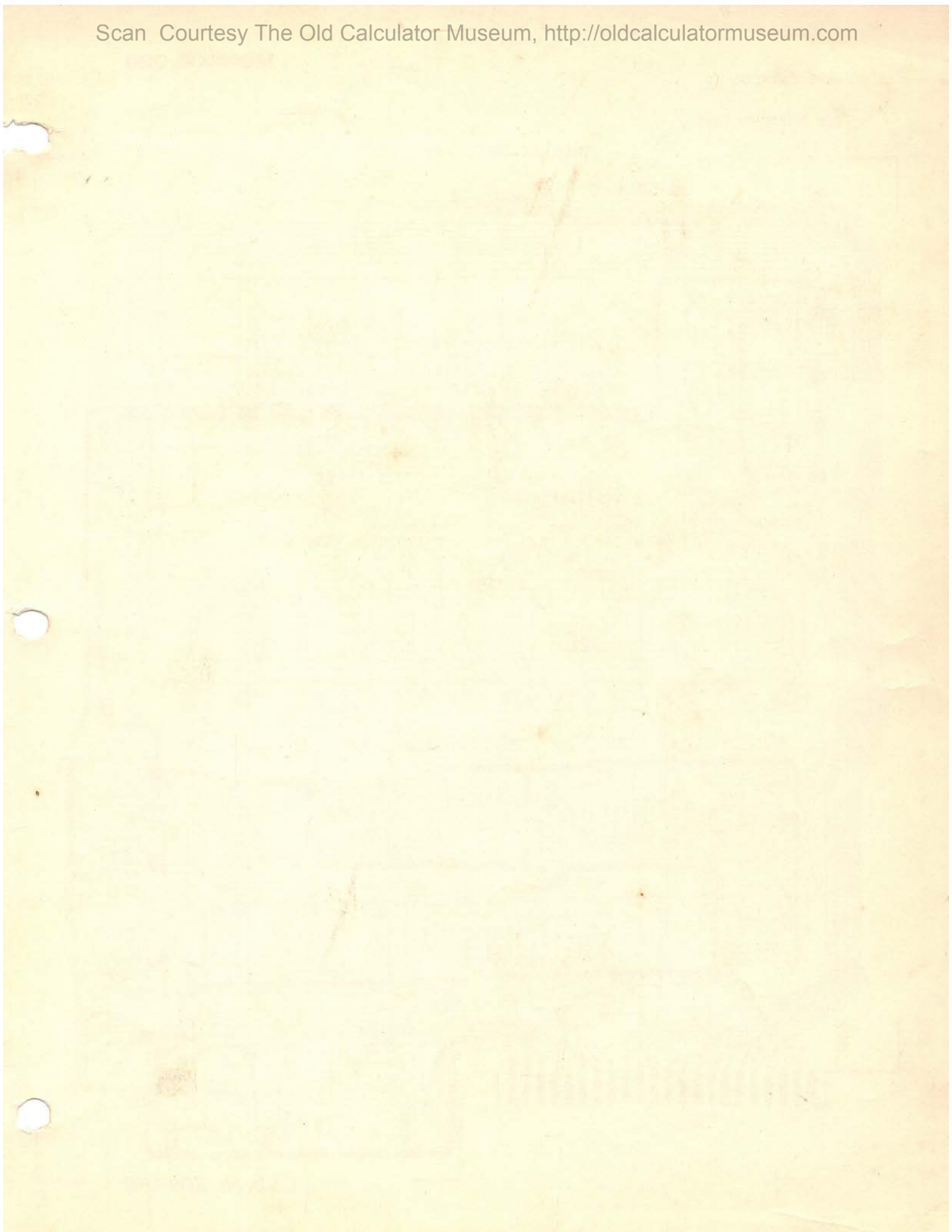
PARTS NO.	Q'ty	DESCRIPTION	REMARKS
X61-6799-01	1	Power Supply Card Printed Board	
X62-1502-02	2	Filter Chork Coil	1. 2mH
X62-6734-01	4	Terminal	
X62-6797-01	2	UL Fuse	1A
X63-2011-01	2	Ceramic Condenser 1000PF	
X63-3083-01	1	Chemical Condenser 2000μF 10V	
X63-3089-01	1	Chemical Condenser 30μF 10V	
X63-3099-01	1	Chemical Condenser 5μF 350V	
X63-3571-01	1	Chemical Condenser 200μF 15V	
X64-0268-01	1	Carbon Resistor 470Ω T 1/4	
X64-0386-01	1	Carbon Resistor 1KΩ T 1/4	
X64-0585-01	1	Carbon Resistor 200KΩ T 1/4	
X64-2116-01	1	Solid Resistor 27Ω	
X64-2314-01	1	Solid Resistor 3.9KΩ	
X64-4353-01	1	Variable Resistor 1KΩ (B)	
X65-5044-01	1	Diode V0-6G	
X65-5542-01	3	Diode V0-3C	
X65-5544-01	1	Zener Diode AW01-5G	
X65-6525-01	2	Transistor 2SD77	

PARTS CATALOG 8

Except UL 0424



PARTS NO.	Q'ty	DESCRIPTION	REMARKS
X61-6794-03	1	Power Supply Card Printed Board	
X62-1502-02	2	Filter Choke Coil	1.2mH
X62-6452-01	0.1m	Jumper Wire	
X62-6534-01	0.1m	Sleeve	
X62-6606-01	2	Fuse	1A
X62-6796-01	1	Fuse Holder	
X62-6735-01	17	Terminal	
X63-2018-01	2	Ceramic Condenser 1000PF	
X63-3083-01	1	Chemical Condenser 2000μF 10V	
X63-3089-01	1	Chemical Condenser 30μF 10V	
X63-3099-01	1	Chemical Condenser 5μF 350V	
X63-3571-01	1	Chemical Condenser 200μF 15V	
X64-0268-01	1	Carbon Resistor 470ΩT1/4	
X64-0386-01	1	Carbon Resistor 1KΩ T 1/4	
X64-0585-01	1	Carbon Resistor 200KΩ T 1/4	
X64-2116-01	1	Solid Resistor 27Ω	
X64-2314-01	1	Solid Resistor 3.9KΩ	
X64-4353-01	1	Variable Resistor 1KΩ (B)	
X65-5044-01	1	Diode V0-6G	
X65-5542-01	3	Diode V0-3C	
X65-5544-01	1	Zener Diode AW01-05	
X65-6525-01	2	Transistor 2SD77	

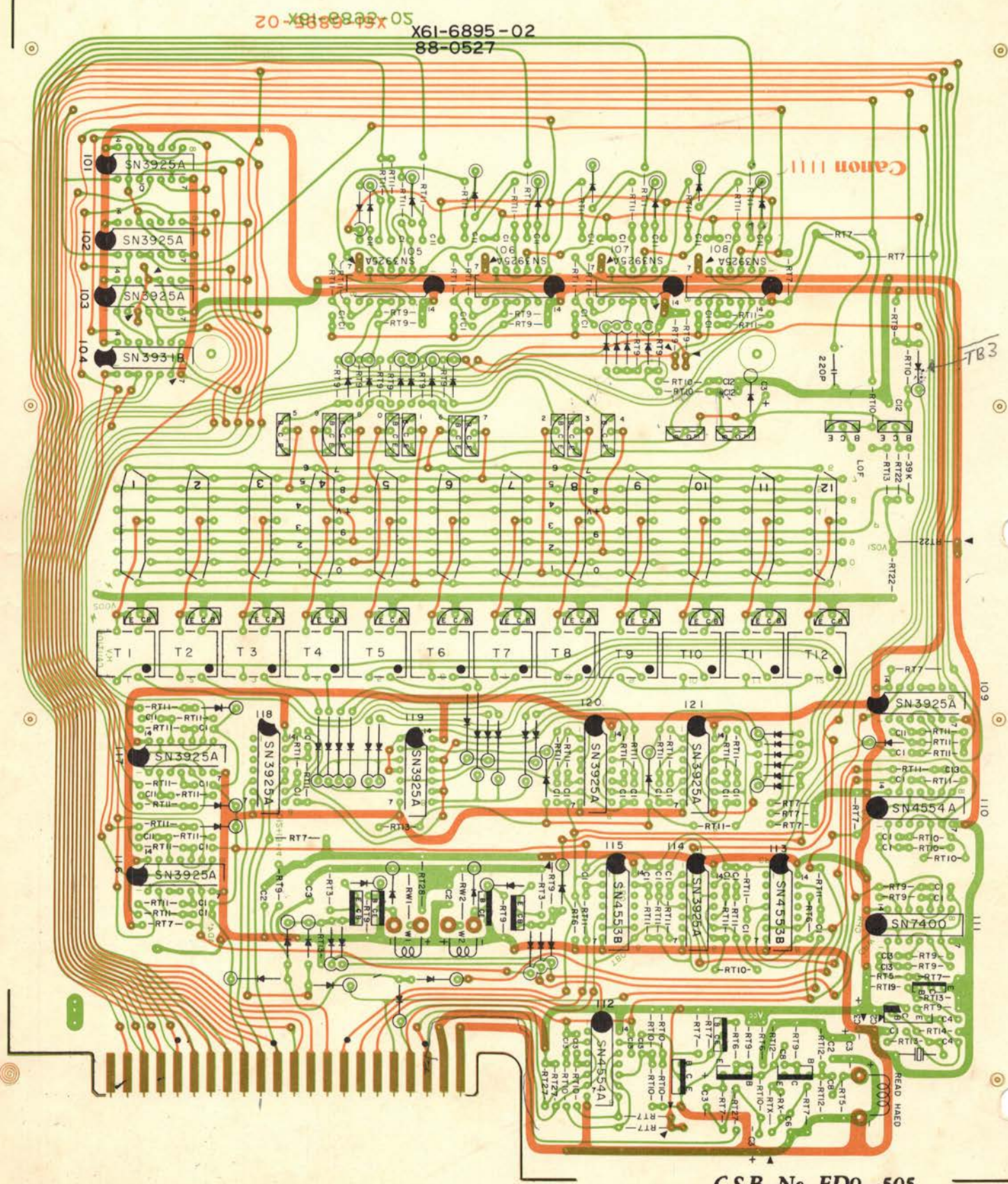


PARTS CATALOG 10

MONROE 920

3.2 Indication Card

INDICATION CARD



C.S.B. No. ED9-505

MONROE 920

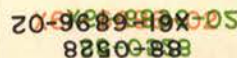
PARTS CATALOG 11

INDICATION CARD

PARTS NO.	Q'ty	DESCRIPTION	REMARKS
X61-6895-01	1	Indication Card Printed Board	
X61-1108-01	12	Drive Transformer	
X61-3019-01	1	Crystal	2MHz
X62-6531-01	0.9m	UL Tube	0.5φ
X62-6744-01	6	Terminal	1.6φ x 3.2BK
X62-7341-01	1	Neon Lamp	
X62-8706-01	2	Film Condenser 0.001μF	
X62-8707-01	1	Film Condenser 0.01μF	
X63-2009-01	40	Ceramic Condenser 47PF	
X63-2010-01	2	Ceramic Condenser 100PF	
X63-2012-01	3	Ceramic Condenser 4700PF	
X63-2014-01	6	Ceramic Condenser 33PF	
X63-2015-01	15	Ceramic Condenser 68PF	
X63-2024-01	1	Ceramic Condenser 220PF	
X63-2508-01	3	Ceramic Condenser 680PF	
X63-3089-01	6	Chemical Condenser 33μF 10V	
X64-0053-01	1	Carbon Resistor 4.7Ω T 1/2	
X64-0244-01	2	Carbon Resistor 470Ω T 1/8	
X64-0547-01	5	Carbon Resistor 220KΩ T 1/8	
X64-0548-01	1	Carbon Resistor 100KΩ T 1/8	
X64-0828-01	3	Carbon Resistor 1KΩ T 1/8	
X64-0829-01	2	Carbon Resistor 1.8KΩ T 1/8	
X64-0830-01	12	Carbon Resistor 2.7KΩ T 1/8	
X64-0831-01	1	Carbon Resistor 3.3KΩ T 1/8	
X64-0832-01	28	Carbon Resistor 5.6KΩ T 1/8	
X64-0833-01	15	Carbon Resistor 10KΩ T 1/8	
X64-0834-01	56	Carbon Resistor 22KΩ T 1/8	
X64-0835-01	3	Carbon Resistor 33KΩ T 1/8	
X64-0836-01	5	Carbon Resistor 56KΩ T 1/8	
X64-0840-01	2	Carbon Resistor 2.2KΩ T 1/8	
X64-0860-01	1	Carbon Resistor 15KΩ T 1/8	
X64-0127-01	1	Carbon Resistor 30Ω T 1/4	
X65-4004-01	12	Nixie Tube	
X65-5045-01	61	Diode ITT WG599	
X65-6044-01	10	Transistor 2SC641B	
X65-6058-01	26	Transistor 2SC780	
X65-7001-01	15	IC SN3925	
X65-7002-01	1	IC SN3931	
X65-7004-01	2	IC SN4554	
X65-7007-01	2	IC SN4553	
X65-7011-01	1	IC SN7400	

MONROE 920

ARITHMETIC CARD



MONROE 920**PARTS CATALOG 13****ARITHMETIC CARD**

PARTS NO.	Q'ty	DESCRIPTION	REMARKS
X61-6896	1	Arithmetic Card Printed Board	
X62-6531-01	0.8m	UL Tube	0.5φ
X62-8703-01	1	Film Condenser 0.1μF	
X63-2009-01	26	Ceramic Condenser 47PF	
X63-2012-01	1	Ceramic Condenser 4700PF	
X63-2015-01	8	Ceramic Condenser 68PF	
X64-0828-01	3	Carbon Resistor 1KΩ T 1/8	
X64-0832-01	17	Carbon Resistor 5.6KΩ T 1/8	
X64-0833-01	7	Carbon Resistor 1KΩ T 1/8	
X64-0834-01	35	Carbon Resistor 3.3KΩ T 1/8	
X64-0840-01	4	Carbon Resistor 2.2KΩ T 1/8	
X65-5045-01	76	Diode ITT WG-599	
X65-6044-01	1	Transistor 2SC641B	
X65-7001-01	17	IC SN3925	
X65-7002-01	10	IC SN3931	
X65-7003-01	6	IC SN3920	
X65-7004-01	10	IC SN4554	
X65-7007-01	2	IC SN4553	

