

United States Patent

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[54] DISPLAY SYSTEM USING A CATHODE-RAY TUBE

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Mar. 29, 1969 Japan.....44/23982

[52] U.S. Cl. 340/172.5, 340/324 A, 315/18

[51] Int. Cl. G05f 5/00, G05b 11/14, G06k 15/20

[58] Field of Search.....340/172.5, 324 A; 315/18, 22, 315/30

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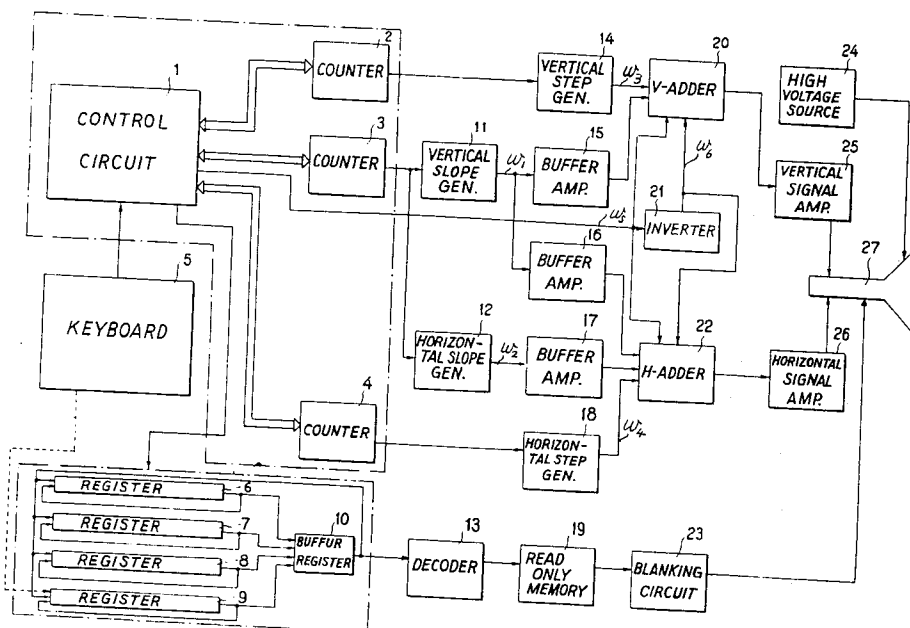
Attorney—Robert E. Burns and Emmanuel J. Lobato

[57]

ABSTRACT

A display system for displaying information patterns on the screen of a cathode-ray tube obtained in a logical operation device, such as a calculator, where counters and registers are commonly used for both the logical operation of the logical operation device and the display operation of the system. The average DC values of the inputs to the vertical signal amplifier and the horizontal signal amplifier for the cathode-ray tube are maintained at stable values at both a period of the logical operation and a period of the display operation in order to eliminate the disturbance and fluctuation of the displayed pattern during the transition — an instant when the operation mode of the system is switched — from the logical operation to the display operation. Slope signals for displaying each digit are generated after a predetermined time from the start of the digit display time for a displayed unit-pattern.

5 Claims, 16 Drawing Figures



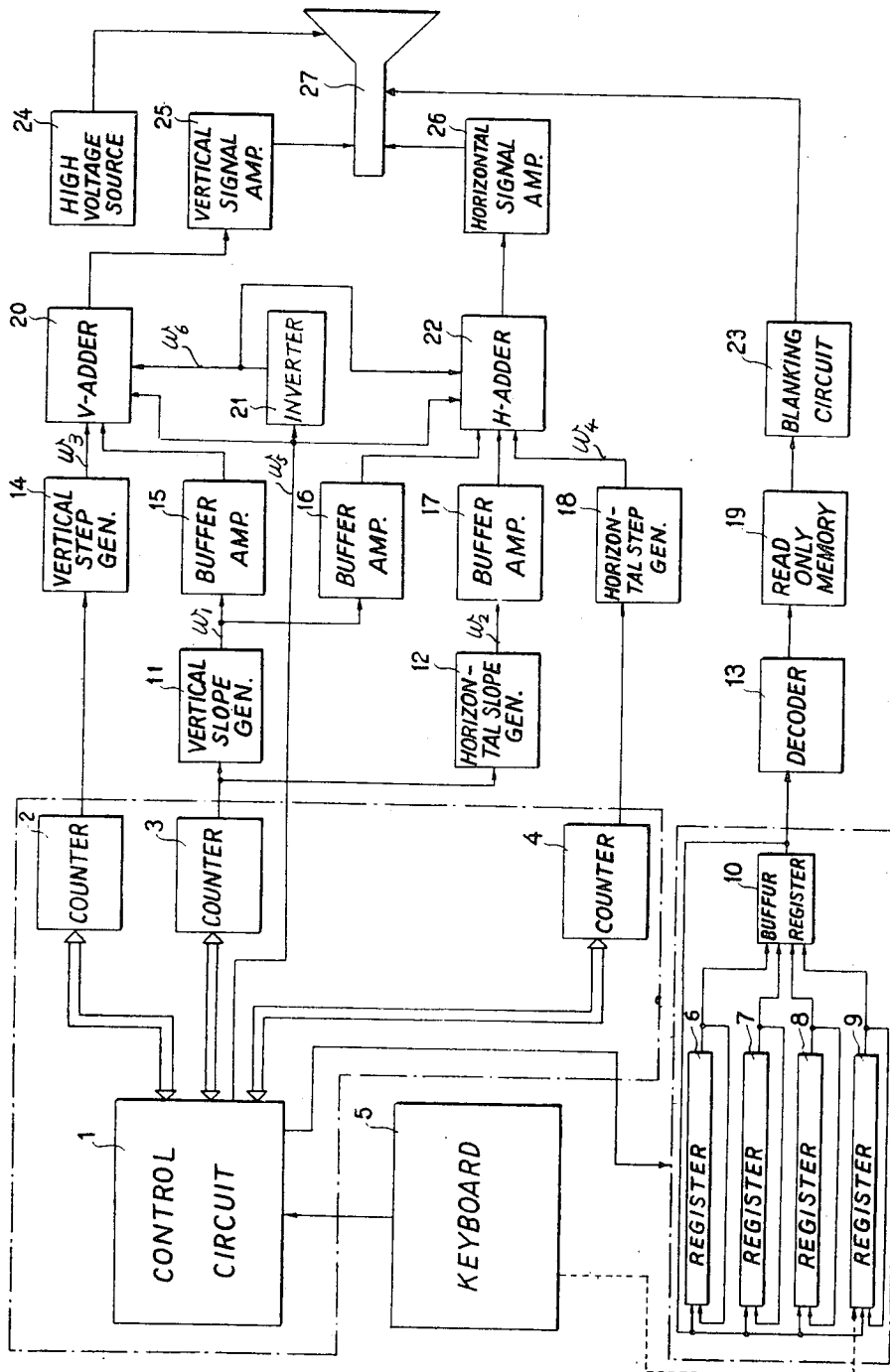


Fig. 1

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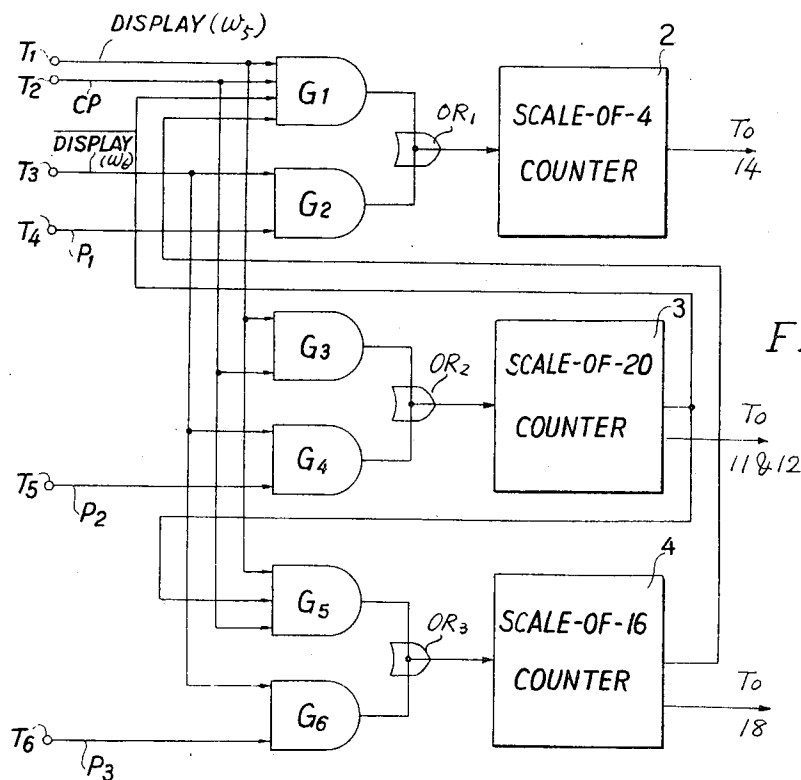


Fig. 2

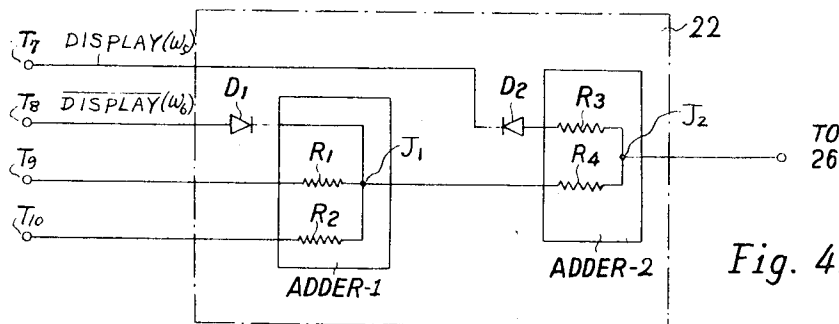


Fig. 4A

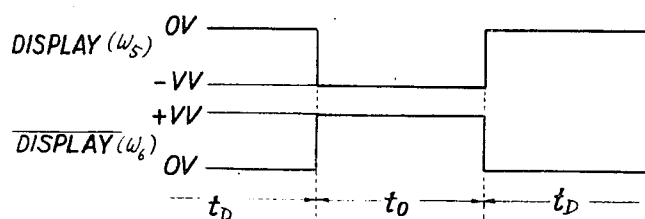


Fig. 4B

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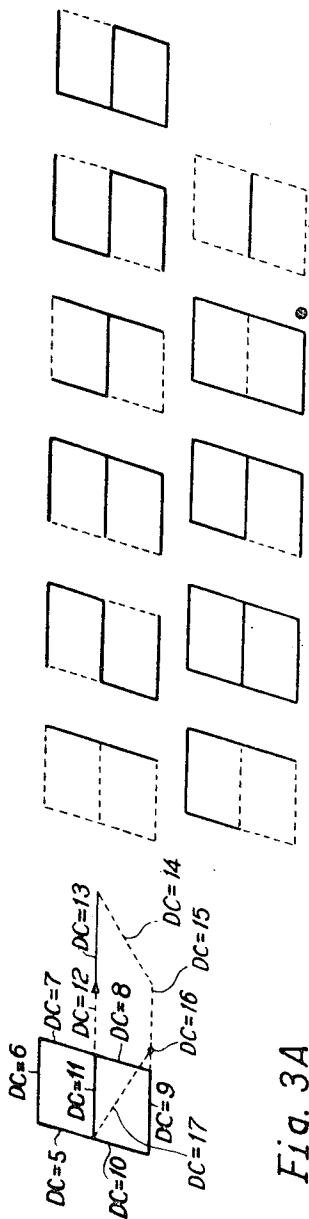


Fig. 3A

Fig. 3B

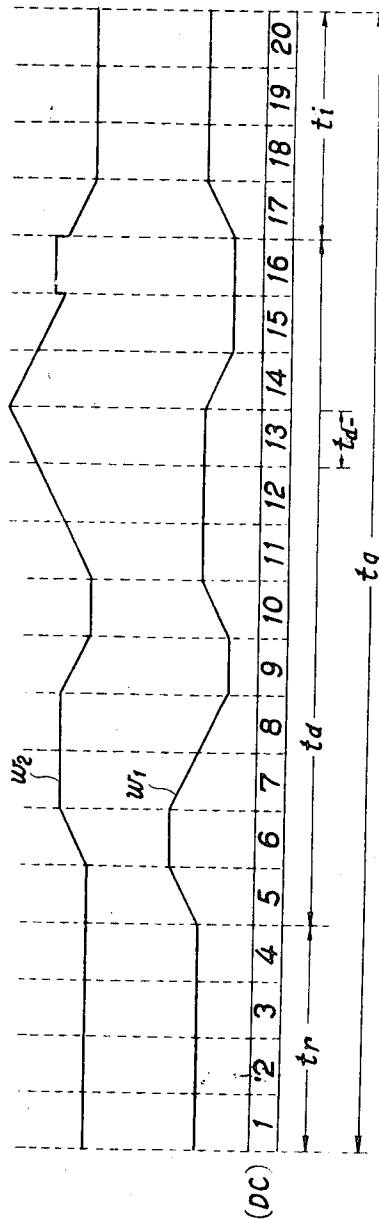


Fig. 3C

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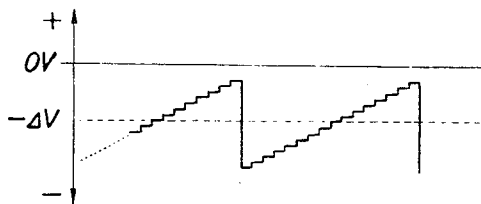


Fig. 5A

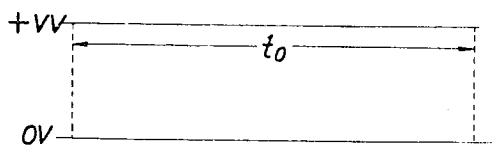


Fig. 5B

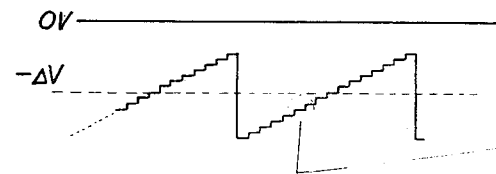


Fig. 5D

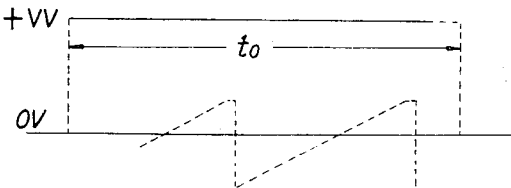


Fig. 5E

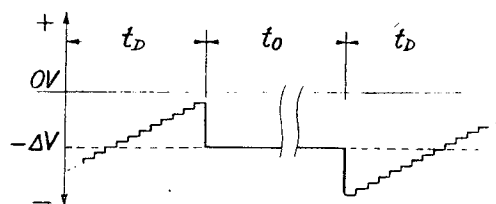
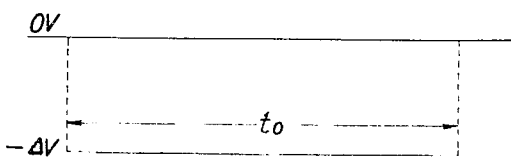
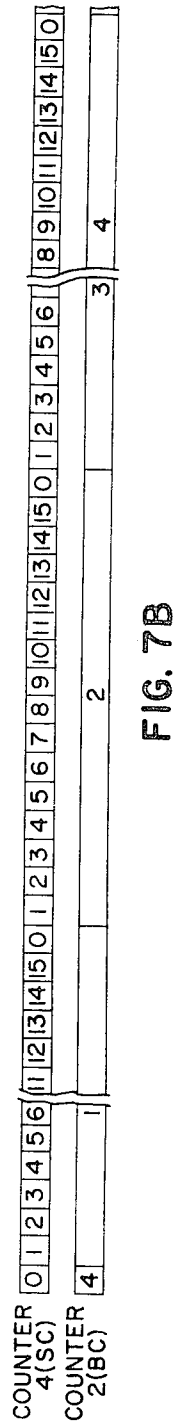
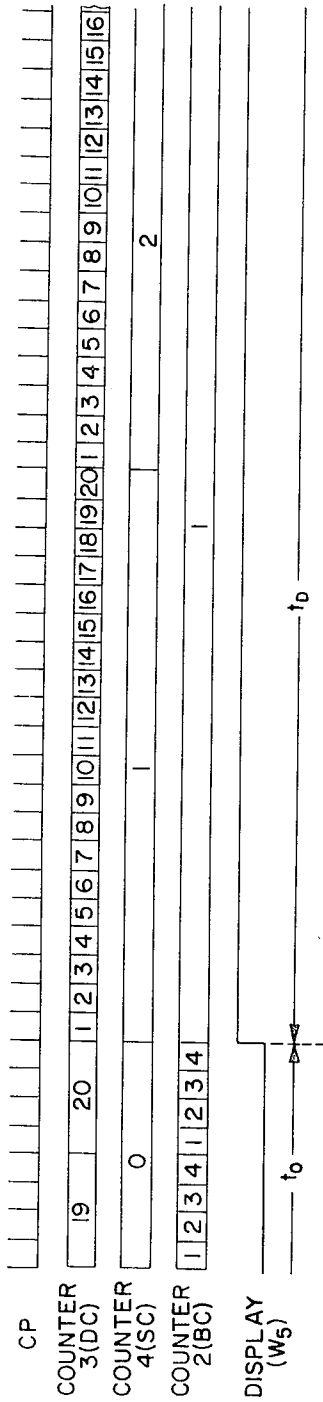
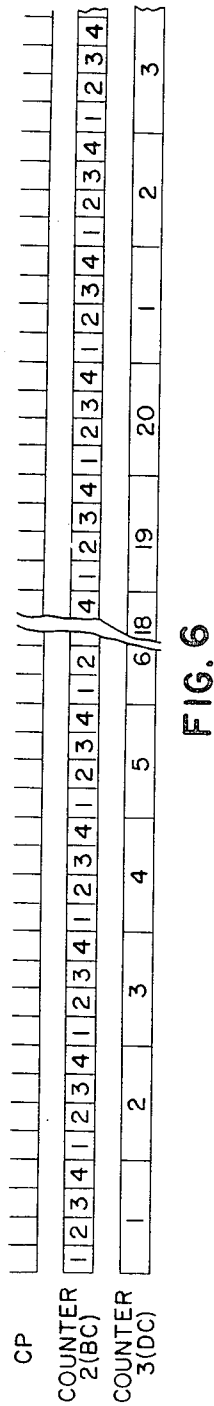


Fig. 5F

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DISPLAY SYSTEM USING A CATHODE-RAY TUBE

BACKGROUND OF THE INVENTION

This invention relates to a display system using a cathode-ray tube and more particularly to a display system for displaying on the screen of a cathode-ray tube pattern information, such as numerals, corresponding to input information in a logical operation device, such as a calculator.

DESCRIPTION OF THE PRIOR ART

Display systems of this type can display a large amount of information and have a display screen which is within the field of view of the operator. However, the cost of the display system of this type is higher than the price of other display systems using indicator tubes, such as a Nixie tube. Accordingly, display systems of this type are usually employed in more sophisticated calculators, whose high prices may be attributed to the following reasons. In a case where a cathode-ray tube is employed to display numerals for a calculator etc., registers and counters used solely for the display operation are provided to eliminate disturbances and fluctuations of patterns displayed on the screen of the cathode-ray tube. Otherwise deflecting circuits for the cathode-ray tube comprise direct-coupling amplifiers. However, these direct-coupling amplifiers are necessarily provided to eliminate "drift," with complicated compensation circuitry for eliminating fluctuations by deviation of temperature (i.e., a temperature-compensating network). Accordingly, the deflecting circuits become expensive.

SUMMARY OF THE INVENTION

An object of this invention is to provide a display system using cathode-ray tube for a logical operation device capable of reduction to practice by the use of a set of counters and registers commonly used for the logical operation and the display operation in an alternately switched manner.

Another object of this invention is to provide a display system using a cathode-ray tube for logical operation device capable of displaying patterns necessary for the logical operation by the use of non-direct-coupled deflection-amplifiers without fluctuation and disturbance of the displayed pattern.

In the display system of this invention, standard pattern signals, each indicative of a predetermined standard pattern, are successively generated, and necessary patterns relating to logical operations performed by the use of counters and registers are displayed on the screen of a cathode-ray tube by blanking the respective standard pattern signals so as to obtain the necessary patterns. In accordance with a feature of this invention, the aforementioned counters and registers are commonly employed for the display operation and the above-mentioned logical operation, and the display function of the cathode-ray tube is interrupted during the period of the logical operation. However, the direct-current voltages applied respectively to the deflection amplifiers at the logical operation time are respectively adjusted so as to be equal to the respective average DC value of the voltages applied to the deflection amplifiers at the display time. Moreover, the generating time of each of the standard pattern signals is determined so as to be shorter than a display time for a unit displayed pattern and so as to be slightly delayed from the start of the display time. As a result of the above construction, fluctuations on the displayed pattern are effectively eliminated, and deflecting circuitry can be constructed without use of the aforementioned direct-coupling amplifiers having such defects.

BRIEF DESCRIPTION OF THE DRAWINGS

The principle of the invention will be better understood from the following more detailed discussion in conjunction with the accompanying drawings, in which the same or equivalent parts are designated by the same or equivalent numerals, characters, and symbols, and in which:

FIG. 1 is a block diagram illustrating an embodiment of this invention;

FIG. 2 is block diagram illustrating an example of control means for counters in the system of this invention;

FIG. 3A is a diagram explanatory of a standard pattern used in the system of this invention;

FIG. 3B shows patterns indicative of numerals which are displayed in the system of this invention;

FIG. 3C shows time charts explanatory of slope waves used in the system of this invention;

FIG. 4A is a circuit diagram illustrating an example of an adder used in the system of this invention;

FIG. 4B shows time charts explanatory of the logical operation time and the display time in the system of this invention;

FIGS. 5A, 5B, 5C, 5D, 5E and 5F are time charts explanatory of the operations of the system of this invention

FIG. 6 shows time charts explanatory of the operations of the system of this invention at the logical operation mode; and

FIGS. 7A and 7B show time charts explanatory of the operations of the system of this invention at an instant when the operation mode of the system is switched from the logical operation to the display operation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

At first, the principle of the system of this invention will be described. With reference to FIG. 1, the operation of the system of this invention is started by controlling a keyboard 5 to instruct a control circuit 1 to control counters 2, 3 and 4 so as to perform logical operations and display operations. In this case, the counter 2 is a scale-of-four counter, the counter 3 a scale-of-20 counter, and the counter 4 a scale-of-16 counter. Input data are applied from the keyboard 5 to a register 9 under control of the counters 2, 3 and 4 to store the input data in the register 9. If instruction for calculation " $A \times B$ " (" C ") is generated by way of example, values " A " and " B " are respectively stored in registers 7 and 8, while the result " C " of this calculation is stored in the register 9. A register 6 is a memory for temporarily storing necessary data. Each of these registers 6, 7 and 8 has a capacity of 16 bits. After the above-mentioned logical operation, the operation condition of this system is changed to display the operation under control of the control circuit 1. Accordingly, one grand cycle of the operation of this invention comprises "logical operation time" and "display time" which are indicated by notations " t_o " and " t_d " respectively. The counters 2, 3 and 4 are originally provided for the logical operation in conventional systems. However, these counters 2, 3 and 4 are used both for the logical operation and the control of display operation in the system of this invention.

In the display time t_d , the contents of the registers 6, 7, 8 and 9 are displayed on the screen of a cathode-ray tube 27 in four lines. For this display, a vertical slope wave w_1 and a horizontal slope wave w_2 are at first generated, by the use of the output pulses of the counter 3, at a vertical slope generator 11 and a horizontal slope generator 12 respectively as standard pattern signals which are successively generated and each representative of a standard pattern

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shown in FIG. 3A. The output pulses of the counter 3 are synchronized with successive changes of the counting state of the counter 3. The vertical slope wave w_1 is applied through a buffer amplifier 15 to a V-adder 20 and added to a vertical step wave w_3 of four steps which is generated at a vertical step generator 14 in response to the output pulses of the counter 2. These output pulses of the counter 2 are synchronized with successive changes of the counting states of this counter 2. The vertical step wave w_3 is employed to successively switch lines of the displayed pattern of numerals. On the other hand, the horizontal slope wave w_2 is applied through a buffer amplifier 17 to a H-adder 22 and added to both the vertical slope wave w_1 applied through a buffer amplifier 16 and a horizontal

step wave w_4 of 16 steps which is generated at a horizontal step generator 18 in response to the output pulses of the counter 4. These output pulses of the counter 4 are synchronized with successive changes of the counting states of this counter 4. The horizontal step wave w_4 is employed to switch digits of the displayed pattern of numerals. The vertical slope wave w_1 applied to the H-adder 22 is employed to incline the displayed patterns of numerals with respect to the vertical direction of the displayed pattern. The output of the V-adder 20 and the output of the H-adder 22 are applied to deflection coils of a cathode-ray tube 27 through a vertical signal amplifier 25 and a horizontal signal amplifier 26 respectively to display standard patterns on the screen of the cathode-ray tube 27 without blanking signals.

On the other hand, the contents of the registers 6, 7, 8 and 9 are successively read out, for one digit of four bits, to a buffer register 10 from the least significant bit positions of each register and applied to a decoder 13, in which each digit read out is decoded. The decoded output of the decoder 13 is applied to a read-only memory 19 storing blanking signals, so that one of the stored blanking signals corresponding to the decoded output of the decoder 13 is applied from the read-only memory 19 to a blanking circuit 23. This blanking circuit 23 controls the cathode-ray tube 27 to blank the unnecessary parts (shown by dotted line in each numeral pattern in FIG. 3B) of the above-mentioned standard pattern so as to obtain a pattern of numeral (shown in FIG. 3B) corresponding to the digits read out from the registers 6, 7, 8 or 9.

In the above-mentioned operations, the displayed patterns of numerals are disturbed or fluctuated at the switching instant from the logical operation time t_0 to the display time t_D due to the time constants of the deflection circuits (25 and 26) and the deflection coil of the cathode-ray tube 27. To eliminate the disturbance and fluctuation of the displayed pattern, a signal DISPLAY (w_5) shown in FIG. 4B is applied to an inverter 21 to obtain a signal $\overline{\text{DISPLAY}}$ (w_6) shown in FIG. 4B. The signal w_6 is applied to both the V-adder 20 and the H-adder 22 to maintain, at respective stable values, the respective direct-current average voltages of the inputs of the horizontal signal amplifier 26 and the vertical signal amplifier 25 at both the logical operation time t_0 and the display time t_D . Moreover, the starts of the slope waves w_1 and w_2 are delayed by four clock pulses from the start of a display time t_D for a displayed unit-pattern, so that a digit to be displayed at a just-succeeding digit display time t_D is read out to the buffer register 10 from one of the register 6, 7, 8 and 9. Thus the principal feature of this invention is that the signal DISPLAY (w_5) and its inverted signal $\overline{\text{DISPLAY}}$ (w_6) are applied to the adders 20 and 22 so as to maintain, at respectively stable values, the respective average DC value of voltages of the inputs of the horizontal signal amplifier 26 and the vertical signal amplifier 25 at both the logical operation time t_0 and the display time t_D , and that a digit to be displayed at a succeeding digit display time t_D is read out to the buffer register 10 at the delayed time t_r (e.g., a time of four clock pulses) to eliminate the effect caused by the time constant of the deflection circuit of the cathode-ray tube 27. The operation of this construction will be described in detail below.

With reference to FIG. 2, operations of the counters 2, 3 and 4 will be described in detail. At the input side of the counter 2 (i.e., a scale-of-4 counter), AND gates G_1 and G_2 and an OR gate OR_1 are provided. To the AND gate G_1 , the signal DISPLAY (w_5), clock pulses CP, and the carry outputs of the counters 3 and 4 are applied from terminals T_1 and T_2 and counters 3 and 4 respectively. To the AND gate G_2 , the signal $\overline{\text{DISPLAY}}$ (w_6) and a first counting pulse train P_1 are applied from terminals T_3 and T_4 . The outputs of the AND gates G_1 and G_2 are applied to the counter 2 through the OR gate OR_1 . At the input side of the counter 3 (i.e., a scale-of-20 counter), AND gates G_3 and G_4 and an OR gate OR_2 are provided. To the AND gate G_3 , the signal DISPLAY (w_5) and the clock pulses CP are applied from the terminals T_1 and T_2 respectively. To the gate G_4 , the signal $\overline{\text{DISPLAY}}$ (w_6) and a

second counting pulse train P_2 are applied from the terminal T_3 and a terminal T_5 . The outputs of the AND gates G_3 and G_4 are applied to the counter 3 through the OR circuit OR_2 . At the input side of the counter 4 (i.e., a scale-of 16 counter), AND gates G_5 and G_6 and an OR circuit OR_3 are provided. To the AND gate G_5 , the signal DISPLAY (w_5), the clock pulses CP and the carry output of the counter 3 are applied from the terminals T_1 and T_2 and the counter 3 respectively. To the AND gate G_6 , the signal $\overline{\text{DISPLAY}}$ (w_6) and a third counting pulse train P_3 are applied from the terminal T_3 and a terminal T_6 . The outputs of the AND gates G_5 and G_6 are applied to the counter 4 through the OR gate OR_3 . The above-mentioned AND gates G_1 , G_2 , G_3 , G_4 , G_5 and G_6 , the OR circuits OR_1 , OR_2 and OR_3 and the terminals T_1 , T_2 , T_3 , T_4 , T_5 and T_6 are provided in the control circuit 1 shown in FIG. 1.

Operations of the counter 2, 3 and 4 at the logical operation time t_0 are as follows. At this time, the signal $\overline{\text{DISPLAY}}$ (w_6) are applied to the AND gates G_2 , G_4 and G_6 , so that all the AND gates G_2 , G_4 and G_6 are opened. The terminal T_2 is coupled with the terminal T_4 in the control circuit 1, so that the first pulse train P_1 corresponds to the clock pulses CP. Accordingly, the counter 2 counts the number of clock pulses CP. Four counting states ($BC=1$, $BC=2$, $BC=3$ and $BC=4$) are employed to indicate four bits of each digit. For example, a digit designated by one true at the counting state $BC=1$ and the three falses at the counting states $BC=2$, $BC=3$ and $BC=4$ corresponds to a decimal number "1", while a digit designated by one true at the counting state " $BC=2$ " and three falses at the counting states $BC=1$, $BC=3$ and $BC=4$ corresponds to a decimal number "2." The carry pulses of the counter 2 are applied to the terminal T_5 as the second pulse train P_2 in the control circuit 1. The number of pulses of the second pulse train P_2 is counted by the counter 3. Twenty counting states ($DC=1$, $DC=2$, ... $DC=20$) of the counter 3 are employed to determine ordinal numbers of digits. For example, serial date obtained at the outputs of the registers 6, 7, 8 and 9 at the counting state ($DC=1$) are determined as a first digit. Similarly, serial date obtained at outputs of the registers 6, 7, 8 and 9 at the counting state ($DC=16$) are determined as a 16th digit. The counter 4 is employed for counting the number of shifts so as to detect how many digits are shifted in the registers from lower to higher. Accordingly, the pulse train P_3 is applied to the terminal T_6 from the control circuit 1 when the number of shifts is to be detected. The 16 counting states of the counter 4 are called as $SC=0$, $SC=1$, ... and $SC=15$. Moreover, the counter 4 is reset to the counting states $SC=0$ except necessary times. In FIG. 6 time charts for the counting states of the counters 2, 3 and clock pulses CP are shown. In the display time, the counters 2, 3 and 4 operates as mentioned below. FIGS. 7A and 7B show the clock pulses CP, states of the counters 2, 3 and 4 and the signal DISPLAY (w_5) at an instant when the operation mode of the system is switched from the logical operation time t_0 to the display operation time t_D . When states $DC=20$ and $BC=4$ are timed with one of the clock pulses CP at the logical operation time after completion of operations caused by instructions by the keyboard 5, the signal DISPLAY (w_5) and the signal $\overline{\text{DISPLAY}}$ (w_6) become true and false respectively. Accordingly, the gates G_2 , G_4 and G_6 are closed while the gates G_1 , G_3 and G_5 are opened.

The scale-of-20 counter 3 counts the clock pulses CP applied through the AND gate G_3 opened by the signal $\overline{\text{DISPLAY}}$ (w_6). In this case, a time for the four counting states representative of "1," "2," "3" and "4" (hereinafter called as $DC=1$, $DC=2$, $DC=3$ and $DC=4$) of this counter 3 corresponds to the time t_r for reading out a digit from one of the registers 6, 7, 8 and 9 to the buffer register 10. A time for the next thirteen counting states representative of "5" to "17" (hereinafter called as $DC=5$, ... $DC=17$) of this counter 3 is the display time t_D for generating the slope waves w_1 and w_2 , while a time for the last three counting states representative of "18," "19" and "20" (i.e., $DC=18$, $DC=19$, and $DC=20$) of the counter 3 corresponds to an idle time t_i . Accordingly, a

carry pulse of the counter 3 indicates the completion of display for one digit.

The carry output of the counter 3 is applied to the AND gate G_3 together with the signal DISPLAY (w_5) and the clock pulses CP. Accordingly, the scale-of-16 counter 4 counts the number of digits displayed by counting the number of carry pulses of the counter 3. Accordingly, the count-up of the counter 4 indicates the completion of display for sixteen digits displayed in one line of the displayed pattern.

The carry output of the counter 4 is applied to the AND gate G_1 together with the signal DISPLAY (w_5), the clock pulses CP and the carry output of the counter 3. Accordingly, the scale-of-4 counter 2 counts the number of lines of the displayed pattern by counting the number of carry pulses of the counter 4. The four counting states of the counter 2 are employed for designating respectively the registers 9, 8, 7 and 6 to be read out to the buffer register 10. Accordingly, a carry pulse of the counter 4 indicates the completion of display for four lines of the displayed pattern.

As mentioned above, the lines of displayed pattern are switched successively in response to each of the carry pulses of the counter 4. In this case, the bias potential in the vertical signal applied from the vertical signal amplifier 25 to the cathode-ray tube 27 must be deviated, by a large deviation voltage, in response to each of successive switching of the displayed lines. In other words, a bias current flowing through the vertical deflection coil of the cathode-ray tube is deviated, by a large deviation current, in response to successive switching of the displayed lines. This deviation current has the largest value at the switching from the highest line to the lowest line of the displayed pattern. However, the step change of the bias current cannot be perfectly carried out due to transient by the time constant of the deflection circuit and the delay of change of a current flowing through the vertical deflection coil. Accordingly, numerals displayed at the beginning part of the switched line are disturbed and fluctuated by the above-mentioned transient at the switching to the next line. To eliminate these undesirable phenomena, the slope waves w_1 and w_2 are generated after four clock pulses from the switching instant changed to the next line of the displayed pattern. Moreover, four bits of information can be transferred to one of the registers 6, 7, 8 and 9 to the buffer register 10 at the time t_r of four clock pulses.

As mentioned above, the counters 2, 3 and 4 and the registers 6, 7, 8 and 9 are commonly used both for the logical operation and for the display operation in the system of this invention. Accordingly, the patterns are not at all displayed on the screen of the cathode-ray tube 27 at the keying operation of the keyboard 5 for instructing data to the calculating means illustrated in FIG. 1 by chain lines or at the logical operation in the above-mentioned calculating means. However, if the system is so designed that the logical operation time is shorter as far as possible, an operator can manipulate this system without embarrassment since the blanking time of the displayed pattern becomes very short.

Next, change of condition of this system from the logical operation time t_0 to the display time t_D will be described. At this time of the change of condition, if the deflection circuit (25, 26) of the cathode-ray tube 27 is constructed by amplifiers without use of direct-coupling (e.g., a capacitive coupling amplifier), complete change to the normal display condition of the entire display system is delayed due to the time constant determined in accordance with the condition of the deflection means of the cathode-ray tube 27. This delay for changing to the normal display condition of the entire display system disturbs the displayed pattern, so that eyes of the operators are fatigued with this disturbance of the displayed pattern.

To eliminate the above-mentioned disturbance of the displayed pattern at the change of condition from the logical operation time t_0 to the display time t_D , each of the adders 20 and 22 are constructed as shown in FIG. 4A by way of example. In the following, the adder 22 is mainly described. However, the adder 20 is similar, in principle, to the adder 22.

The adder 22 comprises an ADDER-1 and an ADDER-2. The ADDER-1 comprises a diode D_1 , resistors R_1 and R_2 connected together to a common junction J_1 to combine the signal DISPLAY (w_6) supplied from a terminal T_8 (connected to the inverter 21), the horizontal step wave w_4 applied from a terminal T_9 (connected to the horizontal step generator 18) as shown in FIG. 5A, and the horizontal slope wave w_2 applied from a terminal T_{10} (connected to the buffer amplifier 17). The output of the buffer amplifier 16 is applied to the common junction J_1 through a resistor. However, this connection means is not shown in FIG. 4A for simple illustration. The signal DISPLAY (w_6) assumes zero volt (0 V) at the display time t_D and a predetermined plus voltage (+V) at the logical operation time t_0 as shown in FIG. 4B. The combined output of the ADDER-1 is further combined with the signal DISPLAY (w_5) supplied from a terminal T_7 (connected to the input of the inverter 21) at the ADDER-2 which comprises a resistor R_4 and a series-connection of a diode D_2 and a resistor R_3 . The resistor R_4 and the series-connection are connected together to a common junction J_2 . The signal DISPLAY (w_5) assumes zero volt (0 V) at the display time t_D and a predetermined minus voltage (-V) at the logical operation time t_0 respectively.

As the result of the above construction of the ADDER-1 and the ADDER-2, a wave on which the horizontal step wave w_4 (shown in FIG. 5A) and the horizontal slope wave w_2 (shown in FIG. 3C) are combined to each other as shown in FIG. 5C is obtained at the output of the ADDER-1 at the display time t_D since the signal DISPLAY (w_6) assumes the zero volt at this display time t_D . On the other hand, since the signal DISPLAY (w_5) assumes also the zero volt at this display time t_D , the wave shown in FIG. 5C is also obtained at the output of the ADDER-2 at this display time t_D .

If the condition of the system is changed from the display time t_D to the logical operation time t_0 under control of the control circuit 1 started in response to the keying of any key on the keyboard 5, the signal DISPLAY (w_6) assumes the voltage +V as shown in FIGS. 5B and 5D since the diode D_1 becomes conductive. Accordingly, the output of the ADDER-1 assumes the voltage +V as shown in FIG. 5D. On the other hand, the output of the ADDER-2 assumes a constant voltage determined by the resistances of the resistors R_3 and R_4 as shown in FIG. 5E since voltage +V and -V are applied to respective terminals of the resistors R_4 and R_3 through the diodes D_1 and D_2 respectively. Accordingly, if the respective resistances of the resistors R_3 and R_4 are so determined that the output of the ADDER-2 at this logical operation time t_0 is equal to the average direct-current value of voltage (i.e., -AV) of the output of the ADDER-2 at the display time t_D as shown in FIG. 5F, disturbance of the displayed pattern caused at the changing time from the logical operation time t_0 to the display time t_D can be eliminated.

What we claim is:

1. A display system for displaying an information pattern in a logical operation device, comprising:
 - a keyboard for generating instructions of an operation mode of a logical operation device,
 - counters for performing said logical operation in accordance with said instructions comprising a first counter for generating a first timing pulse train and carry pulses, a second counter for generating carry pulses and a second timing pulse train timed with each digit of the displayed pattern by stepping said carry pulses of the first counter, and a third counter for generating a third timing pulse train timed with each line of the displayed pattern by stepping said carry pulses of the second counter,
 - a plurality of registers for temporarily storing digital information indicative of process results of said logical operation,
 - means for switching the inputs of said counters,
 - means for generating a vertical slope wave in response to the first timing pulse train,
 - means for generating a horizontal slope wave in response to the first timing pulse train,

means for generating a vertical step wave stepped-up in time with each pulse of the third pulse train,
 means for generating a horizontal step wave stepped-up in time with each pulse of the second pulse train,
 a first adder for combining the vertical step wave with the vertical slope wave,
 a second adder for combining the horizontal step wave with the horizontal slope wave,
 means for maintaining the average voltages of the respective outputs from said first and second adders at respectively stable values irrespective of the presence of a vertical step wave, a vertical slope wave, a horizontal slope wave, or a horizontal step wave at the respective inputs to said first and second adders,
 a cathode-ray tube comprising vertical deflection means, horizontal deflection means, and a brightness modulation means,
 a vertical signal amplifier of a non-direct coupling type for amplifying the output of said first adder for application to the vertical deflection means of the cathode-ray tube,
 a horizontal signal amplifier of a non-direct coupling type for amplifying the output of the second adder for application to the horizontal deflection means of the cathode-ray tube,
 a buffer register for temporarily storing one digit read out from any of said registers within a predetermined time synchronized with pulses of the first timing pulse train, and
 means for generating a blanking signal corresponding to the digit read out of said buffer register for application to the brightness-modulation means of the cathode-ray tube thereby to obtain a desired display pattern on the screen of the cathode-ray tube.

2. A display system according to claim 2, in which four of said registers are to store four lines of said displayed pattern, and the third counter is used as a scale-of-four counter.

3. A display system according to claim 1, in which the first counter is a scale-of-20 counter with which the first four counting states are employed to read out said one digit to the buffer register, the next thirteen counting states are employed for generating the vertical slope wave and the horizontal slope wave, and the last three counting states are employed as an idle time.

4. A display system according to claim 1, in which the second counter is a scale-of- n counter, so that " n " digits are displayed on one line of the displayed pattern.

5. In a display system for displaying on the screen of a cathode-ray tube pattern information in a logical operation device, an improvement comprising: counters and registers used in common for both a logical operation of the logical operation device and the display operation of the system, means for alternately switching said counters and registers between periods of the logical operation and the display operation, means for maintaining the average voltages of respective inputs of a vertical signal amplifier and a horizontal signal amplifier for the cathode-ray tube at stable values in both the period of logical operation and the period of the display operation, means for delaying, by a predetermined time, start of slope waves for each digit from the start of a digit display time, and means for temporarily storing digital information indicative of a just-succeeding displayed digit in said predetermined time, whereby disturbance and fluctuation of the displayed pattern at an instant when the operation mode of the system is switched from the logical operation to the display operation are effectively eliminated.

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